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RESEARCH ARTICLE

1-φ Seven-Level Switched-Capacitor Boost Multilevel Inverter Topology With Optimized Number of Components

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ABSTRACT Increasing the voltage of energy sources, such as photovoltaic (PV), fuel cells, and battery storage units, requires a voltage-boosting technique. This paper introduces an efficient switched-capacitor multilevel inverter (SC-MLI) capable of generating a boosted seven-level output voltage. The key advantages of this topology include the inherent self-balancing of capacitor voltages without the need for auxiliary balancing technique. Additionally, the proposed SC-MLI offers numerous features such as lower voltage stress, improved efficiency, and reduced overall cost. The proposed topology has been evaluated based on parameters such as component count, THD, cost, and efficiency. Experimental validation was conducted on a 1.0 kW prototype setup under varying modulation index and sudden load changes. Finally, a thorough comparison with state-of-the-art seven-level multilevel inverters highlighted the features of the proposed topology.

INDEX TERMS Multilevel inverter, switched capacitor (SC), self-voltage balancing, boost capability.

I. INTRODUCTION

The growing demand for high-quality power in various industries has led to an increase in research on multilevel inverters (MLIs). These industries include motor drives, renewable energy, and electric vehicles. However, conventional MLIs such as Neutral Point Clamped diode (NPC), Flying Capacitor (FC), and Cascaded H-Bridge (CHB) suffer from high voltage stress, higher THD, and low efficiency. To overcome these issues, switched-capacitor multilevel inverters (SC-MLIs) have been developed, offering several advantages over conventional MLIs [1], [2]. SC-MLIs also offer reduced voltage stress and the rate of voltage change (dv/dt), which decreases power losses. However, SC-MLIs require more power semiconductor devices and isolated SC sources, which increases costs and reduces efficiency and reliability.

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To address these problems, Several efforts are being undertaken to generate high voltage levels with fewer components, lesser dc sources, self-voltage balancing properties, and boosting capabilities [3], [4]. These topologies generate higher voltage levels with fewer switches. However, asymmetrical type of configuration increase the switching stress on each switch. The authors in [5] used seven switches, two diodes, and two capacitors to generate 7-level waveform with voltage gain of 1.5. Although the topology uses a reduced number of switches, the diode cause significant power loss. An SC-MLI with a single DC source and four capacitors is described in [6]. Eight power switches and two diodes are used to generate a 5, 7, 9 and 11-levels waveform. Nevertheless, the large number of capacitors used in this topology increases the cost of the inverter. The topology in [7] proposed a 7-level inverter with triple-voltage boosting. To achieve this gain, the topology used three H-bridge cells and three switched capacitors. Recently, a 7-level MLI

topology was developed by [8] using seven power switches and one capacitor to achieve an output voltage of 1.5 gain. However, the configuration utilizes seven diodes, which significantly increases losses and reduces inverter efficiency.

To minimize the voltage stress on the switches, many SC-MLI have been introduced [9], [10], [11], [12]. The author in [9] described an improved configuration that generates seven levels using ten semiconductor switches and two capacitors. The author was able to reduce the voltage stress by limiting switches blocking voltage to V_{dc}. Furthermore, capacitors require a high capacitance. In [10] a 7-level inverter was configured with ten switches, a single DC voltage source, and three capacitors. It can be scaled for higher voltage gain by incorporating four additional switches and exhibits features such as self-voltage balancing, parallel capacitor operation, reduced voltage stress on the switches, and inherent polarity reversal. The authors in [11] improved the efficiency of the inverter and reduced the stress on power devices using an inductor to provide soft charging to the capacitor. In [12], a common ground SC-MLI was proposed, which utilizes nine switches, one diode, and two capacitors to achieve seven levels. The topology presented in [13] is able to generate higher number of voltage levels with fault tolerant capability. However, the topology requires higher number of components.

To reduce the dc source and switched-capacitor current spikes, an inductor is incorporated into the capacitor charging loop [14], [15]. The topology in [14] employs 12 power switches and two capacitors to achieve a triple voltage boost gain, while the topology in [15] utilizes 10 switches and a single capacitor to produce a 7-level output voltage with a voltage gain of 3.0. However, the inclusion of an inductor increases the inverter size and decreases its efficiency.

SC-MLI for grid-connected PV systems was presented in [16], [17], and [18]. Nevertheless, the boosting factor is not sufficiently high compared with other MLI structures that utilize three SC units. This drawback results in reduced reliability, escalated switch capacity requirements, and increased costs of the proposed inverter structure. The topologies discussed in [19], [20], [11], and [21] have triple-boosting capability, but at the same time, they require a large number of components. The compact inverter presented in [22] achieved a reduction in switches for 7-level output with double-boosting gain. This structure required an H-bridge module to generate negative voltage levels. A packed U cell topology is presented in [23]. The topology successfully generates 7 levels using 6 power switches and single switched capacitor fed from single dc source. Nevertheless, due to its lower voltage gain, the topology requires multiple stages of power conversion for implementation with renewable energy.

T-Type SC-MLI was investigated in [24] and [25]. However, the structure uses two different voltage ratings of dc-link capacitors and switched capacitor voltages, which are not recommended in the industry to select power semiconductor devices with different ratings. More recently, an active-neutral-point-clamped (ANPC) inverter based on a novel single-stage boost inverter was investigated. In [26] and [27], hybrid-ANPC was proposed to generating 7-levels with a boost factor of 1.5. It appears that the number of switching capacitors and power semiconductor devices in each MLI topology is constrained. However, they cannot provide an output voltage in an efficient manner. Another T-type NPC topology is presented [28]. The topology implemented control technique to independently control the output voltage to supply single phase or three phase load. T-type topology with minimized voltage stress is presented in [29]. the proposed topology is also superior in its flexible extensibility and capability of supplying inductive loads.

This study introduces an innovative seven-level SCMLI topology with the following attributes to address the aforementioned challenges.

- Reduced number of components.
- Boosting Ability (Vo = 3 × Vin).
- Self-balancing of capacitors.
- Bidirectional power flow capability.
- Minimized voltage stress.

As shown in Fig. 1, the inherent characteristics of the proposed topology make it possible to apply it to a variety of systems, such as fuel cells, battery-powered systems, Solar Photovoltaic (PV) arrays, and industrial motors. Furthermore, the recommended topology is ideally suited for implementation in microgrids, which supply electricity to isolated areas.

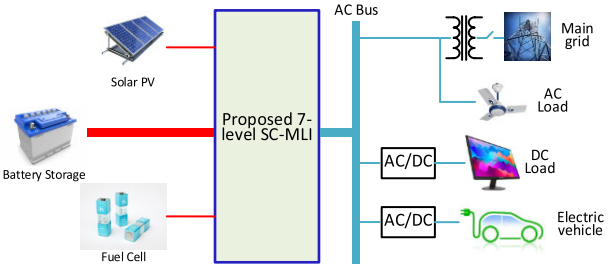


FIGURE 1. The block diagram of the proposed SC-MLI is used to interface various sources and loads.

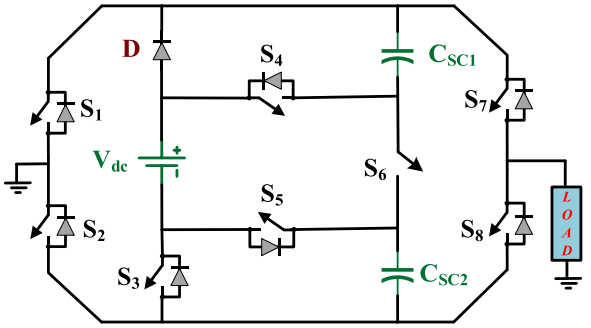


FIGURE 2. Proposed 7-level SC-MLI.

II. PROPOSED SC-MLI TOPOLOGY

A. BRIEF DESCRIPTION OF THE BASIC SC-MLI UNIT

The suggested switching capacitor-based 7-level inverter structure to provide a single AC output voltage is shown in Fig. 2. With a voltage gain of 3.0, this setup creates 7 levels using a single input source (V_{dc}), 7 semiconductor switches ($S_1 - S_5$, S_7, and S_8) with antiparallel diodes, one switch (S_6) without antiparallel diode, and 2 switching capacitors (C_{SC1}–C_{SC2}). To create an output voltage with 7 levels of alternating current, the switching capacitors C_{SC1} and C_{SC2} are alternately charged by the input voltage supply V_{dc} and discharged to the load. Each capacitor experiences a voltage across it of $1.0V_{dc}$, where V_{dc} is the magnitude of the input voltage. Capacitor C_{SC1} is charged to $1.0V_{dc}$ through the activation of switches S_5, S_6, and D whereas capacitor C_{SC2} is similarly charged to $1.0V_{dc}$ by engaging switches S_3, S_4, and S_6.

In Fig. 3, red lines show the direction of current flow during various switching stages. In addition, a green illustration shows how the switched capacitors charge. The voltage levels that the inverter can produce are $0V_{dc}$, $\pm1.0V_{dc}$, $\pm2.0V_{dc}$, and $\pm3.0V_{dc}$. Eight different switching layouts, which correspond to the various operational modes of the proposed inverter, are required to achieve these voltage levels. Fig. 3 shows the switching states for positive and negative voltage generation, explaining the steps required to reach the desired voltage levels.

B. DESCRIPTION OF OUTPUT VOLTAGE STATES

Fig. 3(a-h) illustrate the output voltage levels produced by the suggested topology during the positive and negative cycles. They are explained as follows:

- ***State A*** ($V_o = 0$): In this state, only four switches are activated to produce a zero voltage level, as shown in Fig. 3(d) and (a). During this state, capacitors C_{SC1} and C_{SC1} begins to charge.
- ***State B*** ($V_o = 1.0V_{dc}$): As depicted in Fig. 3(b), capacitors C_{SC1} and C_{SC2} continue charging, resulting in an output voltage of $1.0V_{dc}$.
- ***State C*** ($V_o = 2.0V_{dc}$): Illustrated in Fig. 3(c), this state involves a configuration where capacitor C_{SC1} continue charging while capacitor C_{SC2} start discharging to form $2.0V_{dc}$ level. The current flows through switches S_1, S_5, and S_8. Simultaneously, S_6 turned on to charge the switched capacitor C_{SC1}.
- ***Sate D*** ($V_o = 3.0V_{dc}$): Achieved by following the current path through switches S_1,S_4, S_5 and S_8, as shown in Fig. 3(d). Both of capacitor C_{SC1}& C_{SC2} starts discharging. The output voltage level in this state is $3.0V_{dc}$.

Analyses comparable to this can be conducted for the output voltage negative half cycle. As seen in Fig. 3, the green color represents the charging action of the capacitors, while the red color indicates the direction of current flow during various switching states. The 7-level output voltage generated by the switching pattern shown in Table 1.

TABLE 1. Switching state of the proposed SC-MLI inverter.

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	D	C_{SC1}	C_{SC2}	V_o
1	0	0	1	1	0	0	1	0	▼	▼	$3.0V_{dc}$
1	0	0	0	1	1	0	1	1	▲	▼	$2.0V_{dc}$
1	0	1	0	0	1	0	1	1	▲	▲	$1.0V_{dc}$
1	0	1	0	0	1	1	0	1	▲	▲	zero
0	1	1	0	0	1	0	1	1	▲	▲	
0	1	1	0	0	1	1	0	1	▲	▲	$-1.0V_{dc}$
0	1	1	1	0	1	1	0	0	▼	▲	$-2.0V_{dc}$
0	1	0	1	1	0	1	0	0	▼	▼	$-3.0V_{dc}$

C. BLOCKING VOLTAGE ON POWER SWITCHES

The voltage rating of the switches is a vital factor in deciding the overall cost of the inverter, since it directly influences the selection and sizing of switching components. The highest voltage that a switch must block in order to function determines its voltage rating. Total Standing Voltage (TSV), a crucial indicator for assessing the effectiveness and economy of the inverter design, measures this total blocking capacity across all switches. The maximum blocking voltages for individual switches are stated in the proposed 7-level SC-MLI, which shows the hierarchical voltage distribution throughout the system.

$$V_{S1} = V_{S2} = V_{S7} = V_{S8} = 3.0V_{dc} \quad (1)$$

$$V_{S6} = 2.0\ V_{dc} \quad (2)$$

$$V_{S3} = V_{S4} = V_{S5} = V_D = 1.0V_{dc} \quad (3)$$

where, V_{S1}, V_{S2}, V_{S3}, V_{S4}, V_{S5}, V_{S6}, V_{S7}, V_{S8}, and D are the maximum voltage stress across the switches S_1, S_2, S_3, S_4, S_5, S_6, S_7, S_8,and diode D. Therefore, TSV of the topology will be,

$$TSV = 4 \times 3.0\ V_{dc} + 1 \times 2.0\ V_{dc} + 4 \times 1.0V_{dc} = 18.0\ V_{dc} \quad (4)$$

As the peak output voltage is 3.0Vdc, hence

$$TSV_{pu} = \frac{18V_{dc}}{3.0V_{dc}} = 6.0 \quad (5)$$

Fig. 4 depicts the voltage stress distribution on various switches.

D. CONTROL STRATEGY

Single-carrier sinusoidal pulse width modulation (SC-SPWM) is used to reduce the computational complexity associated with multi-carrier modulation methods and avoid the requirement for synchronization between numerous triangle signals. The final pulses achieved by comparing a single triangular carrier signal with a sinusoidal modulating signal. The fundamental idea behind the suggested switching technique is to compare the triangle carrier signal at the intended switching frequency with the reshaped reference signal, which has been sinusoidally corrected to fit inside

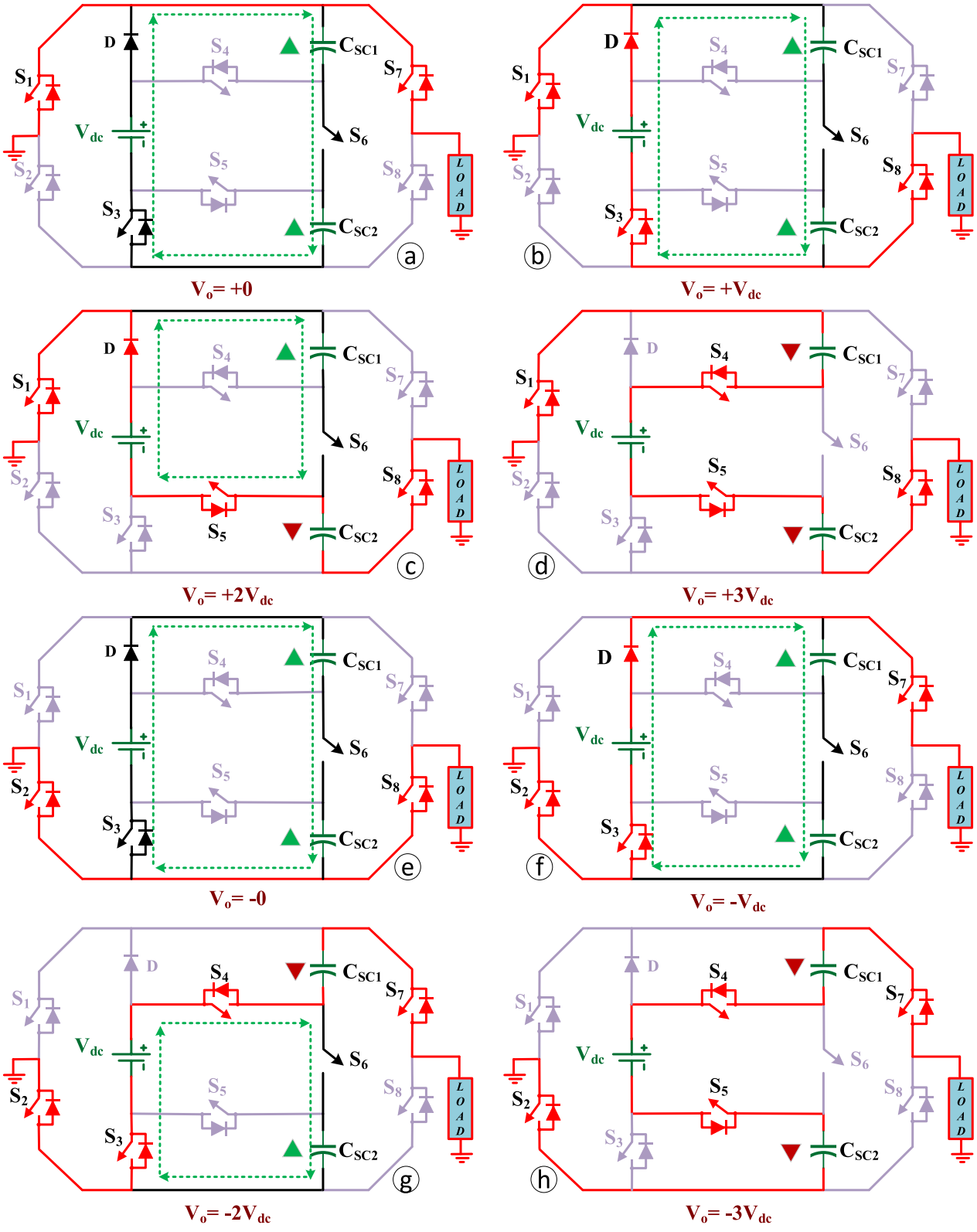


FIGURE 3. Positive voltage states of the proposed 7-level SC-MLI.

the single triangular carrier range. The modulating signal, following reshaping, has an amplitude of (A_{ref}), whereas the triangular carrier has a peak amplitude of (A_{tri}). Fig. 5 illustrates the evolution of the comparison zone on both the

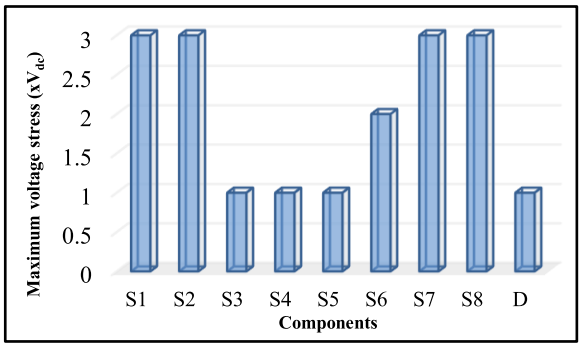


FIGURE 4. Voltage stress distribution of various switches.

positive and negative sides of the sinusoidal reference. The modulation index Ma is mathematically defined as

$$M_a = \frac{A_{ref}}{A_{tri}} \tag{6}$$

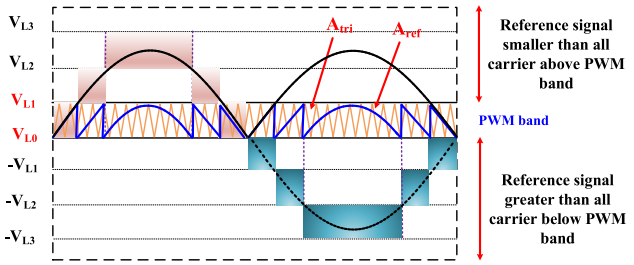


FIGURE 5. Modulation scheme.

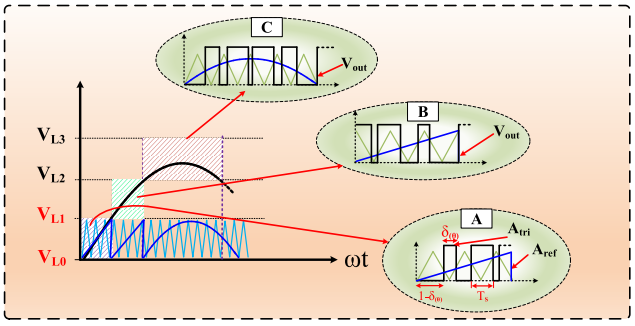


FIGURE 6. PWM expansion for different areas.

E. SIZING OF THE CAPACITORS

In switched capacitor-based inverters, choosing the proper switched capacitors (SC) is essential for reducing voltage ripple, which has an impact on the output voltage's quality. The performance of the inverter is enhanced by appropriate SC selection, which reduces ripple and harmonic distortion [23].

During the voltage levels $\pm 3.0V_{dc}$ and $\pm 2.0V_{dc}$, the floating capacitors (C_{SC1}- C_{SC2}) discharges. These two voltage levels are symmetrical during the positive and negative half-cycle. The modulation index M_a is set to 1.0 to make the study of required capacitance and natural voltage balance easier to understand. As illustrated in Fig. 5,

This method of analyzing the operation during the positive half-cycle proposed by author [30]. Understanding the implications on capacitance requirements and capacitor voltage balance is much easier with this method.

1) Area (A): Voltage levels 0 and $1.0V_{dc}$ are fluctuate during operations in Area-A. The rectified reference signal (A_{ref}) is almost linear throughout each carrier period (T_S) due to the high carrier frequency. This makes it possible to compute duty cycle (δ) for levels 1.0 and 0 in area-A more simply, as shown by equation:

$$\begin{cases} \delta_{1.0} = \delta_\theta = \sin\theta \\ \delta_0 = 1 - \delta_\theta = 1 - \sin\theta \end{cases} \tag{7}$$

The voltage (V_{dc}) will shape the level $1.0V_{dc}$. The following formula can be used to find the total charge in area-A (Q_A) that was applied to the load with a value of (Z_L)

$$\begin{aligned} Q_A &= \frac{1}{\omega}\int_0^{\theta_1} i_o d(\omega t) \\ &= \frac{1}{\omega}\int_0^{\theta_1}\left[0\cdot(1-\delta(\theta)) + \frac{V_{dc}}{Z_L}\delta(\theta)\right]d(\omega t) \\ &= \frac{1}{\omega}\int_0^{\theta_1}\left[0\cdot(1-\sin(\theta)) + \frac{V_{dc}}{Z_L}\sin(\theta)\right]d(\omega t) \end{aligned} \tag{8}$$

where Z_L represents the output load. θ_1 is the switching angle of area-A as shown in Fig. 6.

2) Area (B): In this region, the output voltage alternates between $1.0V_{dc}$ and $2.0V_{dc}$. The corresponding duty cycles during the carrier period T_S are mathematically defined:

$$\begin{cases} \delta_{2.0} = \delta_\theta = \sin\theta \\ \delta_{1.0} = 1 - \delta_\theta = 1 - \sin\theta \end{cases} \tag{9}$$

Here, level 1.0 V_{dc} is equal V_{dc}. Where, level $2.0V_{dc}$ is the same as ($V_{dc} - V_{C_{SC1}}$) voltage. Therefore, Q_B supplied to the load can be obtained as:

$$\begin{aligned} Q_B &= \frac{1}{\omega}\int_{\theta_1}^{\theta_2} i_o d(\omega t) \\ &= \frac{1}{\omega}\int_{\theta_1}^{\theta_2}\left[\frac{V_{dc}-V_{C_{SC2}}}{Z_L}(1-\delta(\theta)) + \frac{V_{dc}}{Z_L}\delta(\theta)\right]d(\omega t) \\ &= \frac{1}{\omega}\int_{\theta_1}^{\theta_2}\left[\frac{V_{dc}-V_{C_{SC1}}}{Z_L}(1-\sin(\theta)) + \frac{V_{dc}}{Z_L}\sin(\theta)\right]d(\omega t) \end{aligned} \tag{10}$$

3) Area (C): The output voltage in Area (C) alternates between $2.0V_{dc}$ and $3.0V_{dc}$. To determine how long

each voltage level is applied, the corresponding duty cycles for these levels during the carrier time are computed:

$$\begin{cases} \delta_{3.0} = \delta_\theta = \sin\theta \\ \delta_{2.0} = 1 - \delta_\theta = 1 - \sin\theta \end{cases} \tag{11}$$

In this region, voltage level 3.0V_{dc} is equal to $(V_{dc} + V_{C_{SC1}})$, and voltage level 2.0V_{dc} is equal to $V_{dc} + V_{C_{SC1}} + V_{C_{SC2}}$.. Hence, the total charge (Q_C) can be determined by:

$$\begin{aligned} Q_C &= \frac{1}{\omega}\int_{\theta_2}^{\theta_3} i_o d(\omega t) \\ &= \frac{1}{\omega}\int_{\theta_2}^{\theta_3}\left[\frac{V_{dc}+V_{C_{SC1}}}{Z_L}(1-\delta(\theta)) \right. \\ &\qquad \left. + \frac{V_{dc}+V_{C_{SC1}}+V_{C_{SC2}}}{Z_L}\delta(\theta)\right] d(\omega t) \\ &= \frac{1}{\omega}\int_{\theta_2}^{\theta_3}\left[\frac{V_{dc}+V_{C_{SC1}}}{Z_L}(1-\sin(\theta)) \right. \\ &\qquad \left. + \frac{V_{dc}+V_{C_{SC1}}+V_{C_{SC2}}}{Z_L}\sin(\theta)\right] d(\omega t) \end{aligned} \tag{12}$$

The total charge in the negative half-cycle is similarly characterized due to the symmetric operation of (C_{SC1}- C_{SC2}) and can be calculated as:

$$Q_{-A} = \frac{1}{\omega}\int_{0}^{\theta_1}\left[0\cdot(1-\sin(\theta)) + \frac{V_{dc}}{Z_L}\sin(\theta)\right] d(\omega t) \tag{13}$$

$$Q_{-B} = \frac{1}{\omega}\int_{\theta_1}^{\theta_2}\left[\frac{V_{dc}-V_{C_{SC2}}}{Z_L}(1-\sin(\theta)) + \frac{V_{dc}}{Z_L}\sin(\theta)\right] d(\omega t) \tag{14}$$

$$\begin{aligned} Q_{-C} &= \frac{1}{\omega}\int_{\theta_2}^{\theta_3}\left[\frac{V_{dc}+V_{C_{SC2}}}{Z_L}(1-\sin(\theta)) \right. \\ &\qquad \left. + \frac{V_{dc}+V_{C_{SC1}}+V_{C_{SC2}}}{Z_L}\sin(\theta)\right] d(\omega t) \end{aligned} \tag{15}$$

The average current (i_{avg}) passing through the neutral point over one fundamental cycle can be derived from equations (8), (10), (12), (13), (14), and (15), reflecting the net current contributions from various operational states as:

$$\begin{aligned} & i_{avg} \\ &= \frac{2}{T}\sum_{i=A}^{D}(Q_x - Q_y) = 0 \\ &\Rightarrow \frac{2}{\omega T Z_L}\begin{bmatrix} (4+2\pi-\theta_1-3\theta_3) - 4(\cos\theta_1+\cos_{\theta 3}) \\ -(V_{C_{SC1}}-V_{C_{SC2}})(4+2\pi-2\theta_1+4\theta_2-6\theta_3 \\ +8(\cos\theta_1-\cos\theta_2+\cos\theta_3)) \end{bmatrix} = 0 \end{aligned}$$

$Q_x \equiv Q_A,\ Q_B,\ and\ Q_C\ ;\ Q_y \equiv\ Q_{-A},\ Q_{-B}, and\ Q_{-C}$

At the steady state of capacitors the average current should be 0. Hence, we can achieve $V_{C_{SC1}} = V_{C_{SC2}} = 1.0V_{dc}$. Therefore, The voltage across the switched capacitor will be naturally balanced without the need of external circuit. The gate pulses necessary for the proposed 7-level SC-MLI switching operation have been generated to perform all three functions (active power, reactive power, and capacitor charging) as illustrated in Fig. 7.

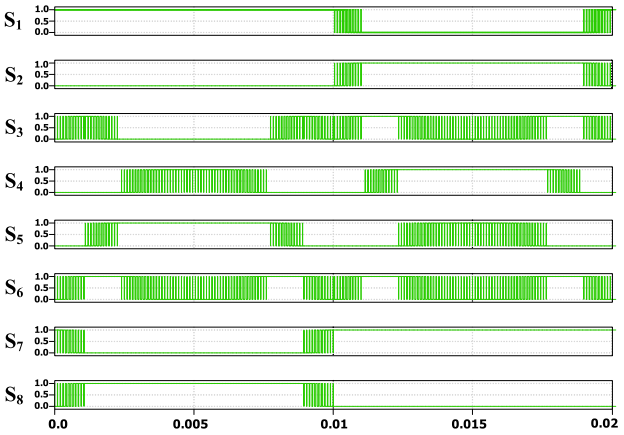


FIGURE 7. Gate pulses of the power switches S1 - S7 (a-g) of theproposed 7-level SC-MLI.

III. COMPARATIVE ANALYSIS WITH CONTEMPORARY SEVEN-LEVEL INVERTERS

In this section, the practicality of the presented SC-MLI is validated by comparing the number (N_{SW}), number of drivers (N_{GD}), number of capacitors (N_C), per unit value of voltage stress ($TSV_{p.u}$), and the total efficiency (η). Table 2 presents a detailed comparison of these topologies based on the selected criteria.

The proposed topologies in [10], [16], [24], [25], and [26], capable of generating 7 output voltage levels. Nevertheless, these topologies require high number of components. The voltage ratings of these components are more and it offer lower voltage gain which considered high cost topologies. The authors in [20] and [22] proposed high gain configuration. However these topologies suffer from high voltage stress on power switches which increases the losses and [20] requires a backend H-bridge and two dc sources.

In terms of reliability, the capacitors are an important parameter and the proposed 7-L topology has a fewer number of capacitors than that in [10]. Although the topology presented in [19] requires only two capacitors, it has a large number of switches with four additional diodes. In addition, the proposed topology has significantly lower TSV p.u., However, [12] and [19] has low TSV p.u. but it faces the problem of high number of components.

Cost and conducting device analysis of the proposed 7-L topology has been studied in more details. By taking into account the number of devices and their voltage ratings, the

cost factor (CF) of the topologies can be calculated [11].

$$CF = \frac{(N_{IS} + N_{SW} + N_d + N_c + N_{gd} + TSV_{pu})}{N_L} \quad (16)$$

The CF of the topologies is presented in Table 2. It can be observed that the topologies in [10], [12], [17], [18], [19], [20], [22], [24], and [25] have higher costs due to their requirement for a higher component count. The topology presented in [23] has a lower cost compared to the proposed topology. However, it has lower voltage gain and efficiency compared to the proposed topology.

The efficiency has been estimated using PLECS software and the thermal modelling of the proposed topology. The contribution of the components such as power switches, diode, and SCs in the power loss has been given in Fig. 8(a). Fig. 8(b) shows the fluctuation of the suggested topology efficiency in relation to the load placed on the inverter. It can be observed that when the load demand on the proposed 7-level SC-MLI increases, the inverter efficiency falls. However, at 1.0 kW, the proposed topology achieved 95.3%.

The proposed topology has a lower value of *CF* than the majority of the topologies shown in Table 2. An efficient and cost-effective power electronics circuit's design greatly depends on a thorough understanding of its power loss. The associated conduction losses, switching losses, and losses in capacitors are the four significant losses that are taken into account while performing a loss analysis of a power circuit. The total power losses calculated using PLECS software. Infineon IKW25N120H3 IGBT power switches used to estimate these losses. The average total conducting device average in the proposed topology are less than that of topologies of [19] and [24]. Table 2 presents the efficiency comparison, showing that the suggested 7-L outperforms all other topologies.

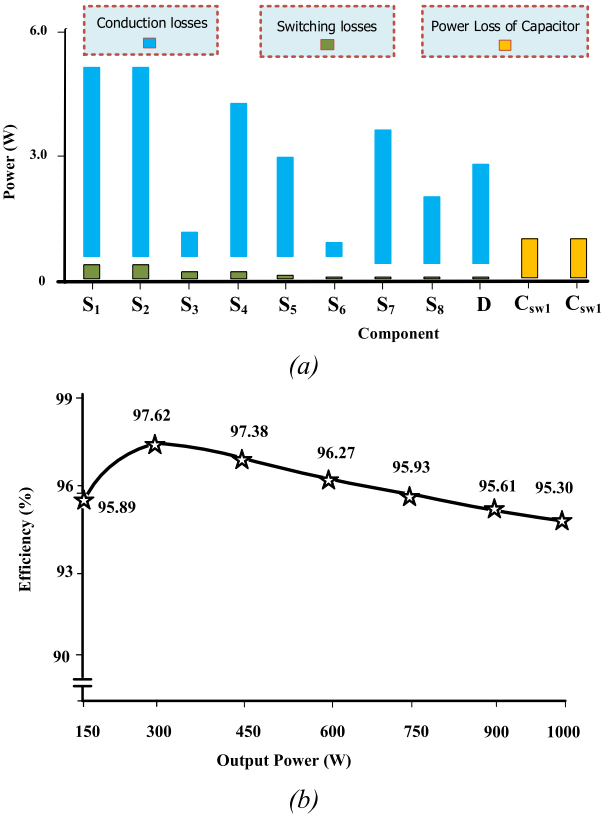


FIGURE 8. Power Loss analysis of the invented topology with (a) powerloss distribution and (b) efficiency plot.

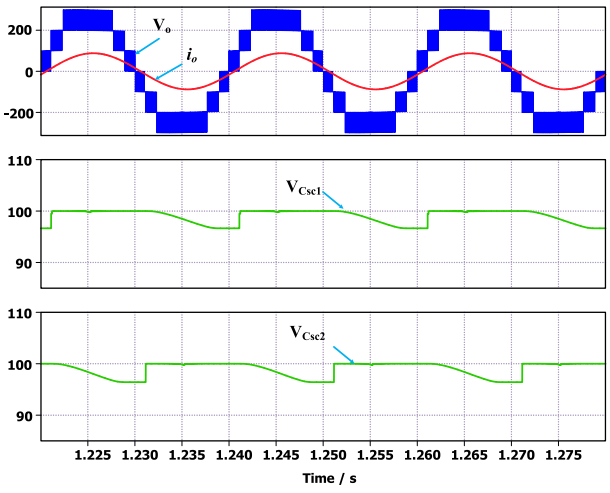


FIGURE 9. Simulation results under steady state condition.

IV. RESULTS AND DISCUSSION

This section analyzes and discusses the simulation and experimental results of the proposed quadruple-boost 7-level inverter.

A. SIMULATION RESULTS

To assess the performance of the proposed MLI architecture, a variety of static and dynamic scenarios have been simulated.

To evaluate the performance of the proposed MLI architecture, The topology was tested under various load conditions including changing load type, changing modulation index, and when there is sudden change in load parameters. The simulation results were obtained using PLECS software. A 100V source was used to assess the inverter's performance.

The load voltage, load current, and capacitor voltages (V_{CSC1}, V_{CSC2}) are shown in Fig. 9 under steady state. It can be observed that the capacitors remain balanced and achieving 7-levels at output voltage.

Additionally, a dynamic condition test is performed on the topology when sudden change on load from (20Ω+40mH) to (10Ω+20mH) as depicted in Fig. 10. The sinusoidal current waveform that followed the load change instant is seen in this result. Another dynamic circumstance that is taken into consideration is a change in the modulation index (M_a), which comes after the scenarios where the load undergo change. This scenario is illustrated in Fig. 11. At $M_a = 1.0$. It can be observed that, the output voltage levels are generated with full control over capacitor voltage. Also, it is noticed that even after M_a was to 0.5 and then 0.2, the recommended topology continued to work effectively with fewer levels.

TABLE 2. Comparison table for different MLI-Topologies with proposed topology.

Top.	N_L	G	N_{IS}	N_{SW}	N_{GD}	N_C	N_D	$TSV_{p.u}$	*CF*	η / f_{sw} /p_o
[10]	7	1:1.5	1	10	8	3	-	6.67	4.09	94.5%, 5kH, -
[12]	7	1:3	1	10	10	2	1	6.0	4.29	97.63%, 5kH, 100W
[17]	7	1:1.5	1	10	10	2	-	7.67	4.38	- 5kH, 700W
[18]	7	1:3	1	10	10	2	-	7.5	4.38	95.5%, 5kH, 1kW
[19]	7	1:3	1	9	9	2	4	5.67	4.24	94.3%, 10kH, 250W
[20]	7	1:3	1	11	11	2	-	7.67	4.67	92.54%, 10kH, 150W
[22]	7	1:3	2	8	8	-	-	12.0	4.29	98%, 5kH, 1kW
[23]	7	1:1.3	1	6	6	1	0	6.0	2.86	96.11%, 2kH, 990W
[24]	7	1:1.5	1	8	8	1	4	7.67	4.24	88.1%, 2.5kH, 200W
[25]	7	1:1.5	1	10	10	2	-	8.67	4.52	96.8%, 5kH, 150W
[26]	7	1:1.5	1	9	9	1	-	6.33	3.76	96.7%, 5kH, -
[29]	7	1:1.5	1	10	9	2	0	5.33	3.90	95%, 5kH, 250W
[P]	**7**	**1:3**	**1**	**8**	**8**	**2**	**1**	**6.0**	**3.70**	**97.62%, 5kH, 300W**

N_L= Number of levels, G = voltage boost ratio, N_{IS}= number of input dc sources, N_{SW}= Number of switches, N_C=Number of flouting capacitors, N_{GD}=Number of gate drivers, $TSVp.u.$= Total Standing voltage, N_D= Number of diodes, η= Efficiency, f_{sw} = Switching frequency, p_o = Output power

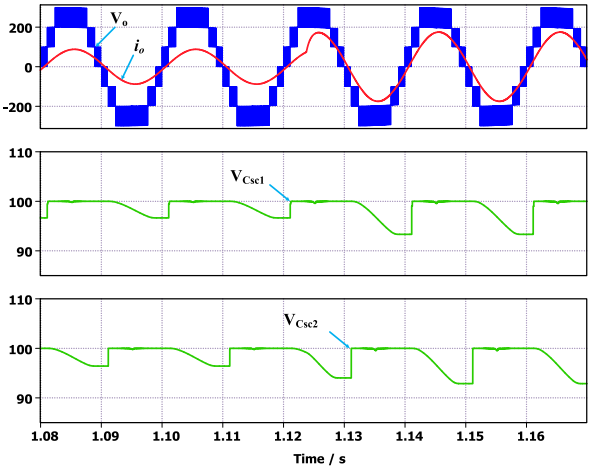


FIGURE 10. Simulation results under load change.

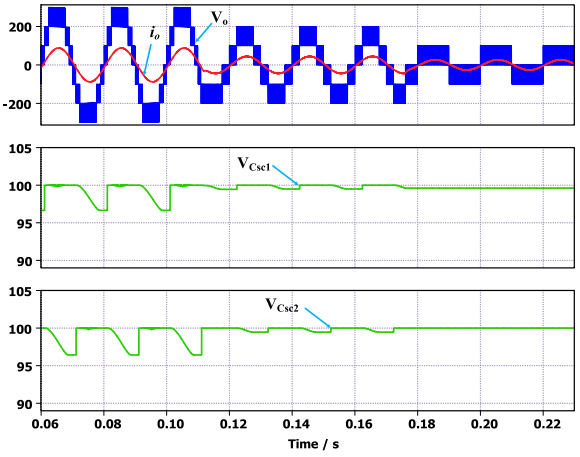


FIGURE 11. Simulation results under modulation index change.

These results show that the proposed circuit can work in a range of operational conditions.

B. EXPERIMENTAL RESULTS

A laboratory prototype with a power rating of 1.0kW is prepared in order to confirm the performance of proposed topology. Experimental results are recorded under various load scenarios. The experimental configuration of the proposed inverter is shown in Fig. 12. In order to generate gate pulses for power semiconductor switches, SC-PWM is implemented and TMS320F28379D microcontroller is used to fire power switches. The specification of experimental setup is shown in Table 3.

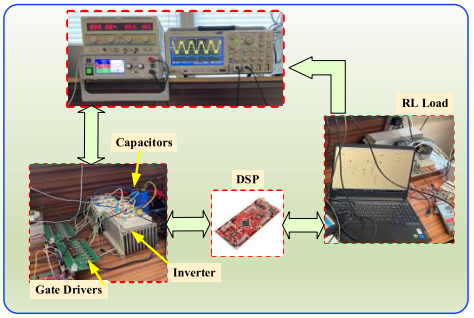


FIGURE 12. Prototype setup.

As shown in Fig. 13(a) & (b), the maximum magnitude of the output voltage is 300V with a voltage step of 50V

TABLE 3. Parameters of experimental setup.

Parameters	Value
Switches	G60N100 IGBT
Capacitor	1200µF, 150V
DSP Controller	TMS320F28379D
RL load	R=30Ω, L= 60mH
Input DC Source Voltage	100V
Switching Frequency	5kHz

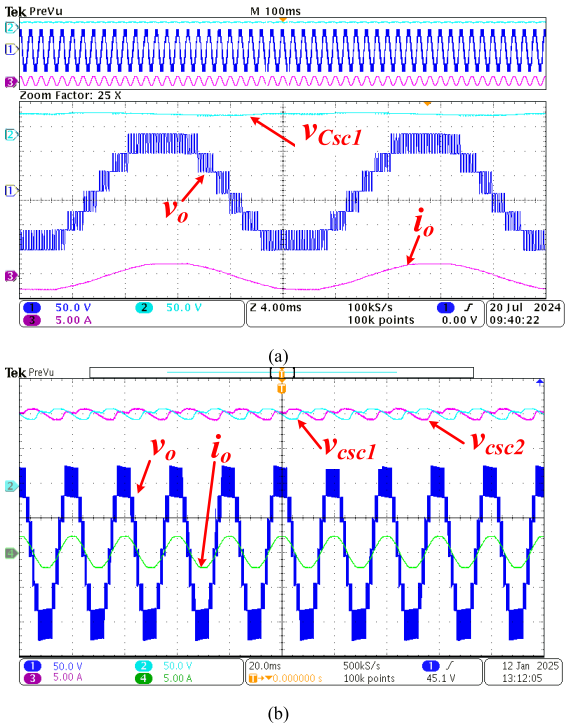


FIGURE 13. Experimental results (a) 7 level output voltage (b) RL load.

when the voltage supply of input magnitude is 100V. The waveforms of the switched capacitors voltage, output voltage, and load current with a (30Ω + 60mH) load are displayed in Fig. 13 (a) & (b).

The prototype configuration is prepared to validate the proposed topology under load fluctuation from R=30Ω, L=60mH to R=15Ω, L=30mH and from R=15Ω, L=30mH to R=30Ω, L=60mH. The associated waveforms are displayed in Fig. 14(a) & (b). It demonstrates that under conditions of sudden load changes, the proposed topology can maintain the SC voltages and output voltage levels. Furthermore, the variation of the modulation from 1.0 to 0.5 and from 1.0 to 0.2 is implemented in the experimental setup and corresponding results are shown in Fig. 15 (a) & (b) confirming the satisfactory dynamic performance. It can be seen that the proposed topology is able to offer a voltage gain of 3.0 when M_a fluctuates between (1.0 and 0.7). However, when M_a is between (0.7 and 0.3), the voltage gain drops to ($V_O = 2.0V_{dc}$). Finally, if M_a drops below 0.3, the inverter generates two levels at unity gain. The main feature of this topology is that the inverter continues supplying the load

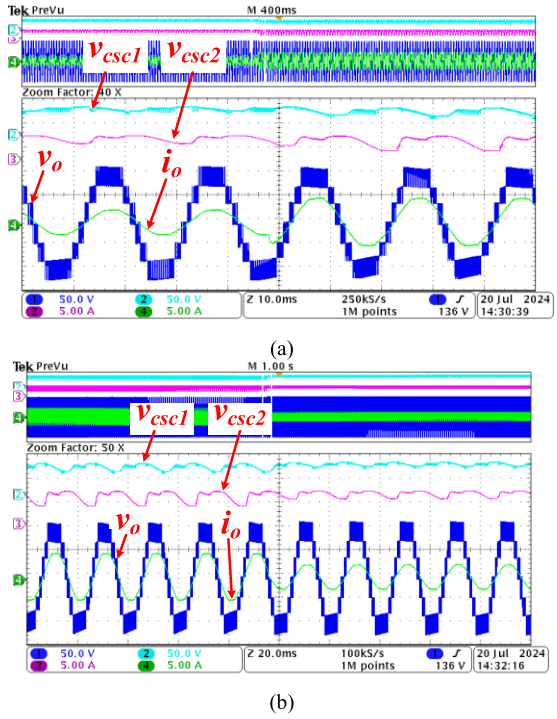


FIGURE 14. Experimental results under modulation index variations.

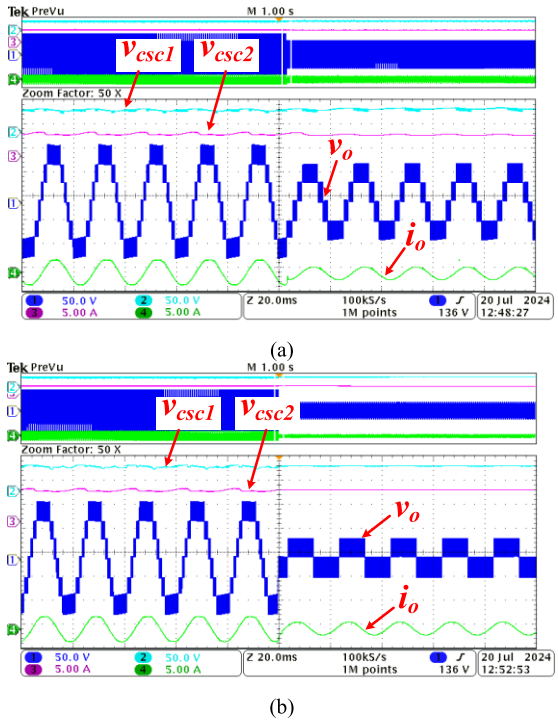


FIGURE 15. Experimental results of modulation index variations: a) fromMa=1.0 to 0.5, and b) from Ma=1.0 to 0.2.

even under a low modulation index. This capability ensures reliable operation during a wide range of modulation indices.

Another test is conducted to verify the performance of the proposed topology for various load types. A sudden load

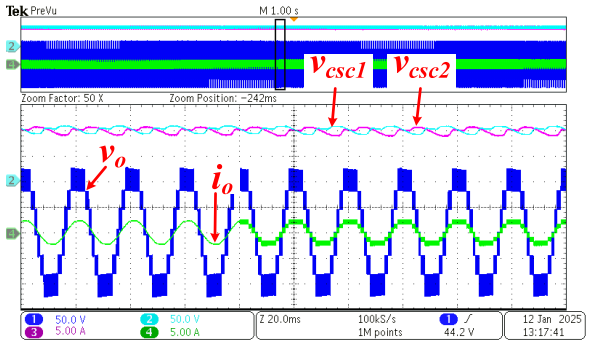


FIGURE 16. Experimental results with load type change.

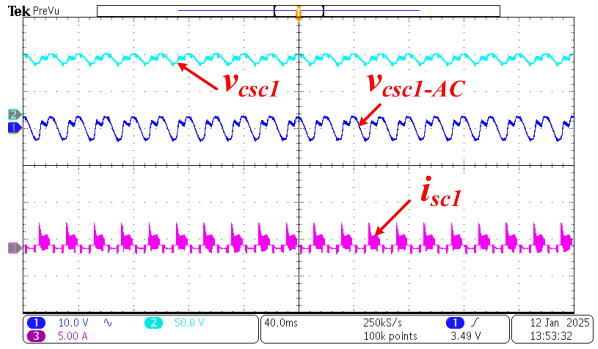


FIGURE 17. Waveforms of SC Voltage, ac components, and current.

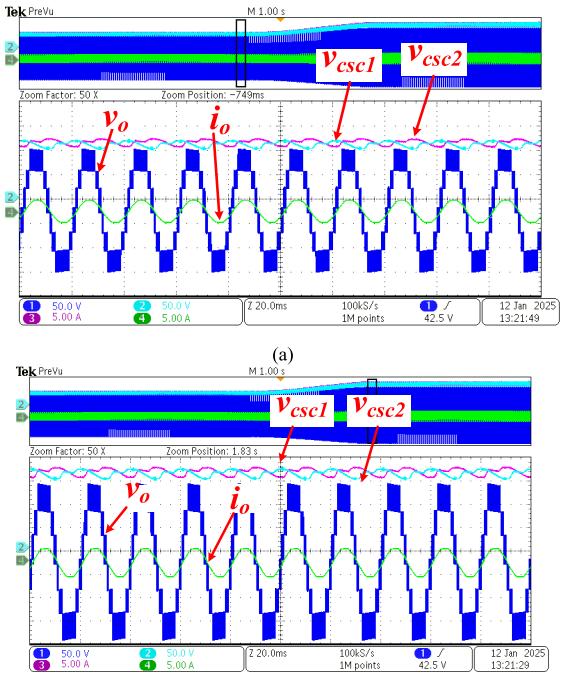
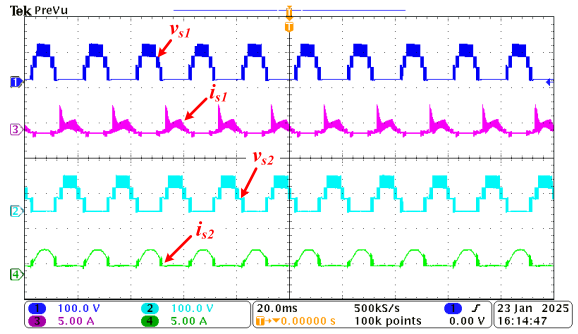
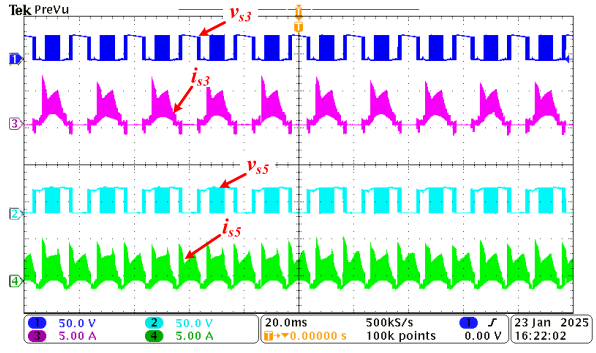


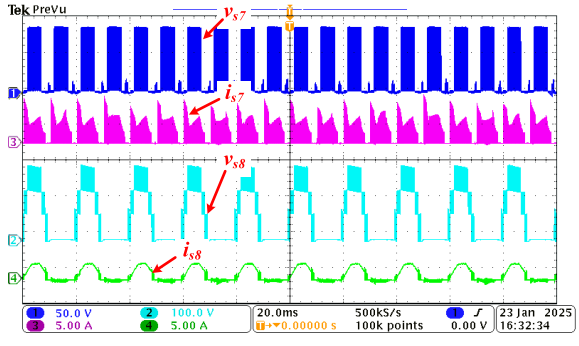
FIGURE 18. Experimental results under input voltage variations.



(a)



(b)



(c)

FIGURE 19. Experimental results of switches current and voltage.

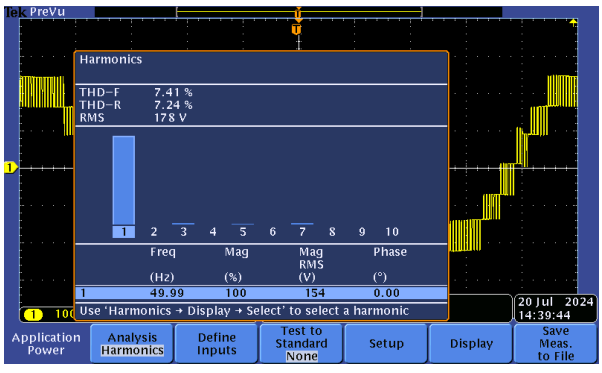


FIGURE 20. Harmonic profile of output voltage at 50Hz.

change from (30Ω + 60mH) to a purely resistive load of (30Ω). Its observed that, the inverter effectively maintains capacitor voltage balance under this condition, as shown in Fig.16.

In order to show the self-balance of both switched capacitors, switched capacitor (v_{sc1}) voltage along with its ac components are shown in Fig. 17. The topology is able to balance the voltage across capacitors without requiring external control circuit. Fig. 18 shows the waveform of the output voltage, switched capacitors voltage, and load current when the input voltage changed from 100V to 120V. It can be seen that, the achieved output voltage increases base on the gain ($V_O = 3.0V_{dc}$).

The blocking voltage along with current of the switches (S_1, S_2, S_3, S_5, S_7, and S_8) is shown in Fig. 19. It is worth mentioning that the switches in charging loop experience a lower blocking voltage ($V_{s3} = V_{s5} = 2.0V_{dc}$), while the switches ($S_1$, S_2, S_7, and S_8) undergo a blocking voltage three times the input voltage.

Moreover, experimental THD for 7-L output voltage at 50Hz represented in Fig. 20, dead-band effects introduced slight 3rd, 5th, and 7th harmonic components.

V. CONCLUSION

In this paper, seven level SC-MLI topology is presented. The topology employs the switched-capacitor technology for a boosting the output voltage. With just two SC unit, three voltage gains can be achieved. The SCs capable of self-balancing which eliminate the need of external control circuit. A simple SC-SPWM technique to reduce the computation time is developed to generate the gating pulses of power switches. Furthermore, the proposed topology is compared with recent published topologies based on number of component, voltage gain, and efficiency. The ability of the proposed 7-level SC-MLI topology to function with both inductive and resistive loads has been experimentally tested. Finally, an experimental test was performed at 1.0 kW, the topology demonstrated high efficiency 95.3% (and 97.62% @ 300W).

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