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A New Approach to the PWM Modulation for the Multiphase Matrix Converters Supplying Loads with Open-End Winding

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Abstract: This article presents three variants of the Pulse Width Modulation (PWM) for the Double Square Multiphase type Conventional Matrix Converters (DSM-CMC) supplying loads with the open-end winding. The first variant of PWM offers the ability to obtain zero value of the common-mode voltage at the load's terminals and applies only six switches within the modulation period. The second proposal archives for less Total Harmonic Distortion (THD) of the generated load voltage. The third variant of modulation concerns maximizing the voltage transfer ratio, minimizing the number of switching, and the common-mode voltage cancellation. The discussed modulations are based on the concept of sinusoidal voltage quadrature signals, which can be an effective alternative to the classic space-vector approach. In the proposed approach, the geometrical arrangement of basic vectors needed to synthesize output voltages is built from the less number of vectors, which is equal to the number of the matrix converter's terminals. The PWM duty cycle computation is performed using only a second-order determinant of the voltages coordinate matrix without using trigonometric functions. A new approach to the PWM duty cycles computing and the load voltage synthesis by 5 $\times$ 5 and 12 $\times$ 12 topologies has been verified using the PSIM simulation software.

Keywords: square-type matrix converters; pulse width modulation; multiphase systems

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1. Introduction

A fully controlled bidirectional semiconductor switch is an element of the Conventional Matrix Converter (CMC) which offers a direct AC–AC voltages conversion with additional input power factor control functionality. This type of converter, in comparison with the more established Voltage Source Inverter (VSI), has certain individual features that determine the innovation of such a solution [1–3]. It does not contain a bulk dc-link capacitor, thus is far more promising in terms of power density with the inherent four-quadrant operation [4,5]. Compared to traditional variable speed drives with CMC, the multi-phase electric motor drive gives some fundamental advantages. These configurations have grater system redundancy because it can operate during some fault conditions, is characterized by the lower torque ripple and lower per-leg converter rating [6]. Furthermore, the operation of multiphase motors is quieter, allowing for the independent control of two or more series/parallel connected motors [7]. Multiphase electric machines can be fed also by the conventional matrix converter with three inputs [8–11]. The matrix topology is also presented as a unit, which control the power flow between the power generator and the electrical grid [12–16]. Multiphase generators have also been used in systems generating electricity such as offshore installations and wind farms [17,18]. Another application of the multiphase matrix converter in straight forward energy conversion is described in [19], where the 6 $\times$ 6 CMC and multi-winding transformer have been used to supply variable

reactive power flow to the power system. A modulation approach based on the model of the 5×5 matrix converter with fictitious DC-link was shown in conference paper [20].

Multi-phase electric machines, including three-phase and five-phase variants, can be designed as a machine with open stator winding. Such a solution, especially in combination with a CMC, offers some important features. First, the possibility of direct power supply to both ends of the stator phase winding increases the maximum voltage amplitude within the linear range of the PWM modulator [21]. It should be noted here that the output voltage of the CMC cannot exceed the input voltages envelope. A quite frequency discussed problem in drives controlled by power converters, is the common voltage, which can be understood as a voltage measured between the ground potential and a virtually created star point connected with the stator terminals. The common-mode voltage in terminals of AC drives resulting in bearing currents harmful for the motor drive. The use of certain voltage modulation techniques in a matrix converter allows eliminating this problem [5,22–24]. As indicated in the brief introduction multi-phase drives with CMCs are rather niche applications. However, PWM algorithms are the subject of numerous studies, and almost all of the presented algorithms assume ideal sinusoidal input voltage and are designed for machines with the symmetric construction. The application of these methods without consideration of an input voltage asymmetry or the source harmonics in the calculation results in inaccurate load voltage generation. The approach to voltage synthesis proposed in the article takes this aspect into account and allows for the generation of the appropriate load voltage.

Due to a large number of input and output phases, the complexity of PWM algorithms based on the space-vector approach increases significantly. For a single matrix converter with three inputs and three outputs, the number of switch states is 3^3 (27). In the case of five input, five output converter, it gives 5^5 (3125) and analogically in drive with the open-end stator winding, the number of states is equal to 5^{10}. Therefore, the graphical presentation of voltage vectors corresponding to all switch states, at a given moment of time, becomes very unreadable, which makes it problematic to design and elaborate the dedicated PWM algorithms. The works [3,25] show that the synthesis of output voltages in multi-phase systems can be successfully simplified. These methods can be classified to the direct method of modulation. Compared to the transformation proposed by Clarke, the use of the Hilbert transform leads to the reduction of the number of required vectors. Therefore, for the CMC 5×5 the PWM algorithm can be developed using only 10 vectors. Apart from the modulation methods based on the space-vector approach, a group of methods of direct modulation can be indicated, such as the Venturini solution [1,26,27], while the general Venturini formulas for PWM duty cycles for several multi-phase converters, including square-type matrix converters are presented in [28]. The work in [25] proposes Wachspress formulas, which can be theoretically applied for any number of inputs. The use of either the Venturini solution or the Wachspress functions forces the commutation all switches of the given output cell (shown in the drawing later in the article). This can be explained by the fact that the switch modulating function is continuous, thus results in higher switching losses. All the PWM modulation methods discussed in the article are characterized by a lower number of switching cycles of at most 6 during the modulation period.

The paper is organized as follows. Definitions and principles of the proposed an output voltage synthesis using the DSM-CMC converter are presented in Section 2. This section also presents the method of generating quadrature signals using the Discrete Second-Order Generalized Integrator (DSOGI) structure. Then, the next three sections demonstrate variants of the proposed modulation. Abilities of the input displacement angle control have been also discussed. Results are summarized and discussed in the conclusion section. Due to a huge number of switching elements, the realization of the experimental setup is very expensive. Therefore, the conclusions presented in the article are the result of circuit simulation in PSIM11 software and analytical research only. However, the proposed solution has been verified partially by an experiment and published in [3,25,29].

2. The Principle of an Output Voltage Synthesis in DSM-CMC Converter

The DSM-CMC converter consists of two square-type matrix converters, CMC_P and CMC_N, connected to load terminals as shown in Figure 1, where the simplified diagram of the circuit is depicted. If the number of load phases is equal to n, the total number of bidirectional power electronic switches is equal to $2n^2$. Both converter are connected with the n-phase AC voltage source v_{i1}, v_{i2}, ..., and v_{in}. The voltage of the phase x of the load

$$v_{ox}(t) = v_{Px}(t) - v_{Nx}(t) \tag{1}$$

measured at the load terminals, are synthesized by these converters by using the switch group h_{11}, h_{21}, ..., h_{n1}.

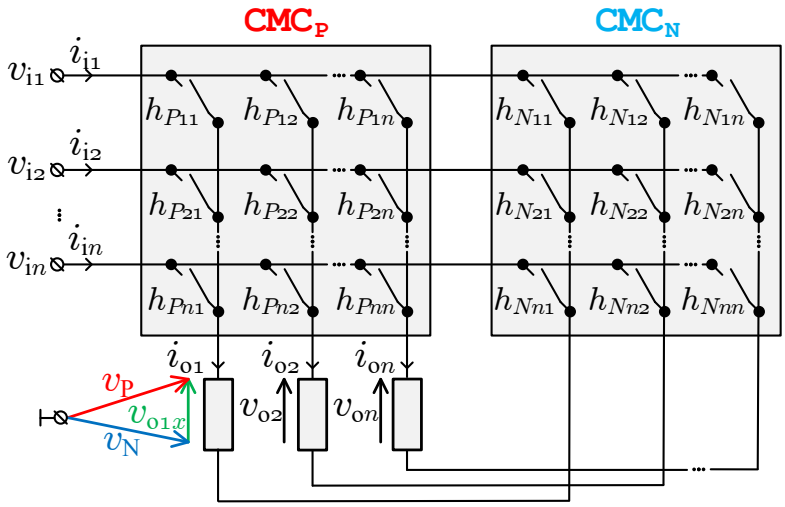


Figure 1. Simplified diagram of the square-type double conventional matrix converter.

As can be seen in Figure 2, switches on both sides of one phase of the load make the single commutation cell with two voltage multiplexers, s_P and s_N, respectively.

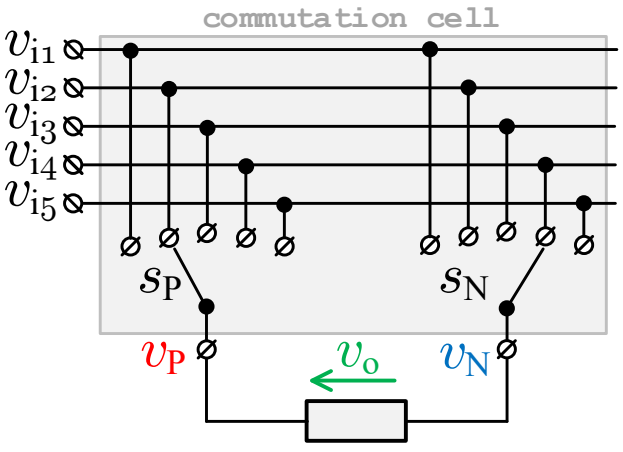


Figure 2. The single commutation cell for DSM-CMC 5 × 5.

2.1. Case of 5 Phases

The number of multiplexer switches is equal to the number of input voltages, and in this case, takes 5. For a better understanding of the proposal, let the further consideration will be focused on 5 × 5 topology.

According to the proposed concept of the voltage synthesis described in [3], all input voltages with pulsation ω_i can be represented as a collection of five rotating vectors:

$$\mathbf{v_i} = \begin{bmatrix} v_{i1x} & v_{i1y} \\ v_{i2x} & v_{i2y} \\ v_{i3x} & v_{i3y} \\ v_{i4x} & v_{i4y} \\ v_{i5x} & v_{i5y} \end{bmatrix} \tag{2}$$

with the real

$$\begin{aligned} v_{i1x} &= V_{i1} \cdot \cos(\omega_i t) \\ v_{i2x} &= V_{i2} \cdot \cos(\omega_i t - 2\pi/5) \\ v_{i3x} &= V_{i3} \cdot \cos(\omega_i t - 4\pi/5) \\ v_{i4x} &= V_{i4} \cdot \cos(\omega_i t - 6\pi/5) \\ v_{i5x} &= V_{i5} \cdot \cos(\omega_i t - 8\pi/5) \end{aligned} \tag{3}$$

and the imaginary parts of coordinates

$$\begin{aligned} v_{i1y} &= V_{i1} \cdot \sin(\omega_i t) \\ v_{i2y} &= V_{i2} \cdot \sin(\omega_i t - 2\pi/5) \\ v_{i3y} &= V_{i3} \cdot \sin(\omega_i t - 4\pi/5) \\ v_{i4y} &= V_{i4} \cdot \sin(\omega_i t - 6\pi/5) \\ v_{i5y} &= V_{i5} \cdot \sin(\omega_i t - 8\pi/5) \end{aligned} \tag{4}$$

where V_{i1}, ..., V_{i5} are the amplitudes of these voltages. Due to the analytic signal concept based on the Hilbert transform, for the pure sinusoidal input waveforms, the imaginary coordinates are just quadrature components and an input voltage vectors collection can be presented as shown in Figure 3 as the symmetric system.

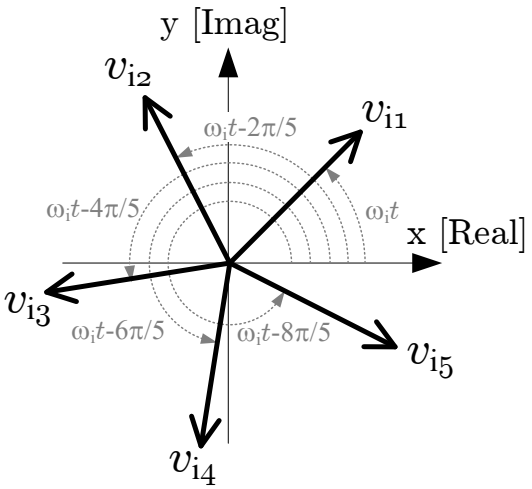


Figure 3. The collection of five the rotating input vectors.

These coordinates can be determined using the Hilbert filter or obtained through FFT/DFT based operation [30–32]. However, the Hilbert filter and algorithms based on DFT, although are quite accurate, are not the simple solution from code developing point of view. Moreover, error signals in the form of DC offsets, glitches, and momentary voltage sags may occur in measurements. Therefore, the input vector coordinates can be calculated in a different manner. A compromise solution, between accuracy and not complicated solution, maybe the use of the Double Second-Order Generalized Integrator with loop feedback extension functioned as Orthogonal Signal Generator (DSOGI-OSG), which in the

OSG part prevents unexpected resonance and variables overflow. DSOGI-OSG structure in continuous time-domain is presented in Figure 4.

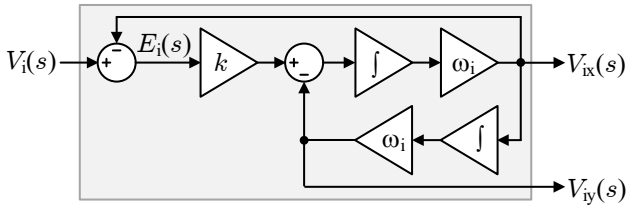


Figure 4. Double Second-Order Generalized Integrator with loop feedback extension functioned as Orthogonal Signal Generator (DSOGI-OSG) structure in continuous time-domain [33–35]: V_i—the input sinusoidal signal, V_{ix}—in-phase component of the input signal, V_{iy}—the quadrature component of the input signal, E_i the error signal, k—the gain block, ω_i—reference pulsation of the input signal, and $\int$ is an integrator block.

The transfer function takes the form of (5) for in-phase output and (6) for orthogonal output, while (7) represents the notch filter equation

$$\frac{V_{ix}(s)}{V_i(s)} = \frac{k \cdot \omega_i \cdot s}{s^2 + k \cdot \omega_i \cdot s + {\omega_i}^2} \tag{5}$$

$$\frac{V_{iy}(s)}{V_i(s)} = \frac{k \cdot \omega_i^2}{s^2 + k \cdot \omega_i \cdot s + {\omega_i}^2} \tag{6}$$

$$\frac{E_i(s)}{V_i(s)} = \frac{s^2 + {\omega_i}^2}{s^2 + k \cdot \omega_i \cdot s + {\omega_i}^2} \tag{7}$$

where the parameter k is a value less than unity (k is taken the value of $1/\sqrt{2}$ here), $E_i(s)$ is the error signal, while ω_i is an input voltage nominal pulsation. If processed signal frequency does not have an exact value, another extension of SOGI structure, called Frequency-Locked Loop (FLL), may be applied [36–38].

The load voltage v_o produced by the single commutation cell, shown in Figure 2, can be analogous represented by two rotating vectors, v_P and v_N, as is depicted in Figure 5. Only the geometrical distance of real (indicated by subscript x) coordinates of these vectors produce the load voltage. While the imaginary coordinate (indicated by subscript y) can generate the reactive power flow at the converter input. In general, there exists some degree of freedom for selecting the instantaneous value of this component because it does not influence on the load currents. The article is focused on the cases, which locus of each output vector is straight a circle. This means that a rotating output voltage vector moves along a circular trajectory and this movement can be clockwise or counterclockwise. Four variants of the PWM modulation scheme are shown in Figure 5.

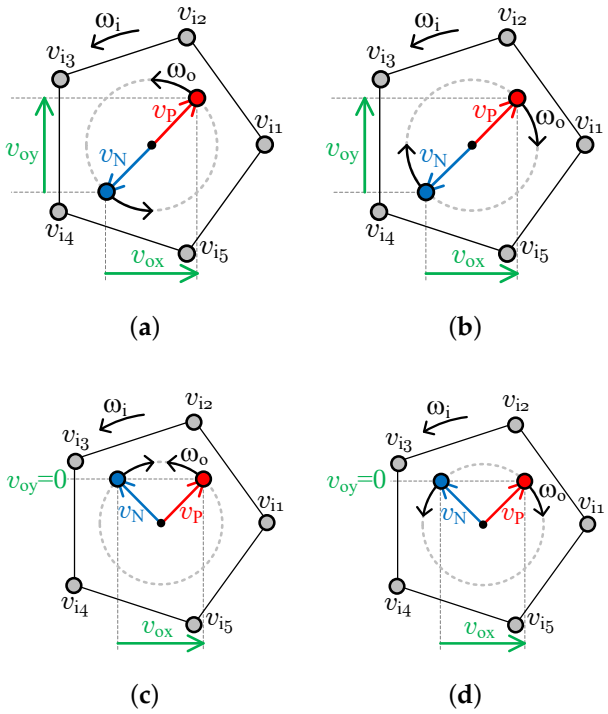


Figure 5. Four variants of output vectors rotation: (**a**) CCV-CCV, (**b**) CV-CV, (**c**) CCV-CV, and (**d**) CV-CCV.

A vector arrangement in Figure 6a, for the given commutation cell, can be presented as the rotating polygon as illustrated in Figure 6b. The polygon surface is named here as the output voltage synthesis field. All the points, which represent output voltage vectors, have to be located inside the synthesis field. Such a geometric arrangement allows for direct application the Wachspress function for the PWM duty cycles calculation [25,28]. However, the number of switching within the modulation period should be minimal, and for this reason, Venturini and Wachpress solution is not suitable. Decreasing the number of switching can be realized by applying the Nearest Three Vectors (NTV) modulation technique, which relays on the selection of a proper triangle in the synthesis field. Figure 6c shows two selected triangles for the voltages generated by CMC_P and CMC_N converters. Note that both points, representing these voltages, are located in their triangular local synthesis fields. This is the required condition of output voltage synthesizability. The selection of the optimal triangle may consist in finding the appropriate vertex of the synthesis field, which clearly indicates the input vector closest to the output vector. In the case of using NTV technique, this solution is sufficient, because the other two required vectors are adjacent to the selected one. As can be seen, vector v_P is closest to the vertex number 2, while vector v_N is closest to vertex 4. All six required PWM duty cycles can be calculated using the smooth interpolation technique, which is, in the discussed case, nothing more than an appropriate triangle area relation for the NTV modulation [3]. An area of the triangle can be computed using the second-order matrix determinant. Thus, an application of that solution only needs coordinates of the triangle vertices. As mentioned earlier, these coordinates can be computed using the DSOGI-OSG block shown in Figure 4.

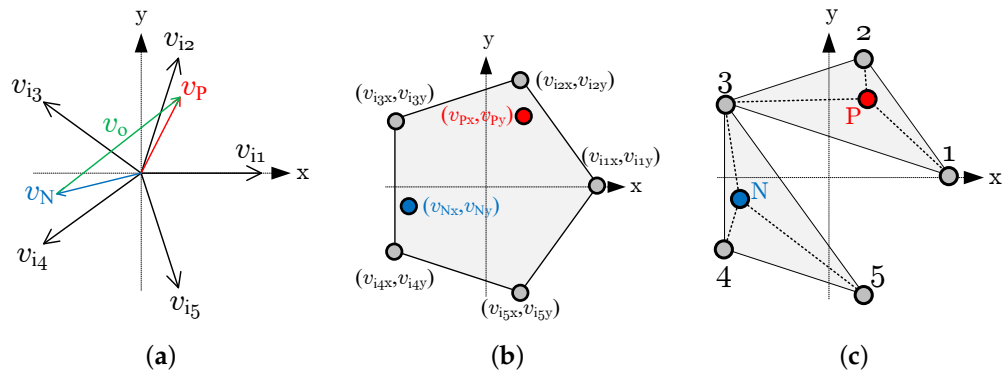


Figure 6. The principle of operation: (**a**) vectors arrangement, (**b**) synthesis field, and (**c**) selected triangles.

2.2. Case of 12 Phases

In the case of more input voltages, for example, when the number of inputs is equal to 12, the choice of the optimal triangle is not so obvious. Now, let us consider the graphical vector arrangements for 12 × 12 topology expressed as regular polygon shown in Figure 7a.

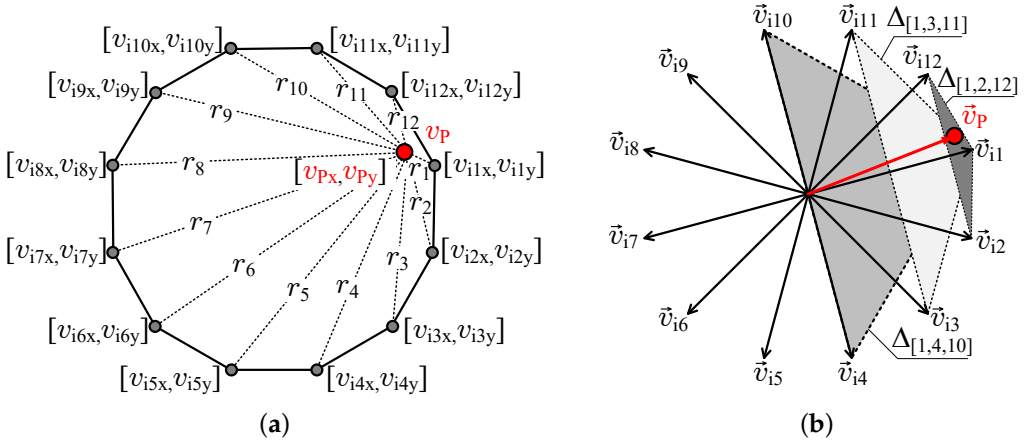


Figure 7. Synthesis field of the 12 × 12 matrix topology (**a**), the input voltage vectors, and an example reference output voltage $\vec{v}_{o1}$ (**b**).

One of 12 presented input vectors is referred here as the base vector. It means that the distance—defined as $r_1 \cdots r_{12}$ and shown in Figure 7b—between this vector and the reference vector $\vec{v}_{o1}$ is the smallest. There are three triangles with a common upper vertex with coordinates $\{v_{i1x}, v_{i1y}\}$: $\Delta_{[2,1,12]}$, $\Delta_{[3,1,11]}$, and $\Delta_{[4,1,10]}$. A vector $\vec{v}_{i1}$ is the base vector in this case. The given triangle $\Delta_{[p,q,r]}$ satisfies the modulation conditions when the sum

$$\Sigma_{[p,q,r]} = d_p + d_q + d_r \tag{8}$$

where

$$\begin{bmatrix} d_p \\ d_q \\ d_r \end{bmatrix} = \xi \begin{bmatrix} \left| \det \begin{bmatrix} v_{qx} - v_{o1x} & v_{qy} - v_{o1y} \\ v_{rx} - v_{o1x} & v_{ry} - v_{o1y} \end{bmatrix} \right| \\ \left| \det \begin{bmatrix} v_{px} - v_{o1x} & v_{py} - v_{o1y} \\ v_{rx} - v_{o1x} & v_{ry} - v_{o1y} \end{bmatrix} \right| \\ \left| \det \begin{bmatrix} v_{qx} - v_{o1x} & v_{qy} - v_{o1y} \\ v_{px} - v_{o1x} & v_{py} - v_{o1y} \end{bmatrix} \right| \end{bmatrix} \tag{9}$$

and

$$\xi = \left| \det \begin{bmatrix} v_{px} - v_{qx} & v_{py} - v_{qy} \\ v_{rx} - v_{qx} & v_{ry} - v_{qy} \end{bmatrix} \right|^{-1} \tag{10}$$

of PWM duty cycles d_{p}, d_{q}, and d_{r} takes the smallest value, ideally equal unity. When two or more triangles meet this condition, the triangle with the smallest area should be selected for further consideration. In practice, this operation can be performed by using optimized DSP functions like qsort (sorting in required order), vecmin (finding the minimum value within the set), or standard conditional operators.

When the value of transfer voltage ratio $q = V_{\mathrm{o}}/V_{\mathrm{i}}$ of the 12×12 topology, e.g., for $\mathrm{CMC_P}$ or $\mathrm{CMC_N}$, is in the range

$$\frac{\cos\left(\frac{\pi}{6}\right)}{\cos\left(\frac{\pi}{12}\right)} \leq q \leq \cos\left(\frac{\pi}{12}\right) \tag{11}$$

a large number of output phases allows generating the output voltage with lower THD, therefore the cost of passive elements can be decreasing. Corresponding simulation results are presented in the further part of the text. PWM duty cycles calculation for $\mathrm{CMC_P}$ and $\mathrm{CMC_N}$ are explained in two separate subsections. While the two concepts of gating signals generation have been presented in the third subsection.

2.3. PWM Duty Cycles Calculation for CMC_P and Topology 5×5

Referred to the triangle $\Delta_{[1,2,3]}$ in Figure 6, the reference output voltage v_{P} is synthesized using 3 switches: h_{11}, h_{21}, and h_{31}. Taking into account previous considerations, the following formulas can be proposed for the calculation of PWM duty cycles,

$$d_{1\mathrm{P}} = \xi_{\mathrm{P}} \cdot \left| \det \begin{bmatrix} v_{\mathrm{i2x}} - v_{\mathrm{Px}} & v_{\mathrm{i2y}} - v_{\mathrm{Py}} \\ v_{\mathrm{i3x}} - v_{\mathrm{Px}} & v_{\mathrm{i3y}} - v_{\mathrm{Py}} \end{bmatrix} \right| = \frac{\Delta_{[2,\mathrm{P},3]}}{\Delta_{[1,2,3]}} \tag{12}$$

$$d_{3\mathrm{P}} = \xi_{\mathrm{P}} \cdot \left| \det \begin{bmatrix} v_{\mathrm{i1x}} - v_{\mathrm{Px}} & v_{\mathrm{i1y}} - v_{\mathrm{Py}} \\ v_{\mathrm{i2x}} - v_{\mathrm{Px}} & v_{\mathrm{i2y}} - v_{\mathrm{Py}} \end{bmatrix} \right| = \frac{\Delta_{[2,\mathrm{P},1]}}{\Delta_{[1,2,3]}} \tag{13}$$

$$d_{2\mathrm{P}} = 1 - d_{1\mathrm{P}} - d_{3\mathrm{P}} = \frac{\Delta_{[3,\mathrm{P},1]}}{\Delta_{[1,2,3]}} \tag{14}$$

where det is the determinant of the second-order matrix, and

$$\xi_{\mathrm{P}} = \left| \det \begin{bmatrix} v_{\mathrm{i2x}} - v_{\mathrm{i1x}} & v_{\mathrm{i2y}} - v_{\mathrm{i1y}} \\ v_{\mathrm{i3x}} - v_{\mathrm{i1x}} & v_{\mathrm{i3y}} - v_{\mathrm{i1y}} \end{bmatrix} \right|^{-1} \tag{15}$$

is the scaling factor, which is equal to the triangle $\Delta_{[1,2,3]}$ surface. Thus, the average value of the $\mathrm{CMC_P}$ output voltage can be expressed by the following formula.

$$\overline{v}_{\mathrm{P}} = d_{1\mathrm{P}} \cdot v_{\mathrm{i1}} + d_{2\mathrm{P}} \cdot v_{\mathrm{i2}} + d_{3\mathrm{P}} \cdot v_{\mathrm{i3}} \tag{16}$$

2.4. PWM Duty Cycles Calculation for CMC_N and Topology 5×5

Referred to the triangle $\Delta_{[3,4,5]}$ in Figure 6, the reference output voltage v_{N} is synthesized by 3 switches: h_{31}, h_{41}, and h_{51}. The corresponded duty cycles can be calculate using the following formulas,

$$d_{3\mathrm{N}} = \xi_{\mathrm{N}} \cdot \left| \det \begin{bmatrix} v_{\mathrm{i4x}} - v_{\mathrm{Nx}} & v_{\mathrm{i4y}} - v_{\mathrm{Ny}} \\ v_{\mathrm{i5x}} - v_{\mathrm{Nx}} & v_{\mathrm{i5y}} - v_{\mathrm{Ny}} \end{bmatrix} \right| = \frac{\Delta_{[4,\mathrm{N},5]}}{\Delta_{[3,4,5]}} \tag{17}$$

$$d_{4\mathrm{N}} = \xi_{\mathrm{N}} \cdot \left| \det \begin{bmatrix} v_{\mathrm{i5x}} - v_{\mathrm{Nx}} & v_{\mathrm{i5y}} - v_{\mathrm{Ny}} \\ v_{\mathrm{i3x}} - v_{\mathrm{Nx}} & v_{\mathrm{i3y}} - v_{\mathrm{Ny}} \end{bmatrix} \right| = \frac{\Delta_{[5,\mathrm{N},3]}}{\Delta_{[3,4,5]}} \tag{18}$$

$$d_{5\mathrm{N}} = 1 - d_{3\mathrm{N}} - d_{4\mathrm{N}} = \frac{\Delta_{[3,\mathrm{N},4]}}{\Delta_{[3,4,5]}} \tag{19}$$

where

$$\xi_{\mathrm{N}} = \left| \det \begin{bmatrix} v_{\mathrm{i4x}} - v_{\mathrm{i3x}} & v_{\mathrm{i4y}} - v_{\mathrm{i3y}} \\ v_{\mathrm{i5x}} - v_{\mathrm{i3x}} & v_{\mathrm{i5y}} - v_{\mathrm{i3y}} \end{bmatrix} \right|^{-1} \tag{20}$$

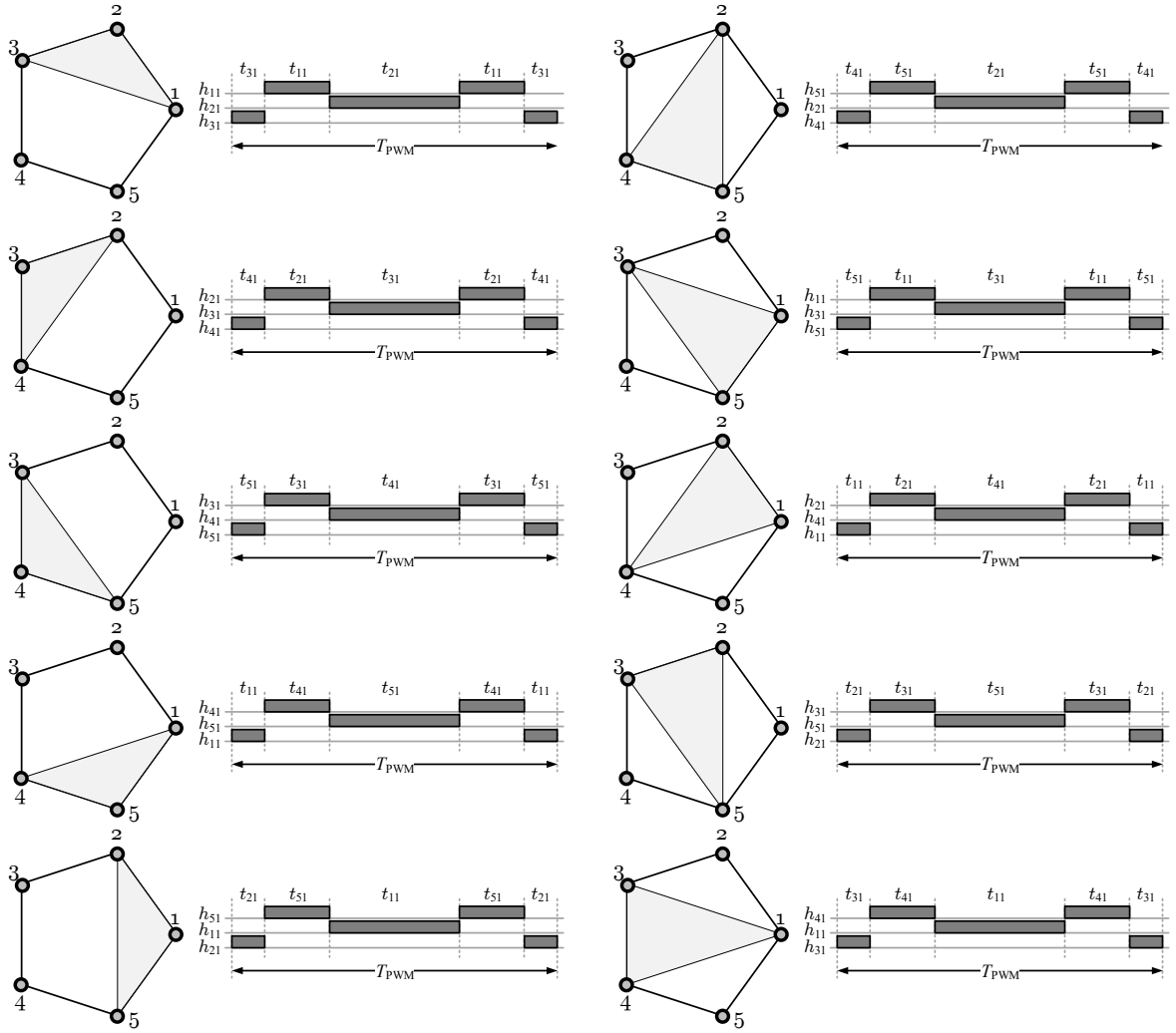
is the scaling factor, which is equal to the triangle $\Delta_{[3,4,5]}$ surface. The average value of the $\mathrm{CMC_N}$ output voltage can be expressed by the following formula

$$\overline{v}_{\mathrm{N}} = d_{3\mathrm{N}} \cdot v_{\mathrm{i3}} + d_{4\mathrm{N}} \cdot v_{\mathrm{i4}} + d_{5\mathrm{N}} \cdot v_{\mathrm{i5}} \tag{21}$$

2.5. The Concept of Gating Signals Generation

The gate signals can be controlled according to different strategies. Apap et al. [39] compared and presented several PWM signal gating methods. Among them, the cyclic Venturini and Min-Mid-Max (MMM) schemes of modulation are proposed. Two approaches have been applied to the gates signal generation: basic and mentioned MMM scheme.

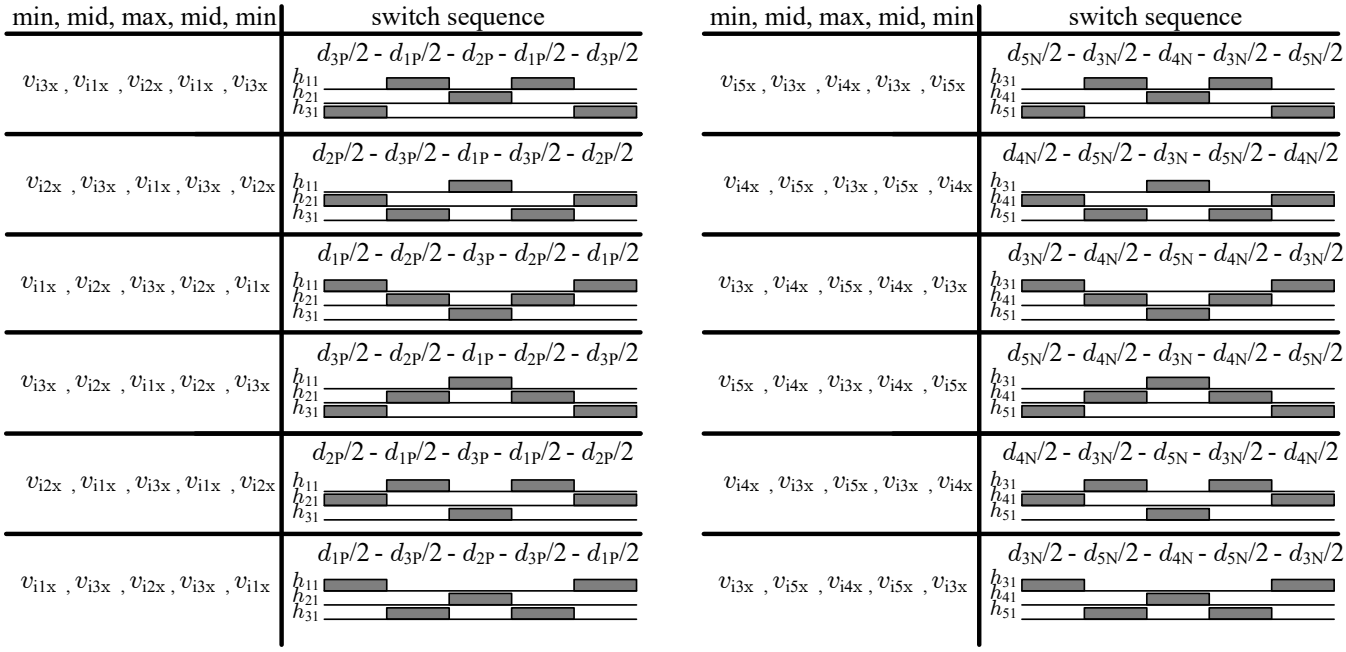
In the case of the basic solution, the sequences of the switch states always depend on the selected triangle in which the synthesis of the output voltage is realized. Therefore, these sequences can be placed in a lookup table. An overview of the basic sequences is shown in Figure 8, where the value of $\varphi \simeq 1.618$, which is so-called the golden ratio exists in the pentagon.



(**a**) sequences type I for $q \in \langle 1/(1+\varphi), \cos(\pi/5) \rangle$ (**b**) sequences type II for $q \in (0, 1/(1+\varphi))$

Figure 8. The switch state sequences in the basic solution of the gating signals for both converter cells CMC_{P} and CMC_{N}.

The MMM method is used to improve the quality of the voltage generated by the converter in terms of THD. The switch states sequences for the CMC_P and CMC_N converters are characterized in Figure 9. Note that these sequences correspond to the case illustrated in Figure 6b.



(**a**) for CMC_P converter (**b**) for CMC_N converter

Figure 9. The MMM type of sequences of the gating signals for both converter cells CMC_P and CMC_N for the case depicted in Figure 6c.

3. The PWM Variant 1—An Output Voltage Synthesis with Zero Value of the Common-Mode Voltage

The common-mode voltage, defined as

$$v_{cm}(t) = (v_{o1}(t) + v_{o2}(t) + v_{o3}(t) + v_{o4}(t) + v_{o5}(t))/5, \tag{22}$$

can lead to the degradation of rolling bearings in electric machines powered by PWM inverters. As indicated in the introduction an open-end windings stator fed by the double matrix converter allows for the PWM modulation without the common-mode voltage generation. The proposed approach to the load voltage synthesis with conjunction with the basic solution of the gating signals control (shown in Figure 8) give the same desired result. Elimination of the common-mode voltage can be performed by all four PWM modulation schemes: CV-CV, CCV-CCV, CV-CCV, and CCV-CV. The use of the first two cases allows obtaining an input displacement angle, which is dependent on the load parameters like in the Venturini methods [1,26].

The referenced *k*-output voltage vectors of the CCV-CCV modulation scheme can be expressed by following equations.

$$v_{Pxk} = q \cdot \cos(\omega_o \cdot t - ((k-1) \cdot 2\pi/5)) \tag{23}$$

$$v_{Pyk} = -q \cdot \sin(\omega_o \cdot t - ((k-1) \cdot 2\pi/5)) \tag{24}$$

$$v_{Nxk} = -q \cdot \cos(\omega_o \cdot t - ((k-1) \cdot 2\pi/5)) \tag{25}$$

$$v_{Nyk} = q \cdot \sin(\omega_o \cdot t - ((k-1) \cdot 2\pi/5)) \tag{26}$$

Above equation are proposed for the first commutation cell. Equations for the rest of the rotating vectors pairs can be represented by analogous elaboration. The referenced output voltages in CV-CV scheme can be represented by following equations.

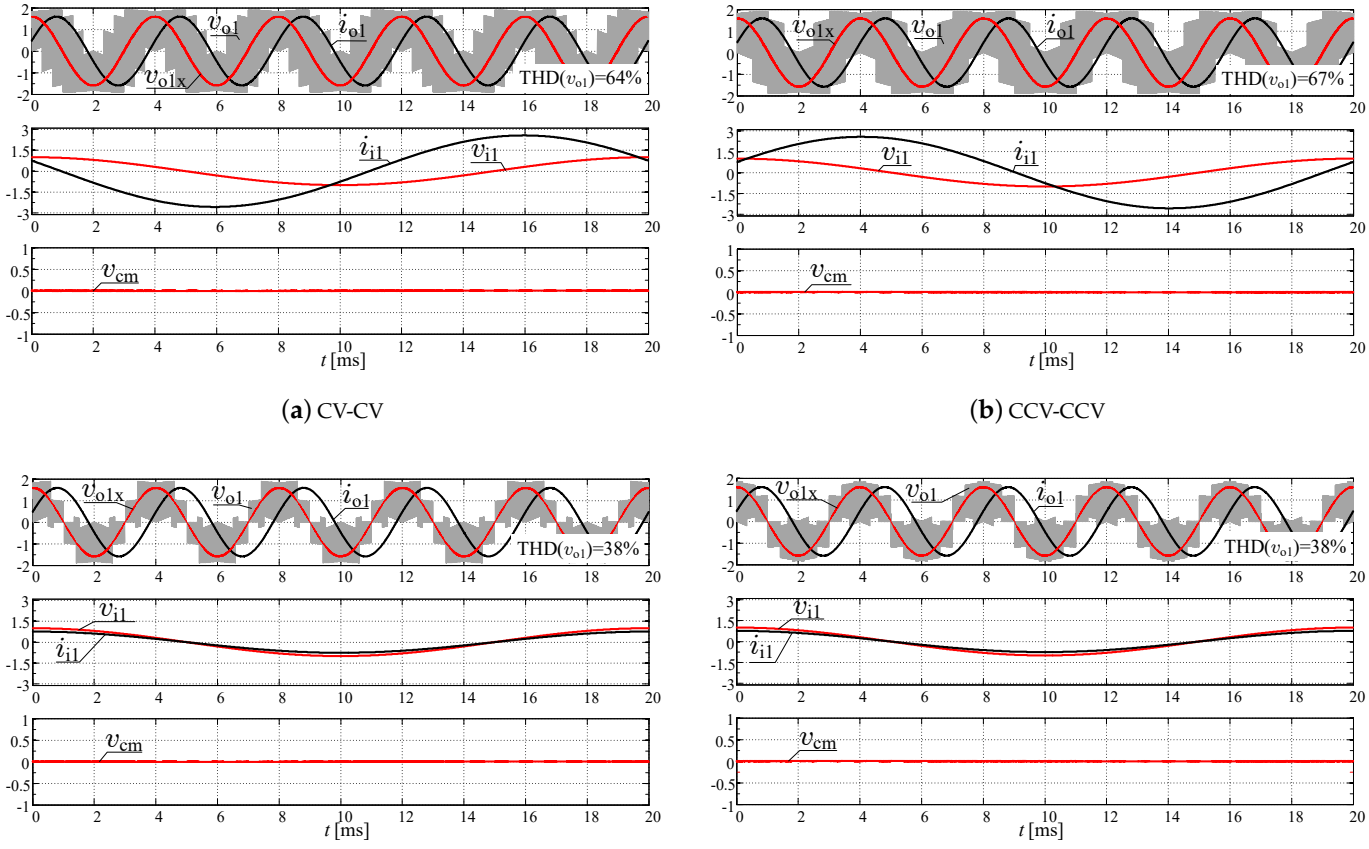
$$v_{\mathrm{P}xk} = q \cdot \cos(\omega_{\mathrm{o}} \cdot t - ((k-1) \cdot 2\pi/5)) \tag{27}$$

$$v_{\mathrm{P}yk} = q \cdot \sin(\omega_{\mathrm{o}} \cdot t - ((k-1) \cdot 2\pi/5)) \tag{28}$$

$$v_{\mathrm{N}xk} = -q \cdot \cos(\omega_{\mathrm{o}} \cdot t - ((k-1) \cdot 2\pi/5)) \tag{29}$$

$$v_{\mathrm{N}yk} = -q \cdot \sin(\omega_{\mathrm{o}} \cdot t - ((k-1) \cdot 2\pi/5)) \tag{30}$$

The possibility to change the rotation of the given output vector by changing the sign of the imaginary component allows realizing the PWM modulation, in which the resultant imaginary component of the $v_{\mathrm{o}y}$ takes the zero value. If vectors $\vec{v}_{\mathrm{P}}$ and $\vec{v}_{\mathrm{N}}$ rotate in opposite directions, as is typical for last two presented schemes of modulation CV-CCV and CCV-CV, the passive input current component is not generated. Simulation results of the PWM variant 1 for DSM-CMC5 × 5 and four modulation schemes are shown in Figure 10. Simulation parameters are listed in Table A1, which can be found in an appendix.



(**a**) CV-CV

(**b**) CCV-CCV

(**c**) CV-CCV

(**d**) CCV-CV

Figure 10. Simulation of the PWM variant 1 for DSM-CMC5 × 5 and four modulation schemes—RL load case.

Analogous simulation tests have been realized for the proposed converter connected to a 12-phase symmetrical power supply. Figure 11 shows the load voltage generated by DSM-CMC12 × 12 for an output frequency equal to 10 Hz, while results obtained for 300 Hz are presented in Figure 12.

Simulation parameters for this case are available in Table A2 in Appendix A. The selection of different sets of simulation parameters did not subserve a specific purpose.

The simulation tests were carried out with the use of two independent simulation files. However, in the case of the DSM-CMC12 $\times$ 12 simulation, a small calculation step was chosen due to the high modulation frequency. It was set to 100 kHz to get a good PWM resolution at 300 Hz of the fundamental frequency.

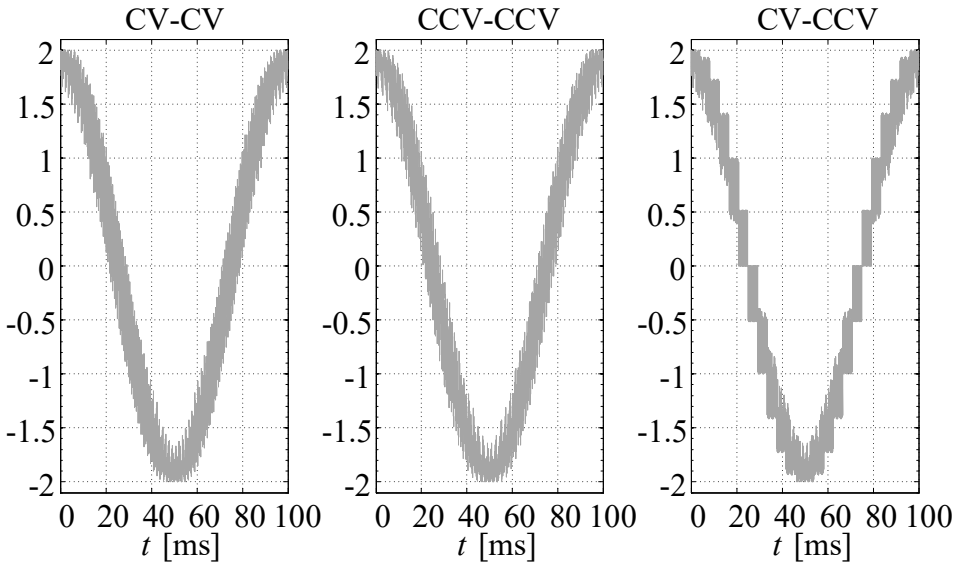


Figure 11. The load voltage v_o for DSM-CMC12 $\times$ 12 converter for the three selected modulation schemes: $f_o = 10$ Hz, $q = 2 \times 0.95$.

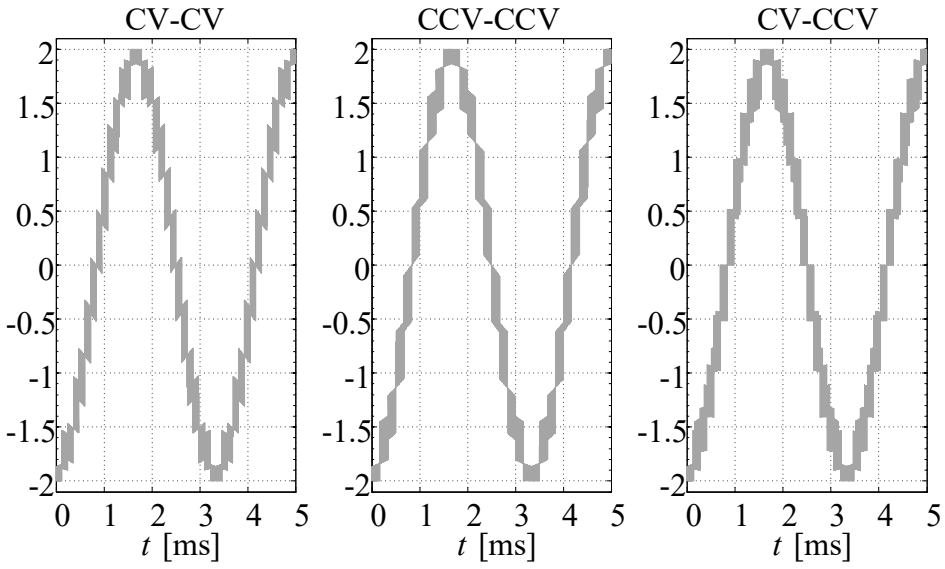


Figure 12. The load voltage v_o for DSM-CMC12 $\times$ 12 converter for the three selected modulation schemes: $f_o = 300$ Hz, $q = 2 \times 0.95$.

Properties of this type of matrix converter, compared with counterpart 5 $\times$ 5, remains the same. In particular, the common-mode voltage is also eliminated by using the basic type of switches state sequences. The voltages shown in these figures are characterized by a low THD, which is about 12%. Comparing to the 5 $\times$ 5 topology, the resulted voltage gain for DSM-CMC is higher and takes optimally the value of 1.93.

4. The PWM Variant 2—An Output Voltage Synthesis with Less Harmonic Distortion

The basic solution of the switch states sequence has been applied in the PWM modulation with eliminating the common-mode voltage. If a lower THD of the load voltage

waveform is desired, a more advanced gating signal generation mechanism can be proposed, such as MMM scheme shown in Figure 9. With regard to variant 1, this is the only change. However, the MMM method is more complicated because the input voltage vector collection should be arranged in a specific order $\{min - mid - max - mid - min\}$ within the selected triangular synthesis field. Simulation results are presented in Figure 13. A lower THD of the load voltage v_o is obtained but the common-mode voltage v_{cm} is also generated, as marked in the presented drawings.

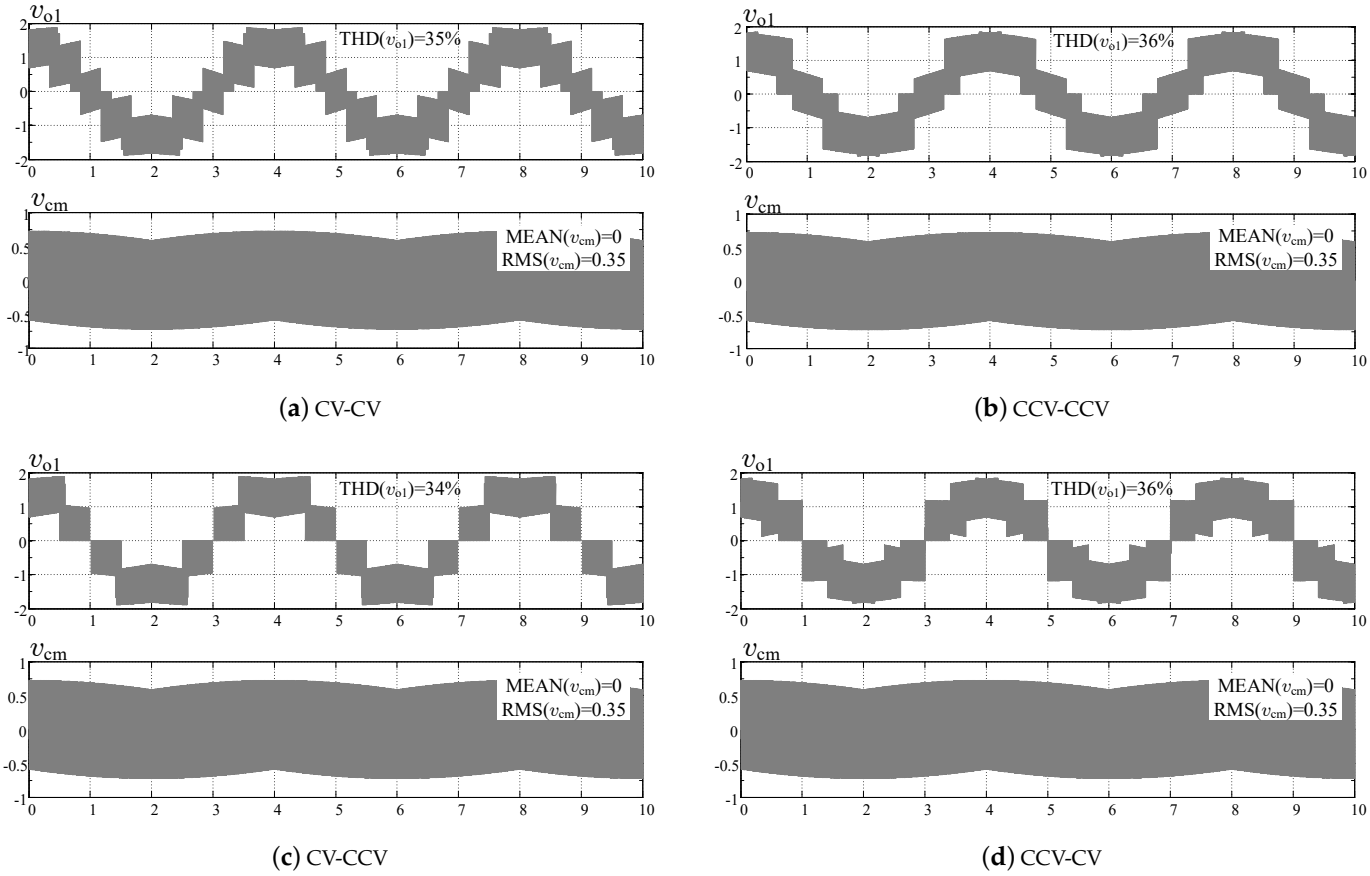


Figure 13. Simulation of the PWM variant 2 for DSM-CMC5 $\times$ 5 and four modulation schemes: $f_o = 250$ Hz, $q = 2 \times 0.8$.

5. The PWM Variant 3—An Output Voltage Synthesis with Maximum Voltage Transfer Ratio and Minimum Number of Switching

A synthesis field for multi-phase and symmetrical AC voltage sources can be represented by a regular polygon as shown in Figure 6 (middle) and Figure 7 (left). A radius of a circle inscribed of this polygon limits an output voltage amplitude in the linear range of modulation. The maximum voltage transfer ratio for CMC_N and CMC_P, related to the input voltage amplitude and number of inputs equal to n, can be expressed as follows,

$$q_{P\,max} = q_{N\,max} = \cos(\pi/n) \tag{31}$$

Therefore, the maximum load voltage for DSM-CMC5 $\times$ 5 in $p.u.$ is equal to

$$v_{o\,max} = 2 \cdot \cos(\pi/5) = 1.618 \tag{32}$$

The value (32) can be increased by modifying the position of the v_P and v_N vectors. In contrast to the methods described in the previous sections, trajectories of these vectors are not a circle. The locus of each vector is not changing smoothly and contains discontinuities. This type of modulation belongs to the discontinuous group of PWM modulations. Both

reference vectors v_P and v_N take exactly five positions, in which they lie on one of five input vectors. An algorithm flowchart for DSM-CMC5 × 5 is presented in Figure 14.

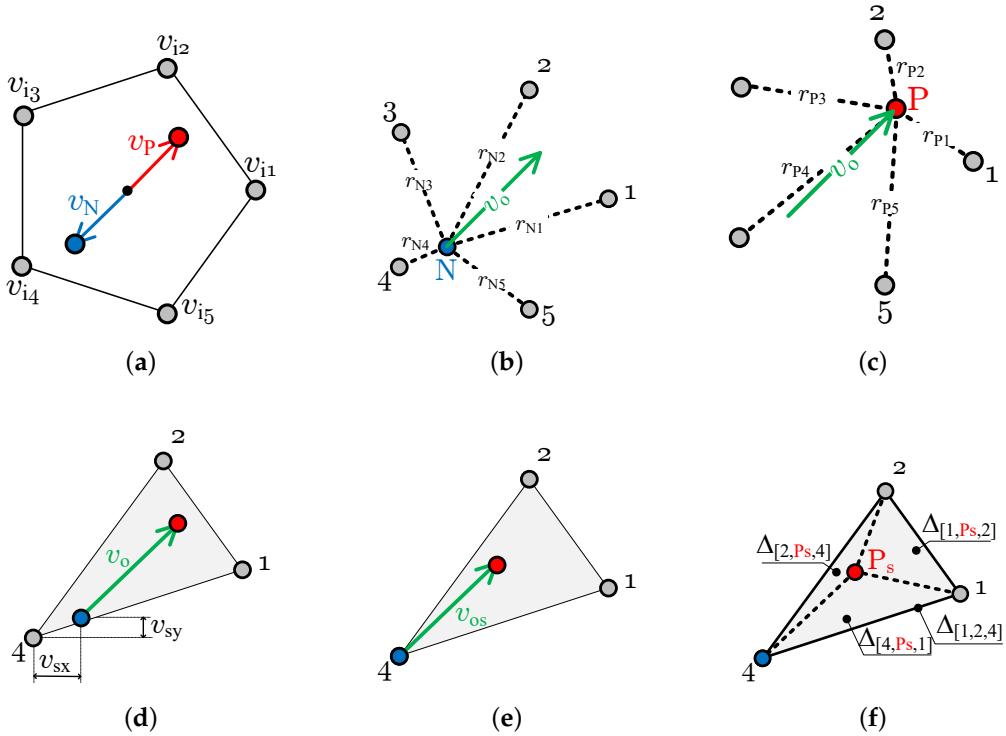


Figure 14. An algorithm flowchart of the variant 3 PWM modulation: (**a**) Step 1: generation of synthesis field and reference voltage vectors v_P and v_N. (**b**) Step 2: calculation of the set of distances between the N point and vertices of the synthesis field. (**c**) Step 3: calculation of the set of distances between the P point and vertices of the synthesis field. (**d**) Step 4: shortest distance selection, setting the origin vertex, and the vector's offset $\{v_{sx}, v_{sy}\}$ calculation. (**e**) Step 5: the reference vector v_o shift resulting in the new coordinates of *P* and *N* points. (**f**) Step 6: calculation of four areas of the triangle and PWM duty cycles.

The output voltage synthesis field is generated using the DSOGI blocks at the first step of the proposed algorithm. The reference output voltage vectors coordinates, $\{v_{Nx}, v_{Ny}\}$ and $\{v_{Px}, v_{Py}\}$, are also calculated at this step. The vectors can rotate clockwise (CV-CV scheme) or counterclockwise (CCV-CCV scheme), as shown in Figure 15.

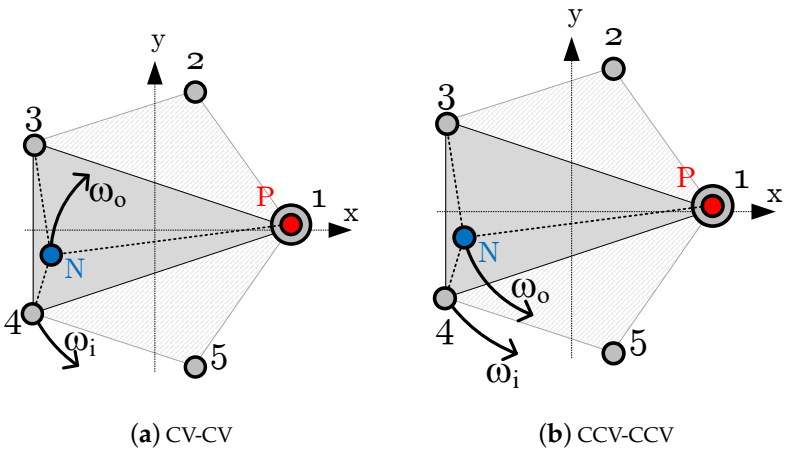


Figure 15. An example rotation of the reference output vector.

Based on the analysis of the vector arrangement in Figure 15, it can be written that the maximum length of the voltage vector, in a linear range of modulation, is equal to the following expression.

$$v_{\mathrm{o\,max\,(variant3)}} = 1 + \cos(\pi/5) = 1.809 \tag{33}$$

However, a vector of this length has to be accordingly shifted inside the synthesis field as shown in Figure 14d–e. Therefore, new coordinates of the reference output vector for the given commutation cell can be calculated as follows.

$$v_{\mathrm{osx}} = v_{\mathrm{ox}} + v_{\mathrm{sx}} \tag{34}$$

$$v_{\mathrm{osy}} = v_{\mathrm{oy}} + v_{\mathrm{sy}} \tag{35}$$

Distances between N-point and all the synthesis field vertices are calculated in Step 2. The same procedure is applied for the point P in Step 3. Next, the shortest calculated distance in a N-collection $\{r_{\mathrm{N1}}, r_{\mathrm{N2}}, r_{\mathrm{N3}}, r_{\mathrm{N4}}, r_{\mathrm{N5}}\}$ is compared with the shortest calculated distance in a P-collection $\{r_{\mathrm{P1}}, r_{\mathrm{P2}}, r_{\mathrm{P3}}, r_{\mathrm{P4}}, r_{\mathrm{P5}}\}$. Finally, the less value is selected, which correctly indicates the optimal vertex of the synthesis field. The shift coordinates are calculated in Step 4. As can be seen in Figure 14d, vertex number 4 has been chosen. Thus, the PWM duty cycles, for the case illustrated in Figure 14f can be calculated using the following formulas.

$$d_{\mathrm{1Ps}} = \Delta_{[2,\mathrm{Ps},4]}/\Delta_{[1,2,4]} \tag{36}$$

$$d_{\mathrm{2Ps}} = \Delta_{[4,\mathrm{Ps},1]}/\Delta_{[1,2,4]} \tag{37}$$

$$d_{\mathrm{4Ps}} = \Delta_{[1,\mathrm{Ps},2]}/\Delta_{[1,2,4]} \tag{38}$$

and

$$d_{\mathrm{4Ns}} \equiv 1 \tag{39}$$

Formula (39) refers to the case where the end of the v_{N} vector coincides with the v_{i4} vector. It means the permanent connection of the input voltage v_{i4} with one side of the load phase during the PWM modulation period. Figure 15 shows a case, which in the one side of the load is permanently connected to an input voltage v_{i1} during PWM modulation. Sequences of the switch states shown in Figure 16 correspond to the case, which in the s_{N} switch is connected permanently to the input phase 4. The zero load voltage is generated by using the same switch in both $\mathrm{CMC_P}$ and $\mathrm{CMC_N}$ matrix converters. Simulation results for maximal voltage transfer ratio (33) are shown in Figure 17. The common-mode voltage v_{cm} is eliminated. An application of the CV-CV and CCV-CCV scheme of modulation resulting in the non-zero input displacement angle.

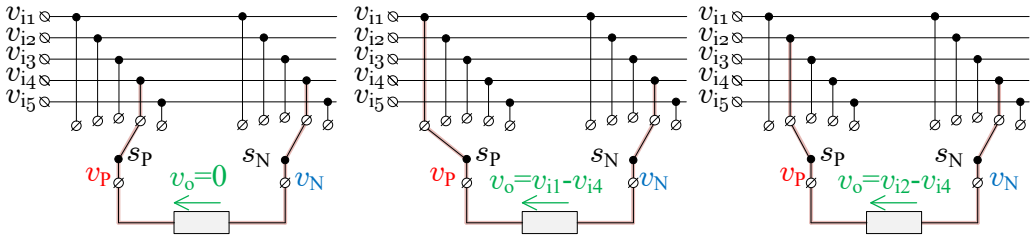
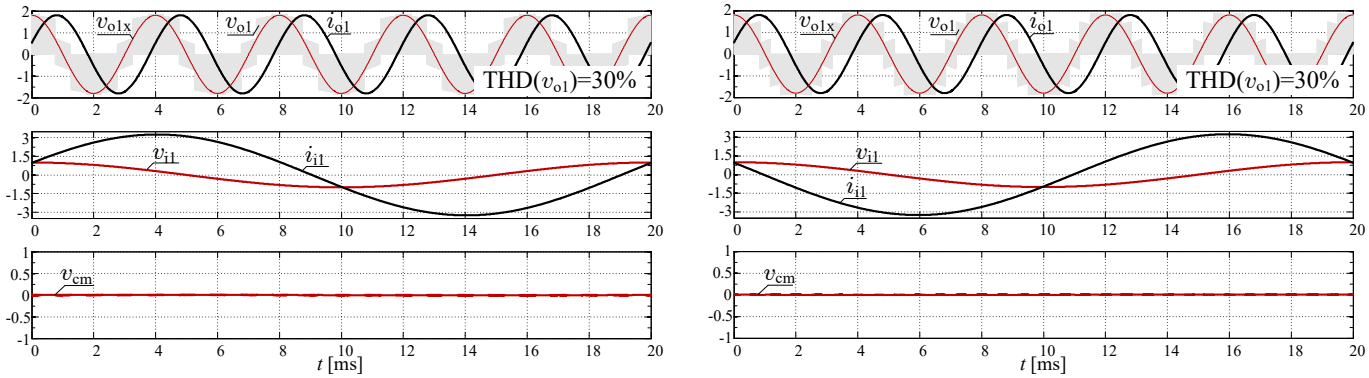
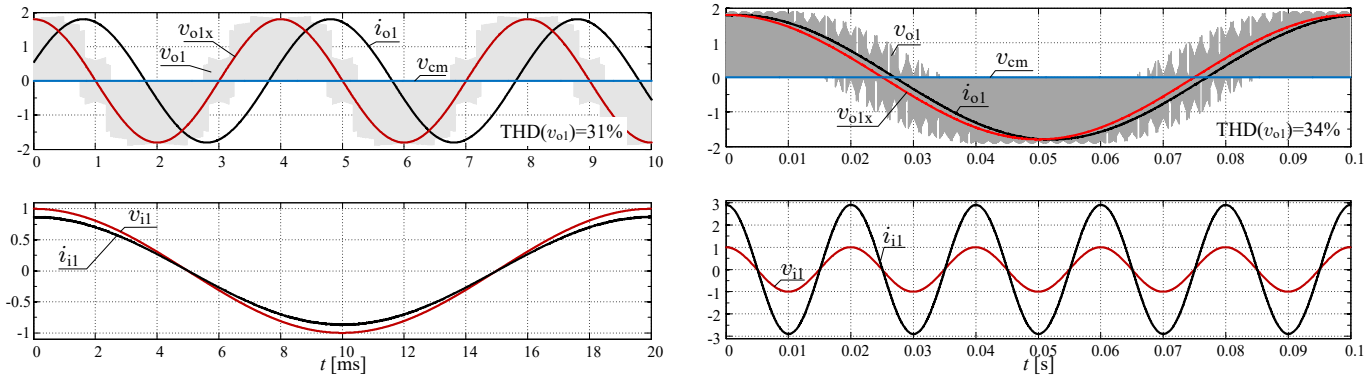


Figure 16. Sequences of the switch states in one commutation cell for the case presented in Figure 14.



(**a**) CCV-CCV (**b**) CV-CV

Figure 17. Simulation of the PWM variant 3 for DSM-CMC5 × 5 and two modulation schemes: $f_o = 250$ Hz, $q = 1.8$.



(**a**) $f_o = 250$ Hz, $q = 1.8$ (**b**) $f_o = 10$ Hz, $q = 1.8$

Figure 18. Simulation of the PWM variant 3 with toggling mode for DSM-CMC5 × 5.

Having half the number of switching operations during the PWM modulation period is an advantage of variant 3. In order to obtain the unity power factor at the system input, the sequence types have to be toggled continuously in the order CV-CV, CCV-CCV,..., etc. However, this mode of operation may require to redesign of an input filter. Example simulation results of the PWM variant 3 with toggling mode for DSM-CMC5 × 5 have been presented in Figure 18.

6. Summary and Conclusions

This paper presents a new approach to the PWM modulation for the multi-phase matrix converters supplying loads with open-end winding. The proposed approach is an alternative for the methods based on the space-vector modulation. Three variants of PWM modulation were presented. Animations for the first two of them are available at IEEE DataPort data set [40]. The first variant allows for eliminating the common-mode voltage, which is a desired feature from a practical point of view. The second variant based on a specific rearranging switches state sequences can offer quasi-multilevel waveforms with low THD. However, a common-mode voltage level can be unaccepted due to influence on the bearings lifetime. Variant 3 of the PWM modulation described in a paper offer over 12% greater voltage transfer gain. Comparison of an input angle value for the proposed variants of PWM modulation is presented in Table 1.

Table 1. Comparison of an input angle value for the proposed variants of PWM modulation.

PWM Variant	Modulation Scheme		
	$\phi_i = \varphi_o$	$\phi_i = -\varphi_o$	$\phi_i = 0$
variant 1	CCV-CCV	CV-CV	CV-CCV or CCV-CV
variant 2	CCV-CCV	CV-CV	CV-CCV or CCV-CV
variant 3	CCV-CCV	CV-CV	toggling

The multi-phase matrix converters, with an equal number of input and outputs, belong to the niche solution. Recently, we can observe an increasing interest in multi-phase systems. Furthermore, the complexity of the modulation algorithms grows up. The described proposal is a research result of analytic signal and an application of the smooth interpolation method in PWM duty cycle computing. Some selected features and properties have been compared with the space-vector method. Table 2 presents such a comparison. The PWM duty cycle computation represented by equations, from (12) to (14), is performed using only a second-order determinant of the voltages coordinate matrix without trigonometry usage. Therefore, the proposed method also naturally extends the applicability of the formulas to unbalanced and distorted AC voltage sources. Moreover, all computation can be realized in the FPGA structure using the simple multipliers and adders. The important contribution of the presented article is a presentation of the novel algorithm, which is much easier than algorithms based on the space-vector approach. This property is essential in multi-phase systems because the number of vectors is very high. The proposed solution uses only vectors that represent the Hilbert analytic signal pair calculated for the input and the reference vectors. The number of vectors needed to realize the output voltage synthesis is equal to only the sum of input and output phases.

Table 2. The comparison of the proposed modulation with the space-vector approach.

	Proposed Modulation	**Space Vector Modulation**
how the vector map is generated	using the analytic signal concept, which is based on the Hilbert transform	using the Clark transform for multi-phase systems
the difficulty of the vector map generator	comparable with SVPWM, using several methods: triple Clarke, or DSOGI, or DFT	comparable with the proposed, using the Clarke rotation operator
degree of difficulty with more phases	the number of vectors is equal to the number of converter's terminals	the number of vectors is equal to $2^{(2P)}$, where P is the number of the load phase
the common-mode voltage elimination in the multi-phase systems	yes	requires the modification of the modulation using the rotating vectors collection
minimization of the number of switching	possible for variant no. 3, in the general case a sorted and optimized the switch states sequence should be used	the minimization of the number of switching is a natural feature for the space-vector modulation, which is based on the nearest three vectors, however—for that selection can be an additional issue of computation
is it applicable for unbalanced and asymmetrical loads with the open-winding	yes	no applicable, space-vector methods assumed the symmetric loads with the open-winding
the load phase failure	ready for that failure, each load phase is controlled by an individual and independence the cell controller	in the event of the sudden change in the number of load phases, the algorithm (switches' state sequences table) must be thoroughly rebuilt, it is not possible in a real-time system, the modification can only be implemented offline
application of trigonometric functions for PWM duty cycle computing	no (it speeds up the algorithm)	yes

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Conflicts of Interest: All authors declare no conflict of interest.

Appendix A. Simulation Parameters

Table A1. Simulation parameters for DSM-CMC 5 × 5.

Parameter	Value
Number of input voltages	5
Number of output voltages	10
Number of an ideal bidirectional switches	50
Source phase voltage amplitude	$V_{\mathrm{i}} = 100$ V
Input frequency	$f_{\mathrm{i}} = 50$ Hz
Output frequencies	$f_{\mathrm{o}} = 10$ Hz, 250 Hz
Voltage gain of $\mathrm{CMC_P}$	$q = 0.8$
Voltage gain of $\mathrm{CMC_N}$	$q = 0.8$
The load parameters	$R_{\mathrm{o}} = 0.5\ \Omega$, $L_{\mathrm{o}} = 1$ mH
An algorithm frequency	$f_{\mathrm{s}} = 10$ kHz
Simulation step	250 ns
Simulation software	PSIM 64-bit Version 11.0.3

Table A2. Simulation parameters for DSM-CMC 12 × 12.

Parameter	Value
Number of input voltages	12
Number of output voltages	24
Number of an ideal bidirectional switches	288
Source phase voltage amplitude	$V_{\mathrm{i}} = 100$ V
Input frequency	$f_{\mathrm{i}} = 50$ Hz
Output frequencies	$f_{\mathrm{o}} = 10$ Hz, 300 Hz
Voltage gain of $\mathrm{CMC_P}$	$q = 0.95$
Voltage gain of $\mathrm{CMC_N}$	$q = 0.95$
The load parameters	$R_{\mathrm{o}} = 10\ \Omega$, $L_{\mathrm{o}} = 0.1$ mH
An algorithm frequency	$f_{\mathrm{s}} = 100$ kHz
Simulation step	100 ns
Simulation software	PSIM 64–bit Version 11.0.3

Simulation research has been performed for symmetric and balanced source and load. Obtained currents and voltages have been presented as $p.u.$ values referred to the base voltage $V_{\mathrm{base}} = V_{\mathrm{i}}$ and the base current equal to $I_{\mathrm{base}} = V_{\mathrm{i}}/Z_{\mathrm{o}}$, where Z_{o} was a load impedance.

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