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CMOS implementation of an analogue median filter for image processing in real time

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Abstract. An analogue median filter, realised in a 0.35 μm CMOS technology, is presented in this paper. The key advantages of the filter are: high speed of image processing (50 frames per second), low-power operation (below 1.25 mW under 3.3 V supply) and relatively high accuracy of signal processing. The presented filter is a part of an integrated circuit for image processing (a vision chip), containing: a photo-sensor matrix, a set of analogue pre-processors, and interface circuits. The analysis of the main parameters of the considered median filter is presented. The discussion of important limitations in the operation of the filter due to the restrictions imposed by CMOS technology is also presented.

Key words: analogue CMOS circuits, early vision processing, median filter, low-power.

1. Introduction

One of the most frequently performed operation on images is median filtering [1]. This non-linear operation is used mainly to enhance image quality, because it allows for the removal of high frequency impulsive noise while preserving sharp edges in the original image. Due to that advantageous properties the median filtering greatly facilitates further image processing such as edge detection or segmentation. Two kinds of techniques are used in integrated circuits to implement the median filters, analogue [2–15] and digital [16–19], depending on the design requirements. Typically, the analogue median filters allow a greater reduction in power consumption, because they do not require analogue to digital conversion (ADC) of the video signals generated by the photo sensors. Contrary, the digital filters require ADC for each analogue input signal, which for a 3×3 kernel requires 9 additional converters. Alternatively, a single fast converter multiplexed between 9 input signals can be used, but that configuration reduces an image processing speed. As it is seen, the needed number of ADCs increases with the square of the kernel size, which means that for practically used kernels, the final circuit becomes excessively large, consuming a relatively large supply power. The analogue implementations of the median filters are simpler in construction, consume less power, and are much faster, but have a limited accuracy of signal processing. Therefore, if the processed image signals are of a low or moderate dynamic, it is advantageous to use analogue filters. The presented median filter is a development of the research on the vision-chip reported in [20–22].

In the remainder of this paper the details of an integrated analogue median filter, realized in a CMOS 0.35 μm technology, are presented. In Sec. 2 the configuration, the principle of operation, and analysis of important parameters of the filter are presented and explained. Section 3 is devoted to details of the filter implementation and results of simulation and measurements. Section 4 presents a prototype image processing system and examples of real image processing. The final discussion and conclusions are presented in the last section.

2. Median filter

2.1. General structure. Figure 1 shows a block diagram of the designed analogue median filter, which consists of 19 MAXMIN circuits. Each MAXMIN circuit has two inputs V_{in1} and V_{in2}, and two outputs $V_{\max}$ and $V_{\min}$. The output signals depend on instantaneous values of both inputs, according to the following relationships

$$\left.\begin{aligned} V_{\max} &= V_{in1} \\ V_{\min} &= V_{in2} \end{aligned}\right\} \quad \text{when} \quad V_{in1} > V_{in2},$$
$$\left.\begin{aligned} V_{\max} &= V_{in2} \\ V_{\min} &= V_{in1} \end{aligned}\right\} \quad \text{when} \quad V_{in1} < V_{in2}. \tag{1}$$

As (1) shows, the MAXMIN circuit selects the maximum input value and transmits it to the output labelled as $V_{\max}$, and analogously, the minimum input value is directed to the output $V_{\min}$. As a result, 19 MAXMIN circuits combined in a way shown in Fig. 1, realize the bubble sort algorithm. The final output voltage V_{out} takes the median value of all 9 input signals $V_{i1} \ldots V_{i9}$

$$V_{out} = MED\left\{V_{i1}, V_{i2}, \ldots, V_{i9}\right\}. \tag{2}$$

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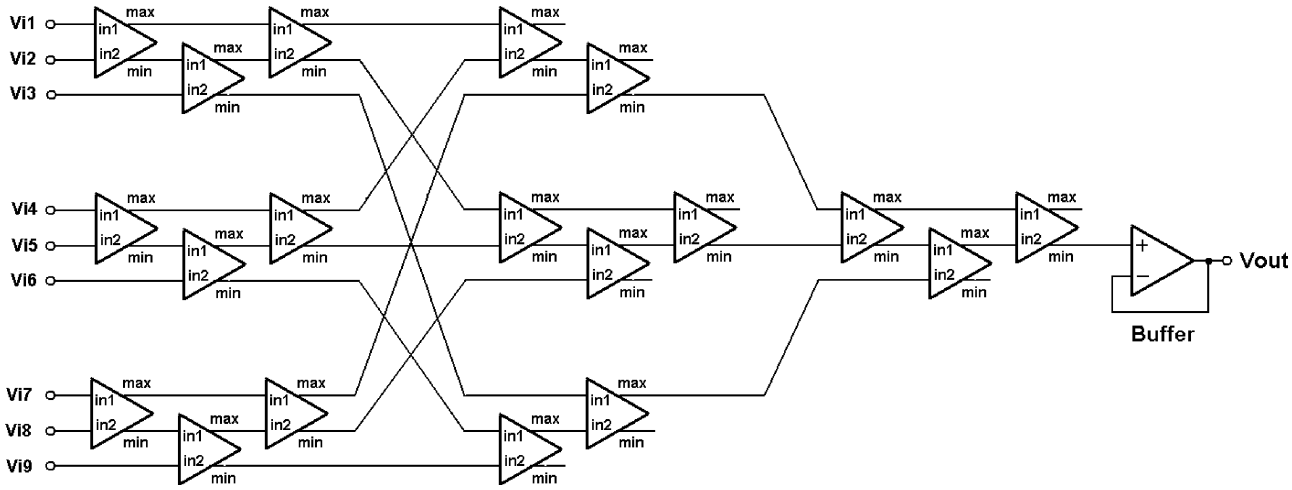

Fig. 1. Block diagram of an analogue median filter

The topology, shown in Fig. 1, has several advantages in comparison to other median filters presented in the literature [2, 4–5, 11, 13]. First of all, the considered median filter is devoid of the negative feedback loops, which guarantees the stability, and an aperiodic time response. Secondly, the MAXMIN circuits can be relatively simple, having very simple circuit realizations, based on a voltage comparator and an analogue multiplexer. And finally, due to the configuration in Fig. 1 has only forward paths, its time response is very fast. The time delay of such a configuration can be easily estimated on the transmission delay of a single MAXMIN circuit. Similarly, the total resolution of the median filter is determined by the resolution of an individual MAXMIN circuit in a signal transmission path. The latter feature greatly simplifies the design of the entire median filter, as it simplifies the estimation of the required specification for the MAXMIN circuits.

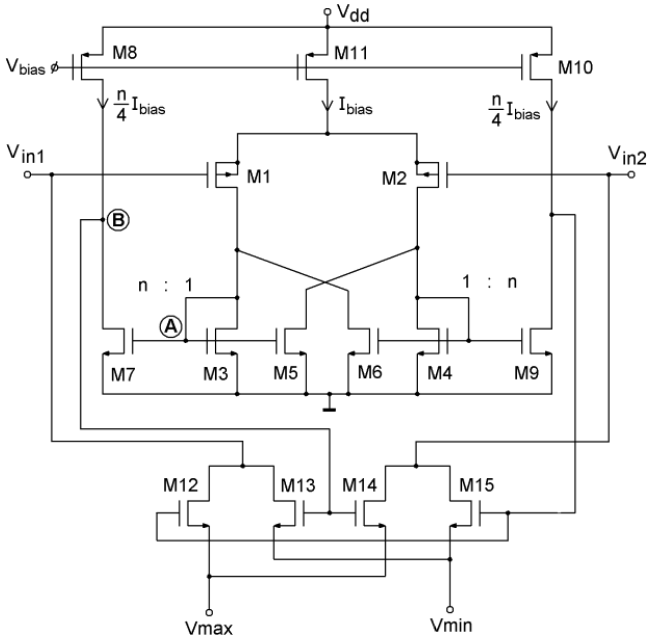

Fig. 2. Schematic of the MAXMIN circuit

The MAXMIN circuit is designed using a differential two stage voltage comparator, which controls an analogue multiplexer composed of 4 MOS switches. Figure 2 shows the details of the circuit. The differential pair M1–M2, together with the active cross-coupled load M3–M6 make the input stage of the comparator. Such a configuration ensures a good stabilization of the common-mode output voltages and a relatively high differential gain. The output stages, based on M7–M8 and M9–M10, generate balanced signals, which controls the switches M12–M15. It is worth to notice, that the series resistance of those switches does not affect the function of the circuit (1), because in the steady state there is no current flow between the filter inputs $V_{i1} \ldots V_{i9}$ and the output V_{out}, and consequently there is no voltage drop.

2.2. Circuit limitations. In the filter in Fig. 1 the input signals propagate in parallel through the layers in the structure. The total propagation time of each signal depends on the path, which it passes. In the worst case, this time is equal to 9 delays of a single MAXMIN circuit. The propagation delay of MAXMIN consists of the delay introduced by the comparator and the delay of the analogue multiplexer. The propagation delay time of the comparator is estimated under assumption that the input differential signal is big enough to fully switch on one of the transistors M1 or M2 (Fig. 2), causing the biasing current I_{bias} to flow through one of them. The propagation time can be estimated as a sum of two components: (i) the delay $t_{delay,A}$ between the input and the node labelled A, and (ii) the delay $t_{delay,B}$ between the node labelled A and B (the comparator output).

$$t_{delay} = t_{delay,A} + t_{delay,B} = \frac{0.5\Delta V_A}{SR_A} + \frac{0.5\Delta V_B}{SR_B} = \frac{0.5\Delta V_A}{SR_A} + \frac{0.5V_{DD}}{SR_B}, \tag{3}$$

where ΔV_A and ΔV_B denote the voltage swings at nodes A and B, SR_A and SR_B are the slew rates at the same nodes. SR_A depends on the biasing current I_{bias} and the total capacitance of the node A, which results in

$$SR_A^+ = SR_A^- \cong \frac{I_{bias}}{2C_{gs3-6} + C_{gs7} + (1 + A_7)\, C_{gd7} + C_{gd1} + 4C_{gd3-6}}, \tag{4}$$

where $A_7 = g_{m7}/(g_{ds7} + g_{ds8})$ is the voltage gain of M7. The positive and negative slew rates at the node B are determined respectively by the drain current of M8 and M7, and the total capacitance of this node, which leads to

$$SR_B^+ \cong \frac{(n/4)\, I_{bias}}{2C_{gs13,14}}, \tag{5a}$$

$$SR_B^- \cong \frac{nI_{bias}}{2C_{gs13,14}}. \tag{5b}$$

The expressions (5a) and (5b) show, that the slew rate for a rising edge is 4 times smaller than the slew rate for a falling edge. The voltage swing ΔV_A can be calculated bearing in mind that the full biasing current I_{bias} flows through M1, and as a result only M3 is active in the load circuit.

$$\Delta V_A = V_{gs3}|_{I_D = I_{bias}} - V_{gs3}|_{I_D = 0} = \sqrt{\frac{2I_{bias}}{\mu_0 C_{OX}\, (W/L)_3}}, \tag{6}$$

where μ_0, C_{OX}, and (W/L) have their usual meanings. The worst case of the total propagation delay can be calculated using (4), (5a), (6), and (3). Assuming that: $(W/L)_{1,2} = 10$ μm/1 μm, $(W/L)_{3-6} = 2$ μm/1 μm, $I_{bias} = 10$ μA, and $n = 2$, the following results were obtained: $\Delta V_A = 0.34$ V, $SR_A = 61.7$ V/μs, and $SR_B^+ = 2270$ V/μs. The propagation delays for this case are $t_{delay,A} = 5.54$ ns, and $t_{delay,B} = 0.72$ ns. Finally, the analytically calculated value of the total propagation delay is $t_{delay} = 6.26$ ns, whereas the delay determined based on the circuit simulation is 4.42 ns.

The delay time of the analogue multiplexer can be resolved based on the time constant associated with the resistance r_{ds1215} of the turned-on switches M12–M15 and the input capacitance C_{in} of the comparator. Assuming that $(W/L)_{12-15} = 1$ μm/0.35 μm, the worst case of $r_{ds12-15}$ is about 7–8 kΩ. The estimated input capacitance of the comparator for $(W/L)_{1,2} = 10$ μm/1 μm and $(W/L)_{3-6} = 2$ μm/1 μm is about $C_{in} \approx 120$ fF. The time constant for this case is about 0.95 ns, which means that the delay of the multiplexer is much smaller than the delay of the comparator.

According to (4) and (5), the speed of the MAXMIN circuit depends on the parasitic capacitances of the transistors. On the other hand, the resolution and the input offset voltage of the comparator is proportional to the geometrical dimensions of transistors M1–M6. The bigger transistors, the lower input offset voltage (V_{OS}) and consequently a better resolution. Using analysis described in [23] the V_{OS} of the comparator in Fig. 2 is

$$V_{OS} = \left(\frac{A_{VTpMOS}}{\sqrt{WL}}\right)_{1,2} + \sqrt{2\frac{K_{PN}}{K_{PP}}\left(\frac{L}{W}\right)_{1,2}\left(\frac{W}{L}\right)_{3-6}}\left(\frac{A_{VTnMOS}}{\sqrt{WL}}\right)_{3-6}, \tag{7}$$

where K_{PN}, K_{PP} and A_{VTnMOS}, A_{VTpMOS} are the transconductance and the Pelgrom's model [24] matching parameters for n and p channel transistors, respectively.

To find the best circuit solution, a trade-off between the speed and resolution requirements for the MAXMIN circuit has to be determined. In order to perform median filtering of images with resolution 640×480 pixels at 50 frames per second, the propagation delay time of MAXMIN circuit must be less than 7 ns. Furthermore, assuming that the video signal is in the range of 0–1.8 V, to obtain processing of 7 bits resolution, the required V_{OS} of the comparators must be less than 14 mV. For the technology parameters $K_{PN} = 170$ μA/V^2, $K_{PP} = 58$ μA/V^2, $A_{VTnMOS} = 9.5$ mVμm, $A_{VTpMOS} = 14.5$ mVμm, a satisfactory circuit solution was achieved using (3)–(7) and a Spectre simulations. The final circuit parameters are as follows: $(W/L)_{1-2} = 10/1$, $(W/L)_{3-6} = 2/1$, $(W/L)_7 = (W/L)_9 = 4/1$, $(W/L)_8 = (W/L)_{10} = 2/1$, $(W/L)_{11} = 4/1$, $(W/L)_{12-15} = 1/0.35$. The biasing currents are established to be 10 μA for M11, and 5 μA for M8 and M10. The Monte Carlo analysis reveals that for the worst case, the propagation delay time t_{delay} is less than 4.4 ns, and the input offset voltage is below 13.8 mV (3 sigma). The summary of the main parameters of the MAXMIN circuit is given in Table 1.

Table 1

The simulated parameters of the MAXMIN circuit

Technology CMOS	0.35 μm AMS
Supply voltage	3.3 V
Input offset (1 sigma)	4.6 mV
ICMR	2 V
Dynamic power consumption @10MHz 1 V_{pp}	54 μW
Propagation delay	4.4 ns
Comparator gain	3800 V/V

3. Measurements of a median filter

The median filter of the topology presented in Fig. 1 was carefully tested by means of simulations and measurements. The limit of the filter resolution was determined based on measurements using 9 input test signals. For the signals differentiated by less than 10 mV the filter was not able to properly determine the correct result. The measured input voltage range is 0–1.8 V, which means that the relative resolution of the filter is 0.55% (7 bits). The time response of the filter for a test signal is presented in Fig. 3. A set of 9 triangle waveform signals (thin lines) is applied to the filter inputs. All the triangle signals, with the same amplitude of 1.8 V, are delayed by 1 μs relative to each other. In this case, the filter is driven by all possible combinations of the inputs. The solid line in Fig. 3 shows the output voltage of the filter, which correctly determines the median value, according to the formula (2). All the above simulations were performed taking into account parasitic capacitances and resistances achieved after the post layout (Fig. 4) extraction.

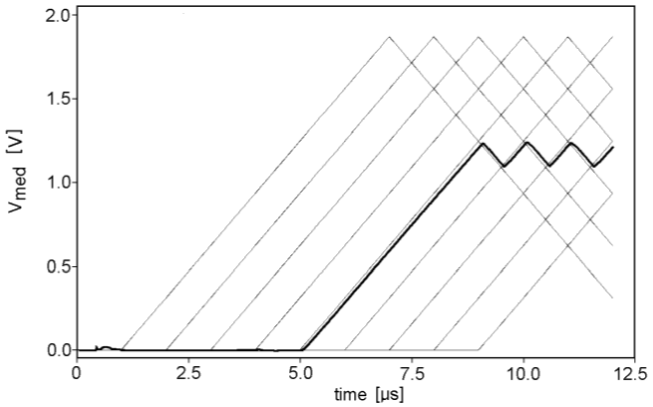

Fig. 3. The output response of the median filter for triangle waveforms

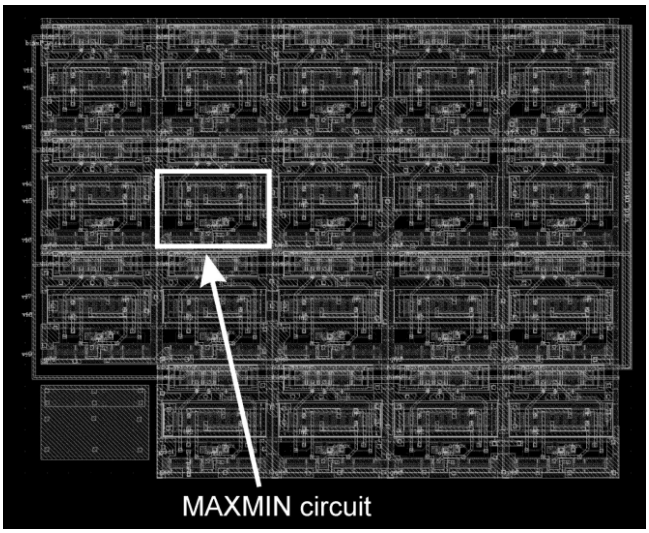

Fig. 4. Layout of the median filter: width 135 μm, height 105 μm

The dynamic properties of the filter were achieved for the worst case. As Fig. 1 shows, the total delay time depends on the combination of the input signals, and reaches its maximum when the input signals propagate through 9 MAXMIN circuits. A time response of the filter was measured for that case. Fig. 5 presents the square wave input signal V_{i5} of 10 MHz frequency, and the output V_{out} of the filter. For the considered case, the total delay is about 34 ns. This means that the achievable speed of an image reconstruction is 10 mega pixels per second. The median filter consumes about 1.2 mW of power upon 3.3 V supply, at full speed of operation.

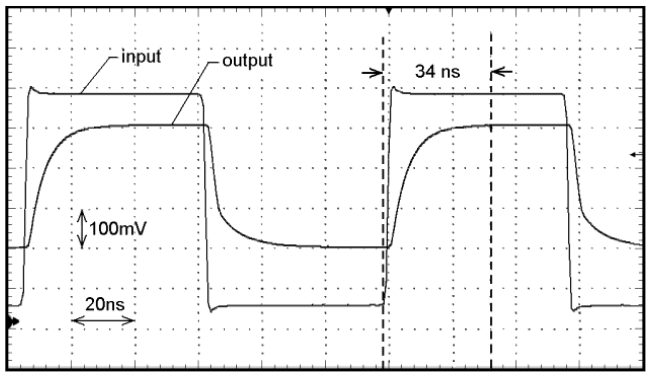

Fig. 5. The waveforms applied to determine the transmission delay

3.1. Comparison. The performance comparison of the proposed median filter to other analogue solutions is summarized in Table 2. All the compared filters operate in continuous time, but they differ in the applied circuit technique and number of inputs. For example, in [4] the analogue delay cells and comparators are used to implement a 9-input median filter. The references [2] and [5] present the filters which perform the bubble sort algorithm using current mirrors and current comparators. Another technique is used in [11] and [13], where 3-input filters are designed using differential amplifiers, and a feedback. A complete comparison of the filters is difficult because in most of the works, the authors do not specify a full set of the filter parameters. Nevertheless, in terms of power consumption, accuracy, speed and area, our median filter is competitive to other solutions.

Table 1
Comparison of the selected median filters

	this work	[5] 2004	[4] 2004	[2] 2007	[13] 1993	[11] 1997
No. of inputs	9	9	9	3	3	3
Technology	0.35μm	0.25μm	2μm	0.35μm	2μm	2μm
Supply	3.3 V	1.5 V	5 V	3.3 V	5V	5V
Accuracy	10 mV(0.55%)	1.2%	NA	NA	10 mV(0.27%)	NA
Input range	0–1.8V	NA	0.7–1.5V	NA	0.8–4.5V	NA
Powerconsumption	1.25mW	NA	14mW	NA	5.6mW	7mW
Delay time	34ns	80ns	NA	NA	NA	200ns
Area [mm^2]	0.014	NA	0.137	0.004	NA	0.2

4. The implementation of the median filter in the vision system

4.1. System architecture and experimental setup. The discussed median filter has been developed for use it in a prototype system with parallel processing of video signals in real time. The specialized integrated circuit, fabricated in a CMOS 0.35 μm technology, was described in detail in [20] and [21].

The system consists of a 32×32 photo-pixel matrix and 32 analogue convolution filters (Fig. 6), which perform a parallel image processing, reaching 2000 frames per second. Due to the limited area of the prototype integrated circuit, only a single median filter is implemented. The video signals from the matrix are sequentially directed to the median filter using an analogue multiplexer, as shown in Fig. 7. For this reason, the maximum speed of a signal processing is relatively low, about 30 frames per second. Based on simulation, the maximum speed of the median filtering is estimated to be about 1600 frames per second if the parallel processing is used. The predicted power consumption of a complete system (32 median, and 32 convolution filters) will be below 1.5 mW, when a special supply save mode is applied to the convolution processors [20].

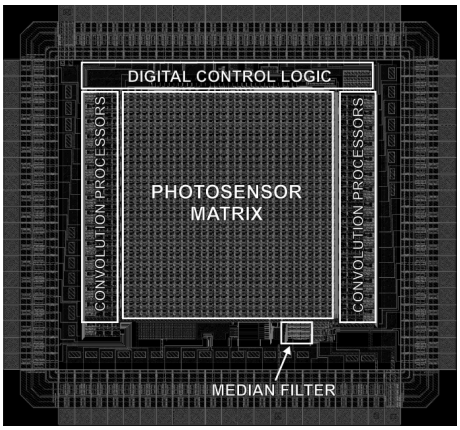

Fig. 6. Architecture of a prototype integrated vision system

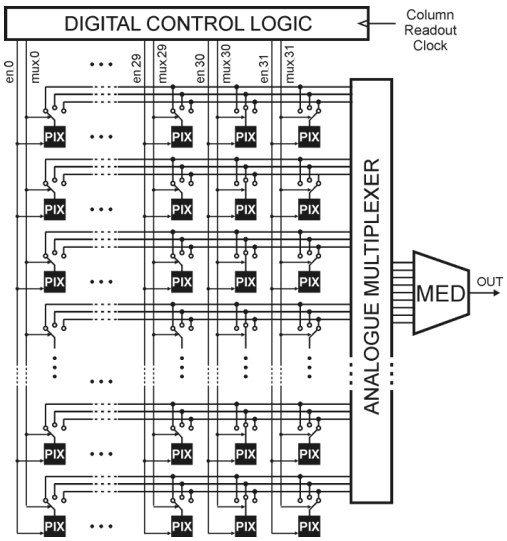

Fig. 7. Arrangement of a median filter and a pixel matrix

The operation of the vision system is controlled by the logic circuits programmed via an input-output port. The video signals from the prototype are converted to a digital form in real time by ADC converters. The complete measuring system contains FPGA platform, a test board with prototype ASIC and a personal computer with a dedicated software (Fig. 8).

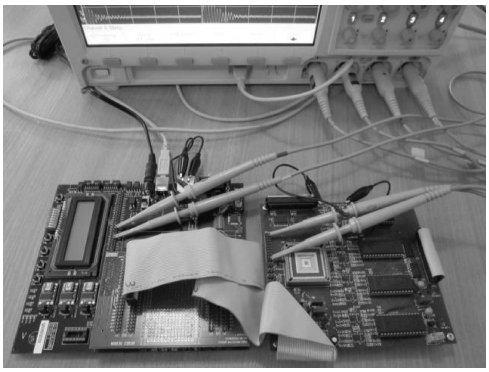

Fig. 8. Photography of a measurement system

4.2. Example of image processing. The raw images generated by a CMOS photo matrix are of low quality, due to the fixed pattern noise (FPN), random noise (RN), photo-response non-uniformity, and so called 'death' pixels (DP) [25]. An example of such an image is presented in Fig. 9a. Without proper processing, this kind of image has little application in practice. One of the most frequently used methods for image enhancement are a low-pass convolution filtering or a median filtering. The sample processing results, using the prototype image system and both types of filtering, are depicted in Fig. 9. As Fig. 9b shows, the convolution filtering reduces

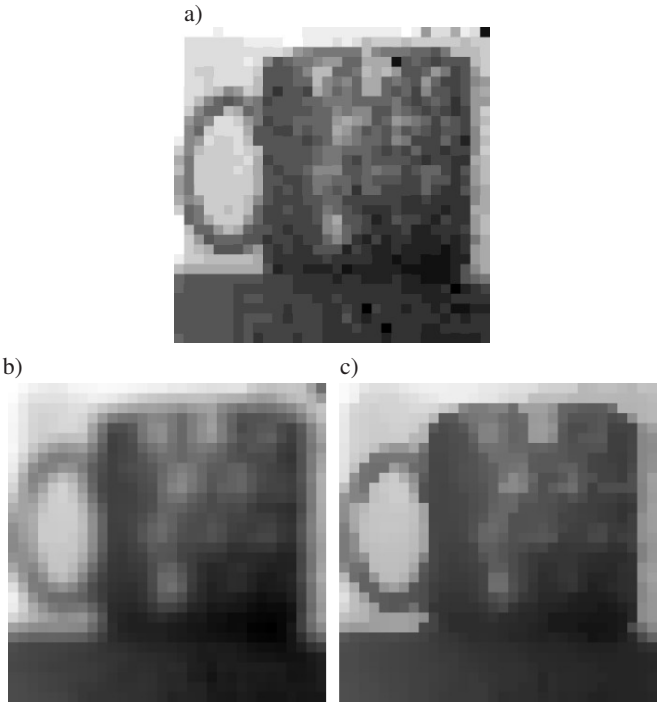

Fig. 9. Results of an exemplary image processing: a) raw image, b) low pass convolution filtering, c) median filtering

FPN and RN, but also causes an image blur, which in turn deteriorates the overall image quality. Significantly better results can be achieved with the median filtering (Fig. 9c), where after the removal of FPN, RN, and DP, the sharp edges of the object are preserved.

5. Conclusions

A low-power, high-speed, compact 9-input analogue median filter based on a bubble sort network is presented. The operation of the designed filter has been carefully tested by means of simulations and measurements, performed with the use of a test vision system containing an integrated prototype visionchip. The presented filter has advantages such as a high processing speed and low power consumption. Its resolution is better than 0.55 %, the delay time is below 34 ns, and the total power consumption is 1.25 mW. The filter has a very compact layout and occupies a relatively small area equal to 0.014 mm^2. Due to the small area and low power consumption the filter is attractive for implementation of large, parallel, real-time image processing systems with a high computation rate.

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