Feasibility Study GaN Transistors Application in the Novel Split-Coils Inductive Power Transfer System with T-Type Inverter

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Abstract: A promising solution for inductive power transfer and wireless charging is presented on the basis of a single-phase three-level T-type Neutral Point Clamped GaN-based inverter with two coupled transmitting coils. The article focuses on the feasibility study of GaN transistor application in the wireless power transfer system based on the T-type inverter on the primary side. An analysis of power losses in the main components of the system is performed: semiconductors and magnetic elements. System modeling was performed using Power Electronics Simulation Software (PSIM). It is shown that the main losses of the system are static losses in the filter inductor and rectifier diodes on the secondary side, while GaN transistors can be successfully used for the wireless power transfer system. The main features of the Printed Circuit Board (PCB) design of GaN transistors are considered in advance.

1. Introduction

Interest in inductive wireless power transmission is constantly growing due to the increasing interests of both low-power wireless chargers for mobile and wireless charging stations of medium and high power for electric bikes and electric vehicles. Such chargers transfer the electric energy wirelessly from primary to secondary inductor by means of inductive coupling [1]. Inductive wireless power transfer systems consist of a transmitting part (contains an inverter, compensation circuit and primary inductor) and a receiving part (receiving inductor, compensation circuit, rectifier) [1]. The researchers have already analyzed the main possible topologies of compensation schemes, their advantages and disadvantages, and described the general recommendations for their implementation. It is well known that Wireless Power Transfer (WPT) systems have some limitations, such as short transmission distance(centimeters or dozens of centimeters at acceptable levels of transmission efficiency) [2,3], sensitivity to the exact positioning of the receiving coil relative to the transmission coil [2,4], size and cost of the system.

Among existing limitations, the issue of the size and cost of the WPT system is one of the most important. Researchers are still looking for the optimal system configurations and topologies of power converters that would best meet the above requirements.

Different types of switches are utilized in the power electronics converters [5–8]. The conventional Insulated Gate Bipolar Transistors (IGBTs) are gradually going out of use in industrial circuits of WPT systems due to their low switching capability [9]. The reverse blocking voltage capability of the conventional IGBT is very low; there are relatively large power losses [10]. It is well known that the use of wideband gap semiconductors (such as GaN-transistors) instead of classical Si power switches can significantly reduce the power losses that lead to the increasing of the system efficiency or significantly increase switching frequency reducing size of passive elements [11–13]. It is advisable to use GaN transistors for T-type topologies [5–8,14]. The GaN features fast switching, low parasitic charges, reverse conductivity with zero recovery charge and low driving power losses and dynamic losses; compared to Si-IGBTs and SiC-MOSFETs [5,6,15–18], higher efficiency, low parasitic output capacitance [16–18] can be achieved. The advantage of GaN over Si is mostly visible at higher frequencies in dynamic losses [15,19]. However, the conduction losses are comparable with the SIC semiconductors [18,19].

The main goal of the article is to study the feasibility of GaN transistor application in the proposed non-traditional (non-classical) WPT system. This will be based on the loss analysis of the main components of the circuit.

The paper, consisting of seven sections, proposes a new solution of the wireless power transfer system based on two parallel single-phase T-type GaN-based invertors (dual T-type inverter) with two transmitting coils on one ferrite core (coupled transmitting inductances). The case study system description and advantages of such solution are represented in Section 2 of the paper. According to previous research [20], more than 70% of the losses in WPT systems for various cases of power, loads and working frequencies depend on semiconductors and inductors [20,21]. Therefore, the contribution of such parameters was taken into account in calculations in this paper. Confirmation of the advantages of the proposed solution, made mainly by power losses analysis, described in Sections 3–5. Sections 3 and 4 proposes the losses models of the GaN transistors and coil inductors, respectively. Simulation and experimental verification of the proposed solution is described in Section 5, with conclusions and list of patents devoted to the proposed WPT system on Sections 6 and 7, respectively.

2. Case Study System Description

Figure 1 depicts the proposed circuit of a multi-level converter for WPT. The primary converter consists of a full-bridge three-level T-type inverter connected to bidirectional auxiliary semiconductor switches. The GaN-based T-type inverter is first proposed for use in a WPT system together with two coupled inductors. It provides a number of advantages over existing analogues.
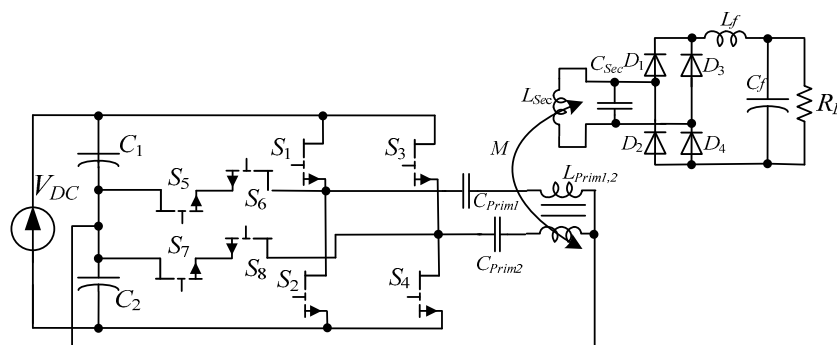

Figure 1. Proposed Inductive Power Transfer IPT converter.

The DC source is applied to the T-type inverter. The energy is transmitted to the secondary side through the primary coils with an air gap (Figure 1). The output current is rectified by the passive full-bridge rectifier, filtered and supplied to the load.

In the scheme, V_{dc} is the source of the input dc voltage; C_1, C_2—input capacitors; S_1–S_4—switches of the single-phase full-bridge inverter; S_5, S_6 and S_7, S_8—auxiliary bidirectional switches; $L_{prim1,2}$—coupled primaries inductances; C_{prim1}, C_{prim2}—primaries compensating capacitances; L_{sec}—secondary inductance; C_{sec}—secondary compensating capacitance; D_1–D_4—bridge rectifier; C_f—filter capacitor; L_f—filter inductance; R_L—output resistive load.

First of all, the multi-level inverters have a number of advantages over conventional H-bridge inverters, including better Electromagnetic Compatibility EMC and higher efficiency [14,22–24], which are extremely important for wireless power transmission systems [24]. However, analysis of the existed publications shows that using of multi-level inverters for WPT systems are just at the beginning stage [25].

Each multi-level circuit has its advantages and disadvantages, but among these types, T-type has some advantages over other types: smaller size, simpler operation principles, lower THD, lower conduction losses and smaller number of semiconductors [10,14,23]. The most important advantage of T-type solution in the WPT application is that only half of dc-link voltage applied to the primary side coil which in turn reduces the primary inductance and size of the coil [14]. The equation (1) for calculating the primary inductance L_{prim} at SP compensation analytically confirms this fact [20]:

$$L_{Prim} \approx L_{Sec}\left(\frac{8}{\pi^2 k_{nom}} \frac{V_{in}}{V_{out}}\right)^2, \tag{1}$$

where L_{sec}-secondary side self-inductance, k_{nom}—nominal coupling, V_{in} and V_{out}—input and output voltages, respectively.

Finally, the splitting of the transmitting coils will reduce the conduction and overall diameter of the primary inductance. The application of two coupled transmission coils of inductance on a single ferrite core reduces the total dimensions of the magnetic components on the primary side (and the losses in copper and ferrite). Multiple magnetic resonant coils lead to higher transmission efficiency and longer transmission distances [26]. In addition, the coupling coefficient between them is considered constant, which simplifies certain calculations of the system. Furthermore, this solution reduces the current through each coil. This leads to a lower overall resistance of the transmission coils, which, in turn, increases the Q factor and the energy transfer efficiency.

It is expected that wireless power transmission systems based on of multi-coil circuits with GaN-based T-type inverters in the transmission part is a promising solution, joining the advantages of the parts which already existed. The proposed solution does not have any heatsinks, has reduced the size of primary coils and can be considered for industrial application. Such a system can be used directly in power supply systems for transmission on different power levels.

Compensating capacitors are required to compensate the leakage inductance on the primary and secondary sides in the WPT systems. In this case, the possible distance between the coils increases [2]. Systems with Series-Parallel (SP) compensation work efficiently with a wide range of loads in addition to the advantages for middle-power and low-power applications and allow reducing dimensions of the receiver coil [20]. Series-Series (SS) compensation does not depend on the change of magnetic coupling and load. These compensation topologies are most widely used for wireless charging. This solution is very well investigated; its benefits and drawbacks are well known [2,27–29].

3. Losses Models of the GaN Transistors

The main sequence of the calculations is presented in this section and Section 5. Initially, the control signals and the shape of voltage and current signals in the inverter were derived from simulation and are used for calculations of power losses in semiconductors.

3.1. T-type Inverter Operation Mode

Two auxiliary switches S_5 and S_6 (Figure 1) are turned on in the T-type topology (Figure 2). Switching states and the voltage are shown for the 3-level T-type Neutral Point Clamped NPC inverter in Table 1 for Figure 1 (for one leg).
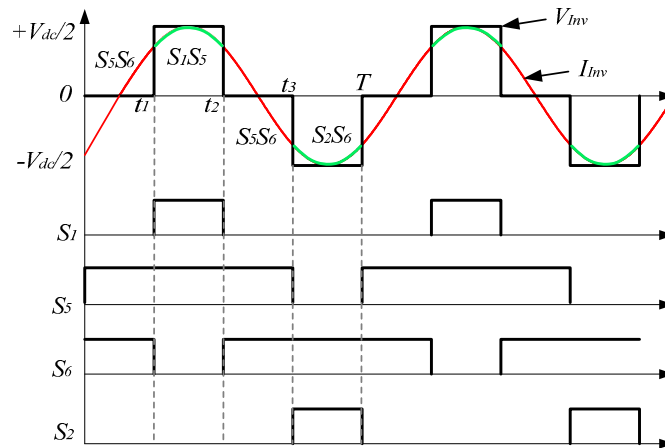

Figure 2. Control signal sequences and shapes of the voltage and the current of the IPT converter. Static losses are calculated, knowing the current through each transistor at a certain interval.

Table 1. Switching States and Voltage for the 3-Level T-Type NPC Inverter [23].

Level	S_1	S_5	S_6	S_2	Voltage
Positive (+)	1	1	0	0	$+V_{dc}/2$
Neutral (N)	0	1	1	0	0
Negative (−)	0	0	1	1	$-V_{dc}/2$

Figure 2 shows the control signal sequence of the transistor (shown for one phase), the voltage (V_{Inv}) and the inverter output current (I_{Inv}).

3.2. Losses Model of the GaN Transistor under Compensation Condition

It is well known that the conduction losses are a significant component to estimate the total losses in the transistors [19]. In addition, the dynamic losses in GaN transistors should be taken into account. The total transistor power losses are determined by the sum of the static and dynamic losses [17].

$$P_{Total} = P_{Cond} + P_{Dyn}, \tag{2}$$

where P_{Cond}–static losses (conduction losses), P_{Dyn}—dynamic losses.

The equation that determines the conduction losses (when the transistor is fully on) is as follows:

$$P_{Cond} = I_{Drms}{}^2 + R_{DS(on)}, \tag{3}$$

where I_{Drms}–rms current value through drain, $R_{DS(on)}$—on-resistance of a transistor's drain-source.

The current I_{Drms} is determined at each interval (Figure 2) for the positive half wave as follows:

$$I^2_{S1S5} = \frac{1}{T}\int_{t1}^{t2}(i_m \sin(\omega t))^2 dt, \tag{4}$$

where i_m—amplitude value of drain current, ω—angular frequency, T—period. For the negative half wave:

$$I^2_{S2S6} = \frac{1}{T} \int_{t3}^{T} (i_m \sin(\omega t))^2 dt. \tag{5}$$

Two sections are defined for the zero state (Figure 2):

$$I^2_{S5S6} = \frac{1}{T} \int_{t0}^{t1} (i_m \sin(\omega t))^2 dt + \frac{1}{T} \int_{t2}^{t3} (i_m \sin(\omega t))^2 dt. \tag{6}$$

Currents are added from all sections and multiplied by the resistance of the transistor over a period of time due to (3) to calculate the conduction losses of the transistor.

Total dynamic power losses [17]:

$$P_{Dyn} = P_{SW(on)} + P_{SW(off)} + P_G + P_{rcl} + P_{oss} + P_{RR}, \tag{7}$$

where $P_{SW(on)}$ and $P_{SW(off)}$—switching losses, P_G—gate charge losses, P_{rcl}—power loss due to the reverse conduction voltage through the body diode; P_{RR}—reverse recovery loss; P_{OSS}—power loss due to the output capacitance.

Gate charge power losses of a transistor:

$$P_G = Q_G + V_{dr} f_{sw}, \tag{8}$$

where Q_G—total gate charge of a transistor, V_{dr}—driving voltage, f_{sw}—switching frequency.

The equations show, that charge losses are increasing at high switching frequency.

Reverse recovery loss is caused by the charge stored in the junction of the internal body diode of a transistor in the T-type inverter [19]:

$$P_{RR} = Q_{RR} \frac{V_{In}}{2} f_{sw}, \tag{9}$$

where Q_{RR} is the reverse recovery charge, V_{in}—input voltage of the inverter. In the transistor datasheet, GaN transistors do not contain the internal body diode, so, reverse recovery loss is not present in these devices.

Power losses due to the output capacitance [17] are the following:

$$P_{OSS} = f_{sw} \int_{0}^{V_{in}} (V_{DS} C_{OSS}(V_{DS})) dv_{DS}, \tag{10}$$

where C_{OSS}—output capacitance of the transistor (determined by the dependencies in the datasheet). These losses are independent of power and are insignificant at the increase of power, but the contribution of this type of losses is significant at low power and high switching frequency.

The power losses due to the reverse conduction voltage through the body diode (or dead-time losses):

$$P_{rcl} = V_{REV} I_D t_{dead} f_{sw}, \tag{11}$$

where t_{dead}—length of the dead-time (reverse diode conduction time), V_{REV}—reverse voltage drop in a GaN transistor.

The exact equations from [17,19], take into account several values (values of switching time, level of corresponding voltages, etc.) from the simulation data or the experimental data. It is not possible to accurately determine the switching time of the transistors from the model in PSIM and at high frequency. The approximate switch-on time is 4.9 ns, the switch-off time is 3.4 ns according to the

datasheet. At the same time, the duration of the on- and off-transistors of each of the shoulders in the model is much larger.

Therefore, a simplified equation is used to estimate the magnitude of switching losses quantitatively [18]:

Turn-on switching losses of a transistor:

$$P_{SW(on)} = \int_{0}^{t\_rise} (V_{DS}I_D)dt, \tag{12}$$

Turn-off switching losses of a transistor:

$$P_{SW(off)} = \int_{0}^{t\_fall} (V_{DS}I_D)dt, \tag{13}$$

where t_{rise} and t_{fall}—transistor's time for turn-on and turn-off (values from datasheet), V_{ds}—drain-source voltage, I_D—drain current.

According to [19], at frequencies below 100 kHz, switching losses of transistors are very low. Switching losses are increasing at frequencies up to 500 kHz but they have no significant effect on the total loss estimation [19]. Thus, most transistor losses are conduction losses and power losses due to the output capacitance.

3.3. Losses Model of Rectifier Diode Losses

The losses in rectifying diodes are also significant, especially at high switching frequency and high current through diodes. The parameters of high-speed Schottky diodes were used for modeling and in the experimental verification.

It is known that the static losses in a diode are determined by the current flow through the diode multiplied by the voltage drop across the diode. Two diodes simultaneously conduct current in the case of a diode bridge:

$$P_{Cond.D} = 2I_{forv}V_{drop}, \tag{14}$$

where I_{forv} is the forward current value through the diode, V_{drop}—voltage drop per diode.

Dynamic losses in the diode are switching losses. All diodes in the diode bridge are involved in the process of rectification. If a Q_{RR} value (this is the reverse recovery charge) is given in the datasheet, then the equation is as follows:

$$P_{SW\_D} = 4Q_{rr}V_{rev}f_{sw}. \tag{15}$$

Reverse recovery charge value is defined as a product of $C_{junction}$ (junction capacitance) by V_{rev} (the reverse voltage on the diode). The result in (16) is obtained by substituting this product into Equation (15):

$$P_{SW\_D} = 4V_{rev}^2 C_{junction}f_{sw}. \tag{16}$$

The total losses in all semiconductors in this scheme are higher than the losses in the transmitting and receiving coils.

4. Design and Losses Models of Coils Inductors

Coupled primary coils were calculated with a nominal value of 90 μH each and a receiving coil with a nominal value of 24 μH (Table 2).

Table 2. Parameter Table for Experiments.

Symbol	Description	Value
V_{in}	Input voltage	300 V
S_1-S_8	GaN transistors	GS66508T
F_{sw}	Switching frequency	150; 200 kHz
C_{sn}	Snubber capacity	100; 470 pF
D_1-D_4	Rectifying diodes	RB228NS100TL
$L_{prim1,2}$	Primary inductances	90 µH
L_{sec}	Secondary inductance	24 µH
k	Coupling coefficient	0.7; 0.9

4.1. Design of the Transmitter and Receiver Coils

The simulation was performed in almost the same order as described in [4]. The model of coils was carried out in ANSYS Electrimagnetic Suite and designed using the Finite Elements Modeling (FEM) method. The transmission coils are on the top and the receiving coil is on the bottom (Figure 3).
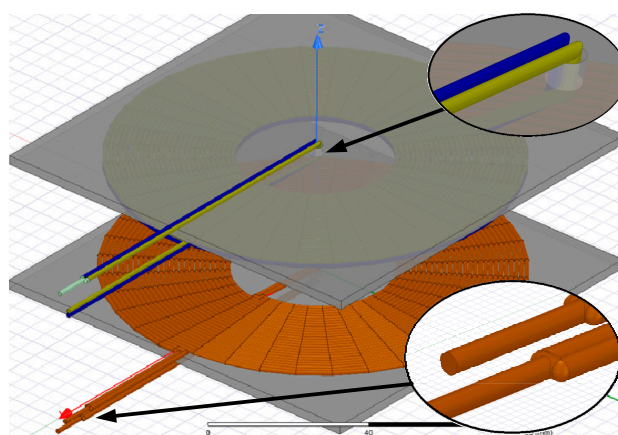
Figure 3. Designed model of coils for WPT.

The primary coil consists of two coils connected in parallel at one lead. One end of the coil pins is drawn through a hole in the ferrite. They do not interfere with the coils as close as possible to each other and do not distort the magnetic flux with this solution. Both primary coils have equal turns each. They are arranged in two layers, one above the other. This solution reduces losses in copper and ferrite and also the total dimensions of the magnetic components on the primary side. Multiple magnetic resonant coils lead to higher transmission efficiencies and longer transmission distances.

The secondary coil consists of double turns (shown in the figure with an enlarged fragment) in one layer. Coil winding with double turns reduces the coil's own resistance at the same value of the inductance itself and increases the quality factor. It increases also the maximum current that the secondary coil misses.

4.2. Losses Model of the Coils Inductors under Compensation Condition

Certain simplifications are allowed in the calculations of losses in the inductors. It is quite a complex mathematical problem to determine the core losses and eddy current losses, especially including the skin and proximity effects of inductors [30]. It is not always possible to achieve acceptable accuracy of calculations even when those losses are determined. The challenges are caused by the complex physical nature of these phenomena.

The core is mainly intended for shielding the magnetic induction flux in the WPT system [4]. Losses in the core are determined by the modified bulky Steinmetz equation at non-ideal sinusoidal voltage [20,30]. However, it is difficult to determine the ferrite coefficients for the equation since an experimental procedure is needed for a specific material under right conditions with high quality equipment. These factors are given rarely by the manufacturer. Therefore, determination of the value of core losses by other methods for this material is not accurate and has no scientific validity.

Most of the available FE tools do not support Litz wire modeling. In addition, magnetic field H differs from turn to turn at determining the proximity effect [4]. Hence, H must be evaluated in the center of each turn individually to calculate the proximity loss for each turn [20]. Conduction losses are usually added to this value at determining a skin effect [20,30]. The Litz wire reduces the skin effect and proximity effect significantly. Furthermore, the proximity effect is minimal between the transmitting and the receiving coils due to the large air gap.

The value of DC conduction losses is sufficient to understand the effect of the geometrical parameters of the coils on the losses value in transistors and coils.

Conduction (ohmic) losses in the primary coils:

$$P_{Lprim12} = I_{Lprim\_rms}^{2}(2R_{Lprim}), \tag{17}$$

where I_{Lprim_rms}—current through primary coils; R_{Lprim}—resistance of one primary coil. Both paired transmitting coils are the same and have the same resistance in this case.

Conduction losses in the secondary coil are as follows:

$$P_{L\sec} = I_{L\sec\_rms}^{2}R_{L\sec}, \tag{18}$$

where I_{Lsec_rms}—current through the secondary coil.

Power losses in the primary coils mostly depend on the inverter current, together with the own resistance of the primary coil.

5. Results of Experiments and Simulation

An experimental model was made to check the feasibility of using GaN transistors in the described scheme (Figure 4). Transistors GS66508Twere used with maximum drain current of 30 A, maximum drain-to-source voltage 650 V, drain-to-source on resistance at 25 °C equal to 50 mΩ. The transistor has zero reverse recovery loss, fast fall and rise times, low inductance and low thermal resistance in a small package. The GS66508T is a top-side cooled transistor that offers very low junction-to-case thermal resistance. Transistors are located at the bottom of the Printed Circuit Board (PCB) without additional radiators. These features combine to provide very high efficiency of power switching.

The PCB consists of four copper layers, divided into signal and power parts. In the signal part of the board top and bottom layers are devoted for signal traces and internal layers for power supply voltage and ground polygons. In contrast, all layers, external as well as internal, are used for power traces. Some special techniques were used on the PCB aiming increase the efficiency and decrease power losses. First of all, high-current power traces were repeated on all four layers and stitched with via matrix to reduce parasitic resistance of such traces. GaN transistors, as it was mentioned above, were placed on the bottom side of the board in accordance to the producer's recommendations [31]. Taking into account that GaN transistors can operate on high frequencies, EMC considerations was implemented on the board. Image of the bottom side of the board with power GaN transistors and other components of one half of T-type circuit is shown on Figure 5. It should be noted that component designators on Figure 5 corresponds to designators on Figure 1. Highlighted components representing current flow in the circuit for switching states marked as "*Positive* (+)" in the Table 1. As it can be seen, such placement of the components on PCB provides as low as possible square of current loops.
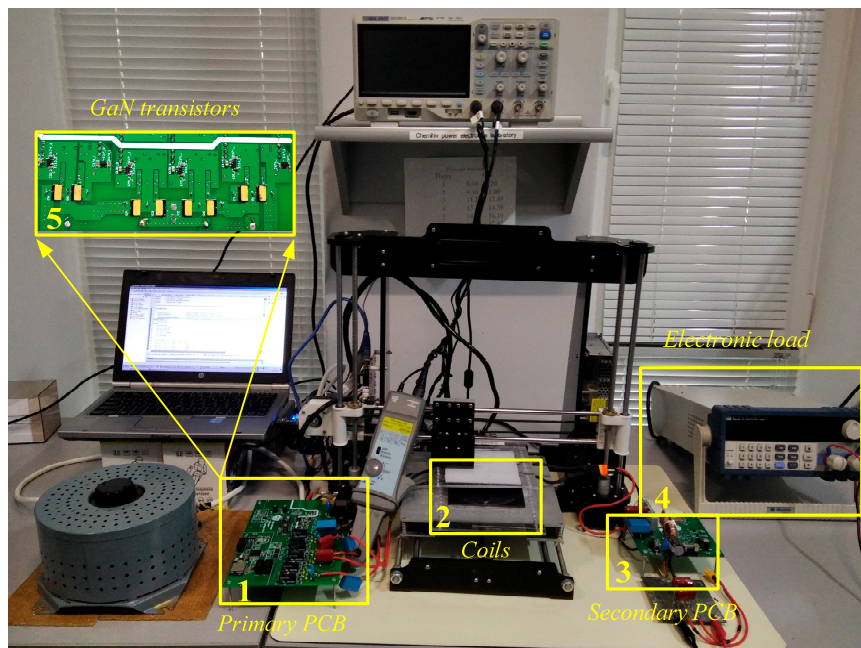
Figure 4. Experimental laboratory GaN-based WPT system: (**1**)—primary side Printed Circuit Board (PCB); (**2**)—transmitting and receiving coils; (**3**)—secondary side PCB; (**4**)—electronic dc load; (**5**)—GaN transistors located on the bottom of the primary PCB.
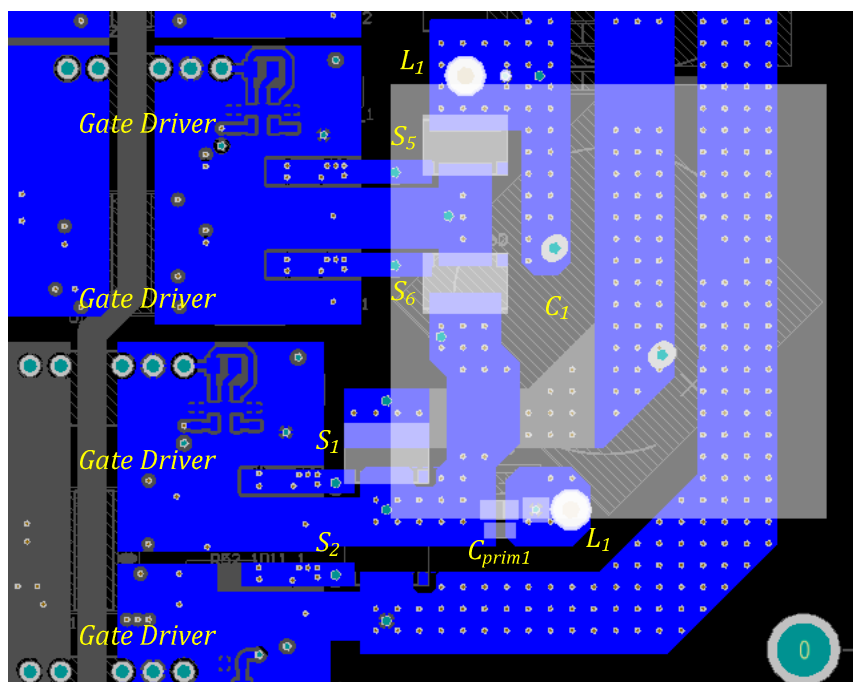

Figure 5. Bottom side of the power part of primary PCB.

The similar square of current loops on PCB are also provided for other switching states, presented in the Table 1. Therefore, such small squares of the current loops in all possible operation modes of the inverter provide low electromagnetic interferences of the power converter, improving EMC of WPT.

The experiments were performed at a distance between the coils of 1 cm (coupling coefficient = 0.9) and at a distance of 2 cm (k = 0.7)—Table 2. The dependences of the output parameters on the operating frequency (150 and 200 kHz) were investigated at different load resistances for each of these distances.

A wirewound resistor was connected for power distribution since the available electronic load has a maximum power of 300 W.

Combinations of the two frequencies described above and the two coupling coefficients were investigated. Figure 6, for example, shows the cases at a coupling coefficient of 0.7.
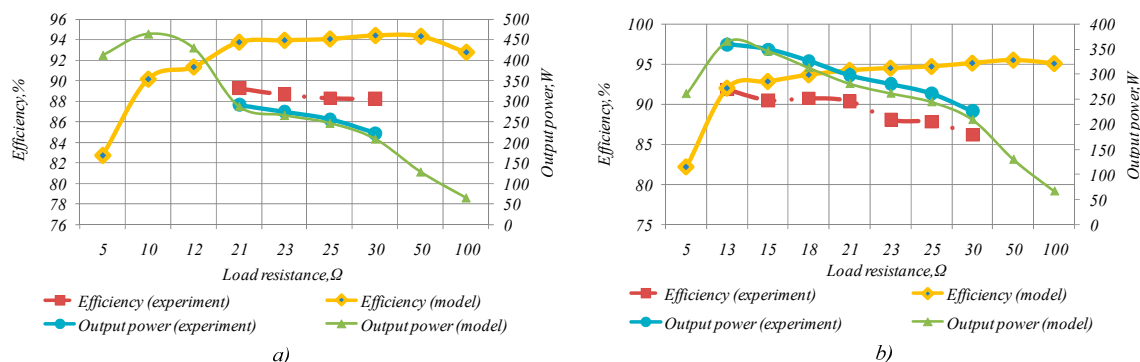

Figure 6. Experimental and simulation dependencies at the load resistance variable at k = 0.7: (**a**) efficiency and output power on the load resistance for f = 150 kHz; (**b**) efficiency and output power on the load resistance for f = 200 kHz.

Figure 6 shows that, in general, the efficiency in the model was slightly higher than in the experiments. However, the experimental efficiency also reached more than 90%. The unevenness of the experimental graphs is explained by the fact that the voltage in the grid can vary constantly during the experiment, while in the model, the desired value is specified.

The investigated maximum transmitted power was 360 W during the experiment under the operating frequency of 200 kHz and load resistance of 15 Ω (Figure 6b). The measured temperatures are shown in Figure 7. The temperature on the transistors surface and coils has almost not changed (40 °C and 42 °C, respectively) during a long-term operation of the circuit at this power. This indicates to the power reserve in these elements (they can withstand more power). The temperature increased to 89 °C on the rectifier diodes. Obviously, the losses in the diodes are the largest of the whole scheme, which confirms the power losses calculations. The heating temperature can be reduced by using a larger radiator or forced air cooling. As a conclusion, the diode losses are the main limitation factor of the further switching frequency increasing.
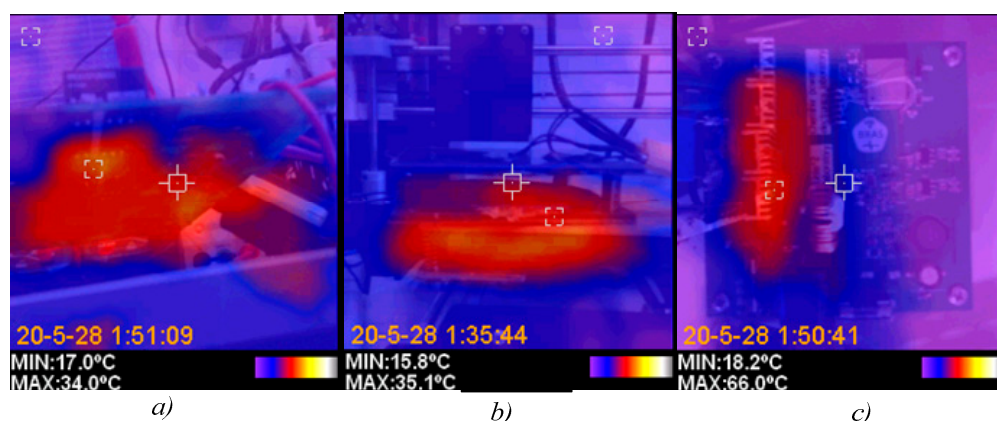

Figure 7. Pictures from the thermal camera at R_L = 15 Ω, k = 0.7, f = 200 kHz, V_{in} = 300 V: (**a**) transistors temperature; (**b**) coils temperature; (**c**) temperature of rectifying diodes.

Large coupling coefficients has been studied to obtain more power (Figure 8). Higher power with a larger duty cycle is of course due to the longer time when the transistors are open and conducting.

The duration of the zero voltage level is minimal under such conditions (Figure 9). The change in the duty cycle has little effect on the efficiency. The dead-time of the transistors was selected taking into account the maximum efficiency of energy transfer. Dead-time in the transistors was set less than 5% of the period.
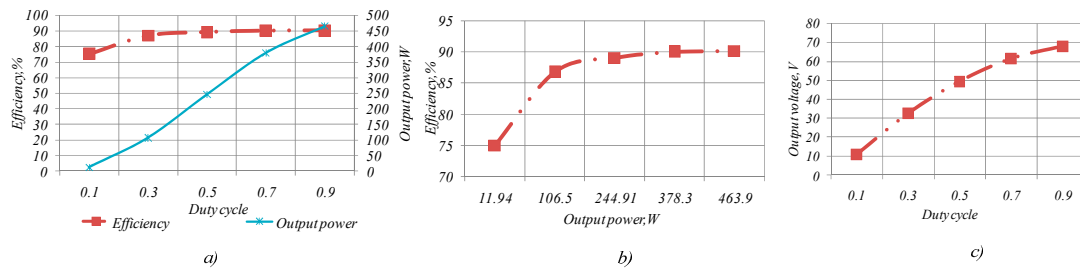

Figure 8. Experimental dependencies at R_L = 10 Ω, k = 0.9, f = 150 kHz, V_{in} = 300 V: (**a**) efficiency and output power on the duty cycle; (**b**) efficiency on the output power with the duty cycle change; (**c**) output voltage on the duty cycle.
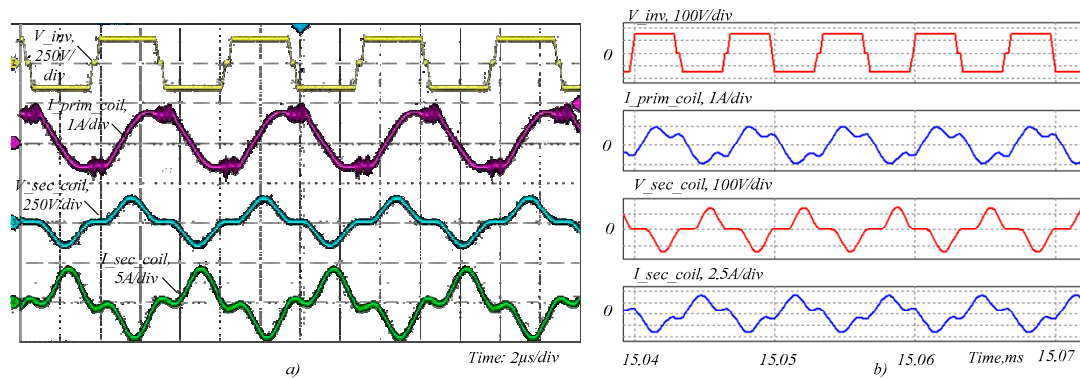

Figure 9. The waveforms on the primary and secondary sides at R_L = 30 Ω, k = 0.9, f = 150 kHz, V_{in} = 300 V: (**a**) experiment; (**b**) simulation.

The shape of the signals in the experiment is shown in Figure 9 for one of the used cases. In particular, the voltage at the output of the inverter (*V_inv*), the current through the primary coil (*I_prim_coil*), the voltage (*V_sec_coil*) and current on the secondary coil (*I_sec_coil*) were recorded.

The shape and the magnitude of the currents and the voltages are very close. The resonance condition is fulfilled.

The influence of the snubber capacity on the power and energy transfer efficiency was also investigated experimentally (Figure 10).
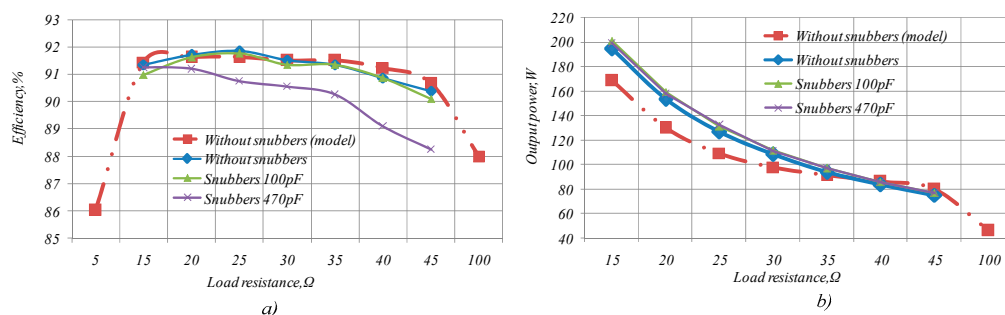

Figure 10. Experimental and simulation dependencies at the load resistance variable at k = 0.9, f = 150 kHz, V_{in} = 300 V: (**a**) efficiency on the load resistance; (**b**) output power on the load resistance.

The snubber capacitance was designed to reduce voltage peaks when the transistor is turned on and off, especially at voltage levels close to critical. Snubber capacitors of different capacities were alternately installed between the drain-source leads of the transistors. The addition of a small snubber capacity in the bridges of the T-type scheme has almost no effect on the energy efficiency (Figure 10a). The effect was more noticeable with an increasing capacitor value and an increasing operating frequency of the transistors.

The distribution of losses is shown at changing the load resistance for the case $k = 0.7$, $f = 150$ kHz, $V_{in} = 300$ V (Figure 11). The circuit model made in PSIM simulation is an exact copy of the experimental circuit. The data were taken from the model to calculate the losses in the circuit elements.
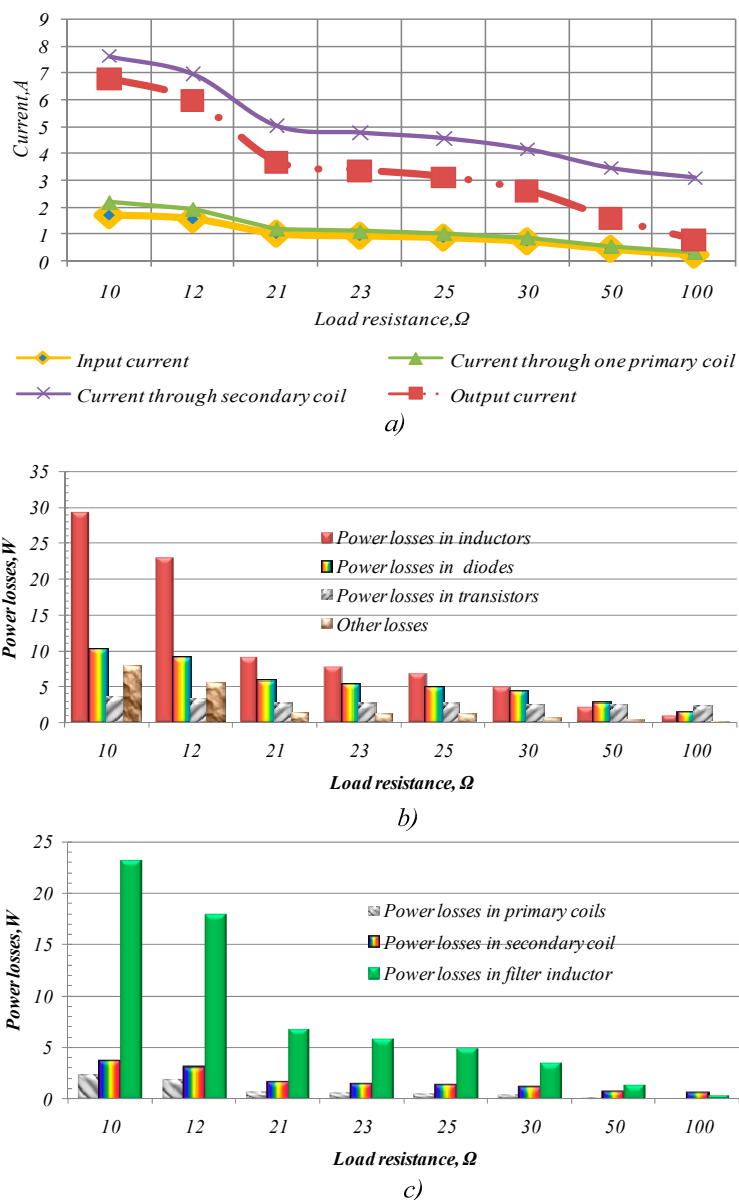

a)

b)

c)

Figure 11. Calculation of power losses at $k = 0.7$, $f = 150$ kHz, $V_{in} = 300$ V and change of load resistance: (**a**) dependencies of currents through elements on the load resistance; (**b**) distribution of losses by major groups; (**c**) power losses in inductors.

The losses in the inductors and diodes are decreasing significantly with an increasing resistance (and hence with a decreasing current: see Figure 11a. Evidence for this is shown in the charts (Figure 11b,c). Other losses are also decreasing with increasing load resistance for the same reasons.

The total power losses in the transistor remain at approximately the same level in this case. It means that GaN transistors do not reach the maximum current, which they can pass through themselves.

The losses distribution in the semiconductor and magnetic components of the circuit for the same case $k = 0.7$, $f = 150$ kHz, $V_{in} = 300$ V at a load resistance of 10 Ω and 50 Ω are compared in more detail in Figure 12. The static losses in the inductors and diodes are significant (predominant) (Figure 12a). The reason is that with less resistance there is more input and output current. The total calculated losses are 84% relative to other losses. This ratio is already 95% in Figure 12 that confirms the statement described in [32]. It can be explained due to a significant decrease in the current value through all elements of the circuit, especially the output current.
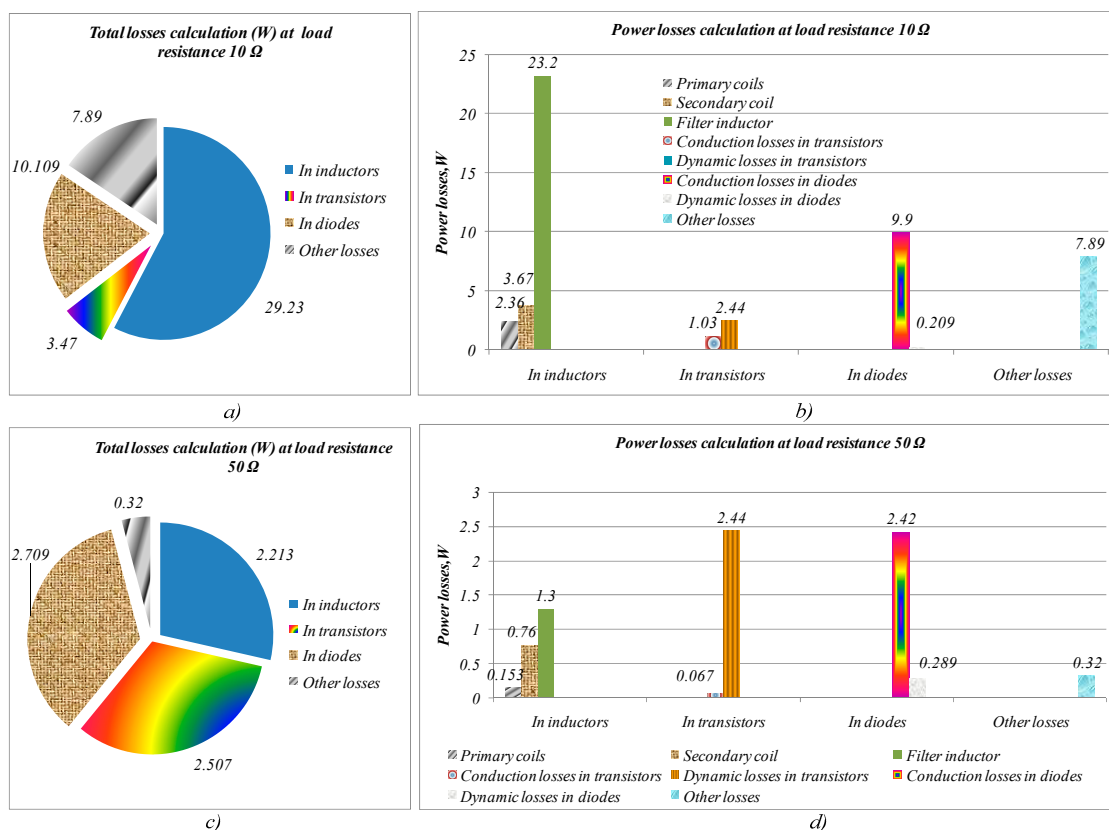

Figure 12. Power losses calculation at $k = 0.7$, $f = 150$ kHz, $V_{in} = 300$ V: (**a**) distribution of losses by major groups for the load resistance 10 Ω; (**b**)detailed distribution of losses for the load resistance 10 Ω; (**c**) distribution of losses by major groups for the load resistance 50 Ω; (**d**)detailed distribution of losses for the load resistance 50 Ω.

The current in the secondary coil is higher due to the lower resistance in the secondary coil and the value of the self-inductance (turns ratio). This causes greater losses compared to the primary coils (Figure 12b,d).

The effect of dynamic losses in the transistor is less noticeable with an increasing transmission power. It means that the contribution of the transistor dynamic losses to the total power losses will be smaller (because they are almost constant due to the large value of P_{oss}).

The dynamic losses of the diode are not significant (Figure 12b,d). They are dependent on the change of output voltage and the operating frequency according to the expression (15) and do not depend on the current.

In summary, in this topology and these transistors, it is possible to obtain an efficiency of up to 95% and a power greater than that shown in this article. This requires very accurate instruments for measuring data and more careful selection of rectifier diodes.

6. Conclusions

The paper analyzes the feasibility of utilizing of GaN transistor in the three-level T-type NPC inverter with two coupled transmitting coils for WPT. The promising T-type topology of the inverter was selected because of the advantages described in the paper over the classical solutions.

To study the system operation, a detailed analysis of the calculation of static and dynamic losses in the transistors and rectifier diodes and static losses in the inductors was conducted. A series of experiments followed, focused on changing different input and output parameters and calculated power losses in the magnetic components and semiconductors. It was established that the greatest losses have concentrated in the magnetic components and rectifying diodes. These losses are mainly of conduction nature, caused by the significant current through these elements. At the same time, the total losses in the transistors are the smallest compared to all other losses on the circuit elements, which shows that this transistor type is absolutely justified for wireless power transfer in this non-classical circuit. However, these transistors are more critical to overvoltage (surges) on the drain-source than other types of transistors. Due to this fact, the particular attention should be paid to PCB design.

The overall energy transfer efficiency was 90% at the maximum experimentally investigated power of 360 W, which is at the level of industrial samples. The system showed excellent stability at different load resistances and changes in different parameters. At the same time, due to the T-type application, along with GaN transistors, this solution has reduced primary coil and does not have heatsink. It has great potential and can operate at higher power with greater efficiency of wireless power transfer.

7. Patents

Ukrainian patent No. 142050 "Wireless power transfer system based on three-level T-type inverter and two coupled transmission coils".

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