Postprint of: Roncero-Clemente C., Husev O., Matiushkin O., Gutierrez-Escalona J., Barrero-Gonzalez F., Vinnikov D., Strzelecki R., Feasibility Study of Three-Phase Modular Converter for Dual-Purpose Application in DC and AC Microgrids, IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS (2023), DOI: 10.1109/JESTPE.2023.3247960

Feasibility Study of Three-Phase Modular Converter for Dual-Purpose Application in DC and AC Microgrids

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***Abstract*—The modern concept of a universal converter is intended as a power converter suitable for application in both dc or ac grids using the same external connectors. This novel family was recently proposed to allow an easier integration of renewable energy sources and energy storage systems, interfacing with dc/ac grids and/or loads with a minimum redundancy of power switches and passive elements. This kind of solution and applications are expected to be a reality in the nearest decade, as ac and dc low voltage distribution networks will coexist. Nevertheless, the initial solutions proposed as universal converter were focused on ac single-phase power conversion systems. In this sense, this article proposes and describes a new member of the universal converter family suitable for dc to dc and dc to ac power conversion (both in three-phase three-wire and in three-phase four-wire). The proposed power topology is derived as a modular extension from the single buck-boost bidirectional cell. Its main operation modes (buck and boost) are discussed, and a pulse-width-modulation technique is developed to generate the corresponding switching patterns. The proposed solution is successfully validated in open-loop mode both in simulation and experimentally with a laboratory prototype. The measured efficiency of the power converter was above 97% in the dc to ac mode and around 99% in the dc to dc mode.**

***Index Terms*—dc-dc converter, renewable energies, solar converter, three-phase dc-ac converter, universal converter, wide-band semiconductors.**

I. Introduction

MICROGRIDS (μGs) and nanogrids (nGs) are low-scale electrical networks entailing modern equipment as high-efficient power converters (PCs). These PCs allow an optimal exploitation of both energy sources (mainly derived from renewables) and energy storage systems (ESSs) in a local way. Existing μGs set up mostly emerges from the imperative global challenge about integrating these renewable energy resources (RESs) such as solar, into the energy mix, therefore mitigating CO_2 emissions [1]-[3] and, at the same time, reducing energy transmission losses and cost. μGs and nGs can also behave as a single and controllable agent with respect to the main utility grid if required (islanded performance) [4]. Moreover, they get the great leverage by an optimized operation with the information and communication infrastructures, in order to supply the energy user´ demand in an efficient and clean way [5]. This last issue is coined into the transactive energy concept [6].

Electrical low-voltage (LV) distribution networks have historically been mainly configured by ac technology, as well as the pioneer μGs and nGs (Fig. 1*a*). Nonetheless, a new paradigm is being born since electrical LV dc distribution grids begin to be a reality [7]. Nowadays, we are experiencing an increase of dc equipment related to the aforementioned renewable energy sources and ESSs, and also on the load side, both in residential, commercial and industrial environments. This architecture presents inherent advantages such as an increased efficiency due the lower conversion losses in PCs, an improved reliability and power quality in electrical networks, and a higher grid stability [8], [9]. It also provides an easier connection of dc generators and ESSs (Fig. 1b). dc powered systems are emerging in electric vehicles and their charging stations (mainly in fast chargers) [10], dc household appliances [11], industrial factories [12] and in building dc distribution systems and in dc μGs [13].

Recently, an interesting advantage of the dc distribution scheme is on the bipolar dc configuration [14]. These dc distributions and μG schemes are compatible with the installed three-phase ac cabling with five conductors. This fact can be intended as an easier retrofitting process while maintaining some of the installations and infrastructures. Thus, this new reality invites to think about an era in which ac and dc distribution networks and μGs will coexist (Fig. 1c). This fact

This research was funded by the Junta de Extremadura (Spain) with the project (IB20165) and the program "Ayudas Talento" (TA18003). It was also partially funded by the Estonian Research Council grant PRG675 and by the Estonian Centre of Excellence in Zero Energy and Resource Efficient Smart Buildings and Districts (ZEBE). *(Corresponding author: C. Roncero-Clemente).*

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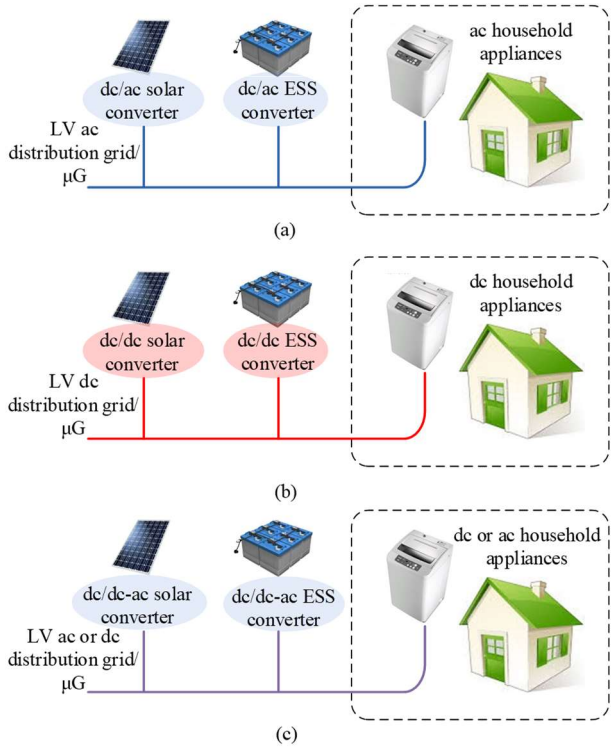

Fig. 1. Schematic representation of possible residential µGs or LV distribution network. (a) ac case. (b) dc case. (c) Merged dc and ac cases.

originates new research topics on this type of grids, and on the associated PCs to ensure a reliable performance. The meeting point of the ac and dc configurations is on the power electronics, considered as the key enabling technology [15]. Several state-of-the-arts review the huge number of dc-dc power converters proposed for different purposes in our framework [16]-[20]. [16] provides a deep comparison of non galvanically isolated high-step-up solar dc-dc converters, focusing on the topologies with high-step-up, low-cost and high-efficiency performance, discussing the pros and cons of the different candidates. If the PC has to interface with electrochemical ESSs, the particular topologies require another features, as for example, the bi-directionality [17], [18]. In other installations involving dc-dc converter, a very high-gain ratio and/or galvanic isolation is required. In this case, the dual-active-bridge (DAB) dc-dc converter is one of the most promising topologies [19]. In order to realize power flow control among solar, ESS and load, the multi-port structure and, in particular, the three-port dc-dc converters are widely used [20].

Some comprehensive reviews about dc-ac topologies also oriented to our framework are highlighted [21]-[24]. On one hand, one of the most relevant circuits used in solar applications is the single-stage buck-boost inverter, due to the ability to increase/decrease the output voltage in a single power stage. [21] provides a recent state-of-the-art of this family of PCs, remarking the pros and cons of each member in a comparative way. In another hand, multilevel inverter solutions have gained popularity in LV level and RESs applications. The high-quality waveforms, modularity, voltage and current scalability and fault-tolerant capability are some of their advantages [22]. At the photovoltaic module level PCs, the microinverters are the solution, and also quite different topologies are used depending on the parameter to be optimized [23]. Finally, multiport solutions also consider ac architectures in some of their ports [24].

At the same time, it is obvious that transitioning from ac to dc grids cannot be achieved immediately. Even if a transition happens, in the near future [25], we will observe a hybrid operation between dc and ac systems, as shown above. Finally, there is no evident business model for investors because they do not see dc appliances. On the other hand, potential investors of dc appliances do not see the sizable market and business cases because of the absence of LV dc grids and are not ready to risk.

Our attention is paid to PC solutions simultaneously suitable for dc and ac µGs [26]. The so-called hybrid converters include both dc and ac terminals involving specific power electronic switches, with the main purpose of integrating the ESSs into a common dc-link by means of the dc terminals. The previously cited family of the multi-port converters allow the interconnection between dc and ac LV distribution networks or µGs [20], [24]. Due the high number of branches in the universal multiphase PC, its use is extended to single-phase ac, multi-phase ac and dc systems [27]. At the residential level, these types of versatile PCs are known as energy routers, with also dc and ac connection capability [28].

A new concept of universal solar PC recently proposed, accept both dc or ac LV grid by the same converter terminals [29]. In this sense, these topologies count with minimal internal redundancy compared to the previous solutions. The possible circuits of the universal solar PC operating with dc or ac are: i) the voltage source inverter derived universal dc-dc/ac converter, ii) the buck-boost derived universal dc-dc/ac converter and iii) the buck-boost converter with unfolding circuit as universal dc-dc/ac converter. The change between dc-dc or dc-ac conversion just depends on the control strategy and the modulation.

A. Motivation and Main Contributions

The coexistence of dc and ac distribution networks and facilities is becoming a reality. Thus, dual-purpose PCs [29] were born as transition technology to facilitate the integration of RESs and ESS in any type of grid, aiming at high performance and versatility. The main novelties of this work are highlighted as follows:

- The previous universal or dual-purpose PCs are single-phase in their ac mode. This work goes beyond that single-phase solution by proposing an extension to be operated within three-phase µGs.
- The proposed topology is characterized by its versatility, as it can perform in three-phase µGs with three or four wires.

- A new pulse-width-modulation is developed for a proper switching signal generation of the proposed PCs.

The work is organized as follows. Section II refreshes the universal solar PC concept and discloses the new circuit suitable for dc and three-phase ac μGs. Section III explains step by step both the dc to ac and the dc to dc operation modes, with the corresponding modulation method. Some design guidelines for the passive elements are discussed in section IV. The simulation and experimental verification in open-loop and steady state conditions are conducted in section V and VI respectively. Section VII concludes the paper.

II. Universal DC-DC/AC Converter Concept

An alternative and promising solution for the modern PCs was recently disclosed [29]. Based on the use of the same external connectors or terminals, these circuits can interface with a string of photovoltaic (PV) panels to perform dc to dc or dc to ac power conversion in a separated way. The benefits of the universal PCs underlie the increasing simplicity and modularity of the coexisting dc and ac grids, contributing to the standardization of their power conversion stages. Their structure contains the semiconductor stage, the output filter, the electromagnetic interference (EMI) filter and the protection system, which provides a total flexibility independently to the type of grid the PC is interfacing with. As aforementioned, the change of the power conversion mode just underlies on the change of the modulation and control strategy. The circuits proposed were derived from traditional buck-boost dc-dc converter with unfolding circuit (Fig. 2(a)). It has ability to operate in a wide input voltage range and a minimum redundancy of components to perform the dc-dc and dc-ac conversion. Another possible single-phase solution (Fig. 2(a)) consists of two parallel bidirectional buck or buck-boost converters with common input voltage source. Each of these converters can be regarded as an independent cell. In the conventional dc-ac application, each cell generates a sinusoidal voltage with a dc bias. Due to the phase-shift between cells, pure sinusoidal voltage can be generated between the output terminals.

A similar approach for ac operation was proposed for a three-phase rectifier in [30] and an inverter in [31]. These studies propose two similar solutions referred to as Phase-Modular Converter (PMC) [32]. These solutions were already compared in [33]. The PMC solution may require slightly larger magnetics components and higher losses in ac mode. At the same time, reduced number of semiconductors and interleaved performance in dc mode makes it extremely attractive if dc mode is considered as a main application.

In order to cope with three-phase ac systems, the three-phase derived universal circuit is proposed and shown in Fig. 3 (a). It is composed by three or four identical buck-boost dc-dc bidirectional branches, which can be controlled to produce the required power conversion to supply a three-phase three-wire or a four-wire ac load (Fig. 3 (b) and (c)), to inject power to a three-phase three-wire or a four-wire ac grid (Fig. 3 (d) and (e)) as it was also demonstrated in this work [34] and called like Y-inverter.

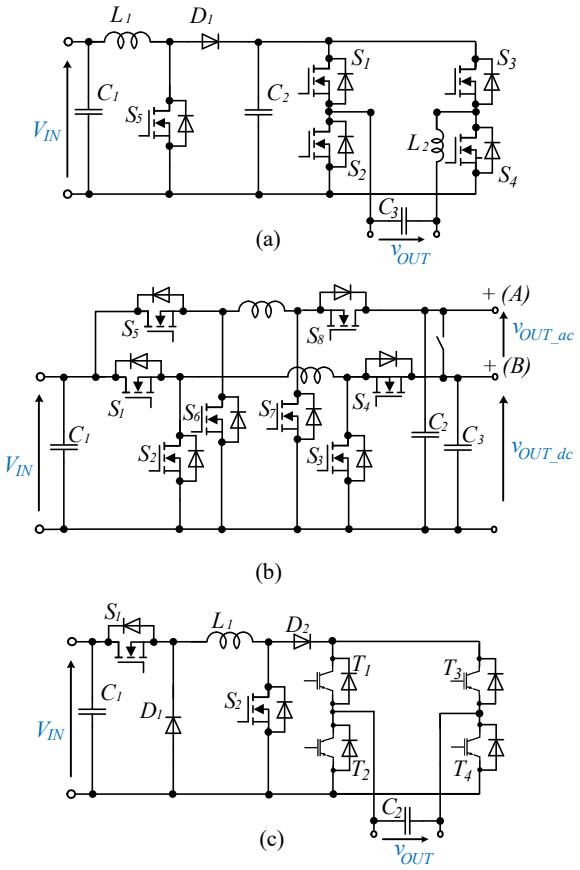

Fig. 2. Single-phase universal PCs: (a) buck-boost with unfolding circuit, (b) buck-boost phase-modular dc-dc derived solution.

This work proposes its further modifications. First of all, in order to provide the operation with the dc grid or load, the converter must have an additional suppressor capacitor C_S and a Solid-State Circuit Breaker (*SSCB*) for very fast disconnection in case of any emergency. In advance to *SSCB* it has two or three additional switches SW_1, SW_2 and SW_3, depending on the availability or not of the neutral wire. Due to these switches, the circuit can be reconfigured to the parallel interleaved operation and can supply a dc load or to inject power to the dc grid (Fig. 3 (f) and (g)). The external ac and dc circuit breakers (CB) can be used to connect only to ac or dc.

The circuit can also perform in reverse power flow mode (behaving as a synchronous rectifier), and also as interface with a bipolar dc grid. Besides the integration of RESs or ESSs into the μGs/nGs, a potential application of the proposed universal three-phase converter may be in the electric vehicle charging infrastructures (especially in fast chargers) [35].

The following section explains its basic operation principle for both the dc-ac and the dc-dc conversion procedure.

III. Operation Principle

The proposed circuit (Fig. 3 (a)) is capable of performing the dc to ac and dc to dc power conversion with the proper switching of its power switches. In order to assure the electrical isolation between the ac and dc distribution networks and their facilities, the dc to ac and dc to dc power conversions are not

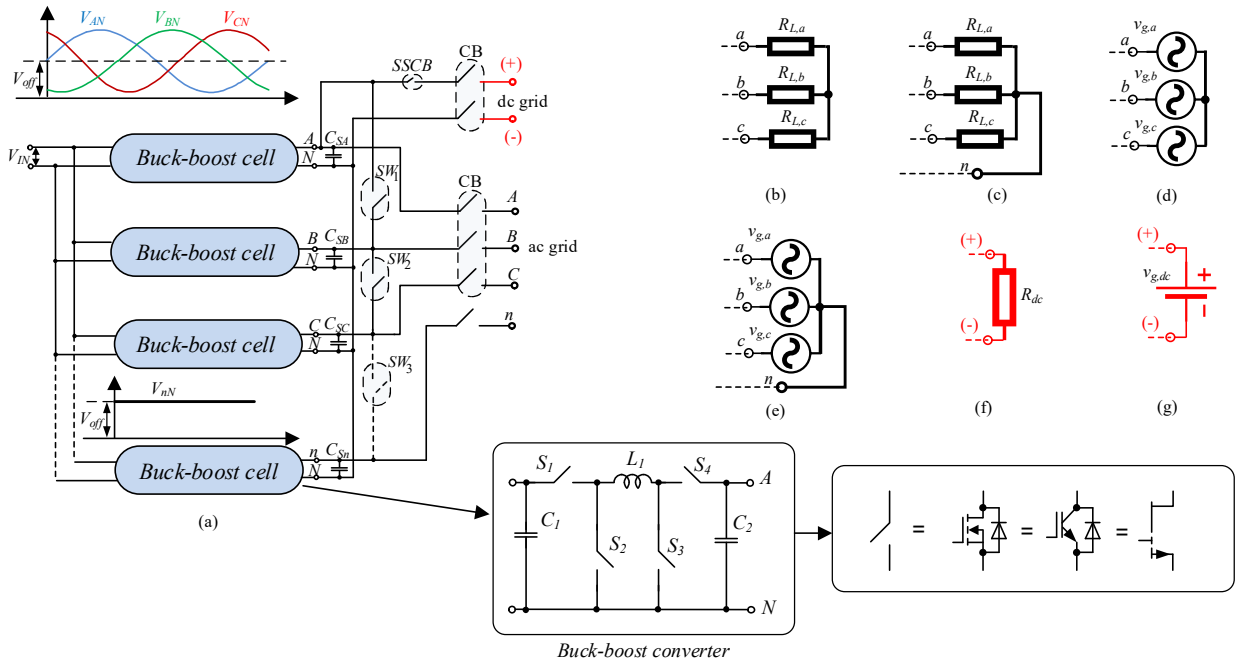

Fig. 3. (a) Proposed dc-dc and dc-ac three-phase universal converter. (b) Three-phase three-wire ac load model. (c) Three-phase four-wire ac load model. (d) Three-phase three-wire ac grid model. (e) Three-phase four-wire ac grid model. (f) dc load model. (f) dc grid model.

performed simultaneously. At the same time, one has to pay attention to the mechanical switches (relays), whose will be in ON position to enable the dc-dc conversion with an interleaving modulation strategy.

A. dc to ac Operation

Each single branch or cell that composes the three-phase converter has to synthetize a dc-biased sinusoidal voltage wave $\hat{V}_{Cf}$because only unipolar voltage is feasible. Each instantaneous reference voltage per phase may be expressed as $v_i^*(t) = V_{off} + \hat{V}\sin(\omega t + \varphi_i)$, where $i = a$, b and c. V_{off} is the dc bias, $\hat{V}$is the peak voltage and ω and φ_i are the angular pulsation and phase respectively. Each phase is $2\pi/3$ radians out of phase with the others. At the same time, the differential dc bias voltage across the load is null. In a case of supplying a three-phase four-wire system, the fourth branch, acting as source neutral-wire, has to synthetize a dc voltage equal to V_{off}.

An overall view to perform the three-phase three-wire dc to ac conversion is illustrated in Fig. 4 (a). Based on different situations of the input voltage V_{IN}, only boost (cyan line, V_{IN3}) only buck (yellow line, V_{IN1}) or alternating buck and boost conversions (pink line, V_{IN2}) are activated. For example, if $V_{in} < V_{off} + \hat{V}\sin(\omega t + \varphi_i)$ then the three cells will operate in boost mode. As the proposed universal three-phase PC can operate by stepping down or up V_{IN}, the alternating buck and boost scenario is highlighted for a general and comprehensive explanation of the modulation technique.

If V_{IN} is higher than the instantaneous value of $v_i^*(t)$, the output voltage is synthetized by working in buck mode. The duty cycle for S_1 (D_{S1}) is given as (note that phase a is selected for description):

$$D_{S1} = \frac{v_a^*(t)}{V_{IN}}, \tag{1}$$

meanwhile S_2 switches in a complementary way. Furthermore, S_3 and S_4 are turned OFF and ON respectively. The output voltage in the other two phases are obtained in identical way. However, if V_{IN} is lower than $v_i^*(t)$, then the voltage boost is activated and the corresponding duty cycle for S_3 (D_{S3}) is expressed as

$$D_{S3} = 1 - \frac{V_{IN}}{v_a^*(t)}, \tag{2}$$

with S_4 operating in a complementary way and S_1 and S_2 turned ON and OFF respectively. The modulation signals (D_{S1}, D_{S3} and carrier with a frequency modulation index equal to 30), and the different gate signals for the phase a (S_{G1}, S_{G2}, S_{G3} and S_{G4}) are illustrated in Fig. 4 (c). This control scheme is compatible with the proposed current closed-loop control system described in [33], devoted to the single-phase grid-connected application.

B. dc to dc Operation

In a similar way than in the dc-ac operation, Fig. 4(b) illustrates the different situations depending on the input voltage V_{IN}, where the boost (blue line, V_{IN} *2*) or the buck (red line, V_{IN} *1*) performance are possible.

An interleaved approach is selected in order to achieve a higher efficiency and an and smaller size of inductors during the dc-dc power conversion. This is a common approach in industrial solutions. The three buck-boost branches are paralleled by means of the electrical connections of relays SW_1 and SW_2. The apparent switching frequency in the dc grid ($v_{g,dc}$) or load (R_{dc}) is three times higher than the individual switching frequency of each leg [40]. Moreover, this redundant

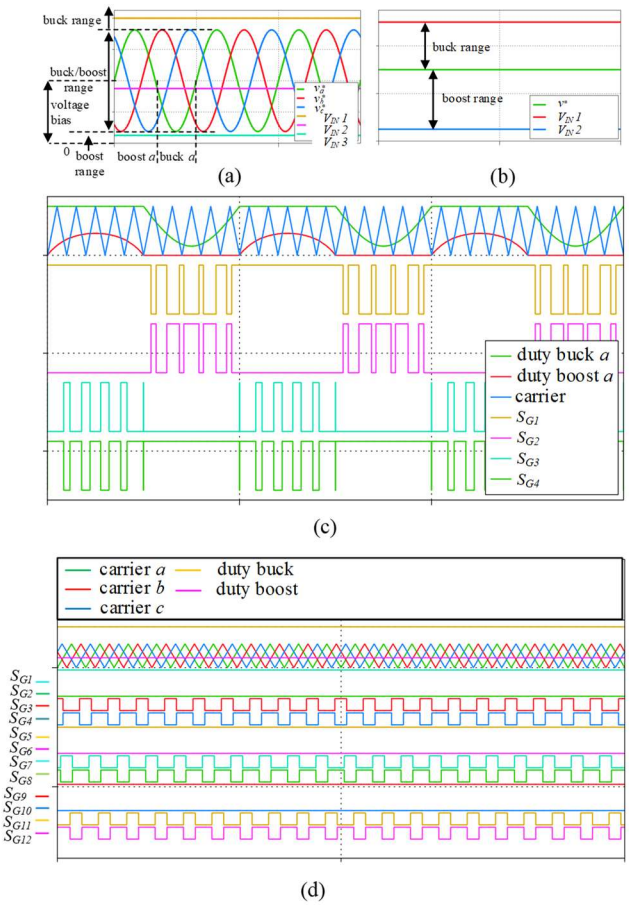

Fig. 4. Modulation schemes during the dc-ac and the dc-dc power conversion with three-paralleled branches. (a) References $v_i^*(t)$ and input voltages V_{IN} in dc-ac. (b) References $v^*(t)$ and input voltages V_{IN} in dc-dc. (c) Switching signal generation for phase *a* during dc-ac. (d) Switching signal generation with interleaving carrier during dc-dc.

configuration makes the system more reliable under the fault operation.

To generate the switching pattern of each paralleled branch, interleaving can be implemented by using the same number of carriers as the number of legs connected in parallel. To achieve an optimal output current spectrum and proper operation, the carriers should be evenly time-shifted within a switching period. In our case, the time shifted is 120°. Note that in a case of four cells with interleaved operation (three-phase four-wire converter in dc-ac mode), then the time shift between carriers would be 360°/4.

The same expressions than (1) and (2) describe the duty cycles of D_{S1}, D_{S3}, D_{S5}, D_{S7} D_{S9} and D_{S11} depending on the buck or boost performance. Note that the reference voltage is a constant value v^* in this case. The corresponding gate signals S_{G1}, …, S_{G12} in a boost case with interleaved carriers are depicted in Fig. 4 (d).

IV. Passive Elements Estimation

According to the Fig. 3 (a) and considering a circuit per-phase analysis of phase *A* during the buck mode of the dc-ac operation, the current ripple Δi_L with power switch S_1 turned ON is expressed as

$$\Delta i_{L,a}^{on} = \frac{(V_{IN} - v_{Cf,a}(t))D_{S1}T_S}{L_a}, \tag{3}$$

where $v_{Cf,a}(t)$ is the capacitor *A* voltage and T_S the switching period. Note that the internal resistance of the inductor L_a is neglected for simplicity. At the same time, considering a lossless system with a transferred power balance $P_{IN} = P_{OUT} = P$ and the equation (1), the expression for the inductance value estimation is solved as follows:

$$L_a \geq \frac{(V_{IN} - v_{Cf,a}(t))(V_{off} + \hat{V})^2}{V_{IN} f_s K_L 2P}, \tag{4}$$

with f_s representing the switching frequency and K_L the inductor current ripple factor and equal to $\frac{\Delta i_{L,a}}{I_{Lmax,a}}$.

In order to estimate the voltage ripple $\Delta v_{Cf,a}$ across the output capacitor $C_{f,a}$, its current flowing through is analyzed. Assuming that the output current is proportional to the capacitor voltage, $\Delta v_{Cf,a}$ can be deduced as:

$$\Delta v_{Cf,a}(t) = \frac{1}{C_{f,a}} \int i_{Cf,a}(t)\, dt = \frac{\Delta i_{L,a}}{8 C_{f,a}} T_S, \tag{5}$$

with $i_{Cf,a}(t)$ as the output *A* capacitor current. Taking the same assumption than in equation (4), an expression for determining the minimum value of the capacitor is:

$$C_{f,a} \geq \frac{V_{IN} - v_{Cf,a}(t)}{8 V_{IN} L_a f_S^2 K_C}, \tag{6}$$

representing K_C the capacitor voltage ripple factor and equal to $\frac{\Delta v_{Cf,a}}{V_{Cfmax,a}}$.

Finally, by doing a similar analysis for the boost mode of the dc-ac operation, the minimum value for inductance L_a and capacitor $C_{f,a}$ can be obtained:

$$L_a \geq \frac{(V_{IN}^2 - (V_{off} + \hat{V})V_{IN})}{f_s K_L P} \text{ and} \tag{7}$$

$$C_{f,a} \geq \frac{P(V_{IN} - (V_{off} + \hat{V})}{(V_{off} + \hat{V})^2 V_{IN} f_s K_C}. \tag{8}$$

Fig. 5 a) illustrates the idealized waveforms of the capacitor voltage and inductor current for a better understanding of the previous analysis and derived equations. Note that a reduced passive element sizing is expected due to the interleaving strategy in the dc-dc operation. Thus, the dc-ac power conversion is considered as more unfavourable case. Fig. 5 b) represents the dependency of the inductor current ripple versus the output voltage magnitude. It is expected to observe a higher ripple during the boost mode for high duty cycles.

V. Simulation Verification

To verify the theoretical statements presented above and the feasibility of the proposed dc-dc and dc-ac three-phase universal converter, a comprehensive simulation study in open loop was performed in PLECS software. As one of the main application fields of this converter family is in the power conversion

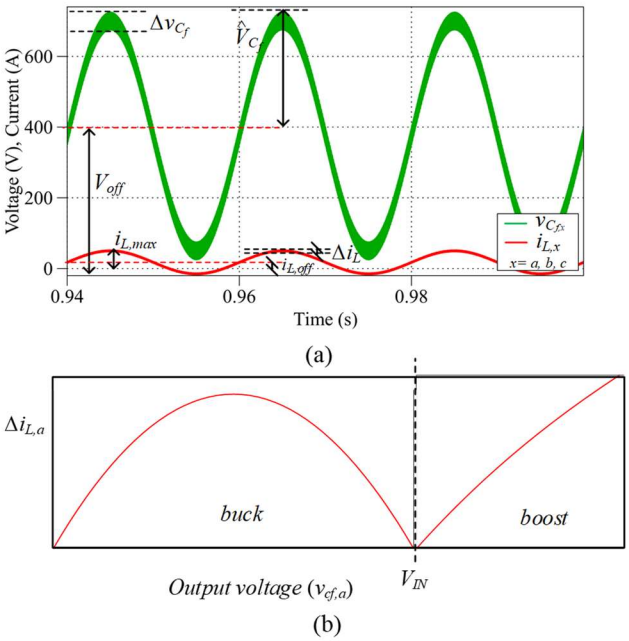

Fig. 5. a) Idealized capacitor voltage and inductor current waveforms. b) Dependency of the inductor current ripple versus the output voltage range.

involving renewable energies, V_{IN} was set to perform in the boost mode both in the dc-dc operation, and in alternating buck-boost mode in the dc-ac operation. The main parameters and values selected for conducting the tests are summarized in Table I.

Fig. 6 shows the most relevant waveforms in the steady state during the dc-ac operation. The voltage and power levels correspond to the rated power of the PC. The sinusoidal output voltages and currents measured in the load ($v_{RL,a}$, $v_{RL,b}$, $v_{RL,c}$, $i_{RL,a}$, $i_{RL,b}$ and $i_{RL,c}$) are depicted in Fig. 6 (a). As expected, the differential dc bias voltage across the load is canceled. Nevertheless, the output voltage in the capacitors contains the dc voltage bias (V_{off}) together with the sinusoidal component to get the expected peak voltage value ($\hat{V}$) around 725 V (Fig. 6 (b)). The output voltage exhibits a higher ripple during the boost mode with the highest voltage magnitude. The inductor currents $i_{L,a}$, $i_{L,b}$ and $i_{L,c}$ are shown in Fig. 6 (c), which also contains a common offset and a sinusoidal component. These currents present a second order harmonic component due to the alternating buck and boost conversion mode in each fundamental cycle. Finally, the instantaneous input voltage (v_{IN}) and current (i_{IN}) are represented in Fig. 6 (d).

TABLE I
MAIN PARAMETERS AND VALUES

Parameter	Value (Size)
Input voltage (V_{IN})	350-390 V
Inductors L_a, L_b and L_c	1.6 mH
Inductor current ripple (K_L)	20 %
Capacitors $C_{f,a}$, $C_{f,b}$ and $C_{f,c}$	1.5 µF
Switching frequency (f_s)	50 kHz
Output peak voltage ($\hat{V}$) (in dc-ac)	325 V
dc voltage bias (V_{off}) (in dc-ac)	400 V
Output voltage (v_{Rdc}) (in dc-dc)	700 V
Load resistances $R_{L,a}$, $R_{L,b}$ and $R_{L,c}$ (in dc-ac)	3 x 47 Ω
Load resistance R_{dc} (in dc-dc)	141 Ω

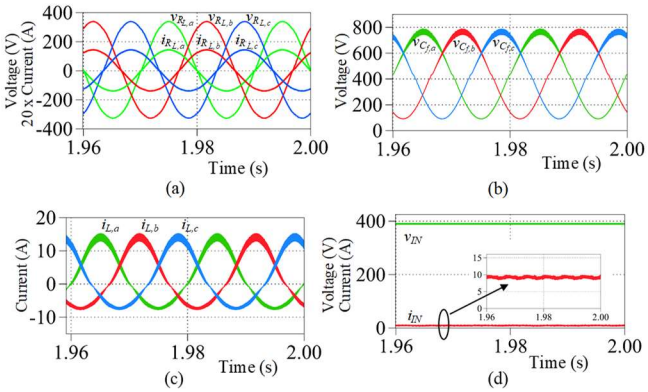

Fig. 6. Main simulation steady state waveforms in the dc-ac mode. (a) Load voltages and currents ($v_{RL,a}$, $v_{RL,b}$, $v_{RL,c}$, $i_{RL,a}$, $i_{RL,b}$ and $i_{RL,c}$). (b) Capacitor voltages ($v_{Cf,a}$, $v_{Cf,b}$ and $v_{Cf,c}$). (c) Inductor currents ($i_{L,a}$, $i_{L,b}$ and $i_{L,c}$). (d) Instantaneous input voltage (v_{IN}) and current (i_{IN}).

The main waveforms in steady state as well during the dc-dc power conversion are collected in Fig. 7. Both the instantaneous input voltage (v_{IN}) and current (i_{IN}) are presented in Fig. 7 (a). It is worthy to note the very low high frequency ripple observed in i_{IN}. This fact is related to the high value of the switching frequency and the applied interleaved strategy in the paralleled branches. This feature would contribute to an increased performance and reliability of the primary energy ES source (PV panels or ESSs). The low high frequency ripple is also appreciated in the zoomed view of the load voltage (v_{Rdc}), and load current (i_{Rdc}) in Fig. 7 (b). The inductor currents in dc-dc conversion ($i_{L,a}$, $i_{L,b}$ and $i_{L,c}$) and their zoomed view (in Fig. 7 (c) and (d) respectively) allow to appreciate the interleaving strategy, where each inductor current is shifted 120° each other.

VI. COMPARATIVE EVALUATION

Before comparison, it is important to underline that there is not direct 3-phase competitor with the same dual-purpose functionality. But, at the same time, the conventional dual-stage

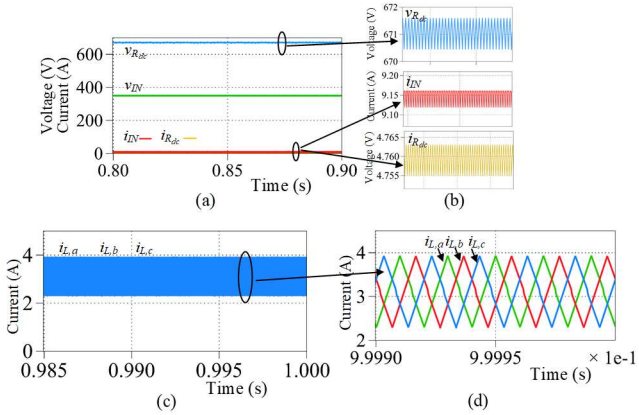

Fig. 7. Main simulation steady state waveforms in the dc-dc mode. (a) Load voltage (v_{Rdc}), instantaneous input voltage (v_{IN}), input current (i_{IN}) and load current (i_{Rdc}). (b) Zoomed view of v_{Rdc}, i_{IN} and i_{Rdc}. (c) Inductor currents ($i_{L,a}$, $i_{L,b}$ and $i_{L,c}$). (d) Zoomed view of $i_{L,a}$, $i_{L,b}$ and $i_{L,c}$.

TABLE II
COMPARISON WITH COMPETITIVE SOLUTIONS

Compared solution	Number of semiconductors	Number of magnetics	Number of capacitors	Isolation
Boost + VSI [34]	8	4	5	no
Universal converter[27]	12	9	7	yes
Proposed solution	12	3	4	no

combination (boost + voltage source inverter (VSI)) can perform this functionality. In fact, it was already compared in the dc-ac operation [34]. It was clearly shown that the proposed solution is better in terms of efficiency and power density. It is also evident that the proposed modification of the Y-inverter is significantly better in case of the dc-dc operation due to the interleaving approach. A second competitor is the universal converter [27]. It has a very wide universality and a galvanic isolation stage. At the same time, many other solutions can be applied, such as impedance-source-converters [42], [43], switched-capacitors based converters [44], [45], or flying inductor/capacitor structures [46], [47]. Nevertheless, most of them were initially designed and optimized for a single-phase application and they will have evident components redundancy for the three-phase application. The simplified comparative analysis which includes a comparison in terms of numbers of the active and the passive components is summarized in Table II. Nevertheless, a comparison in terms of the number of components may be not sufficient, in particular for high power application. For example, an interleaving approach demands more active and passive elements, but allowing a significant losses and converter size reduction.

In this sense, and assuming the same technology for the same type of components, and the same input/output parameters, we can analyze the stored energy in the passive elements. Thus, the volume of the core of the inductor as well as the volume of the capacitor can be estimated based on its maximum stored energy as:

$$Vol_L \cong \sum_{i=1}^{N_L} L_i \cdot \hat{i}_{Li}^2, \tag{9}$$

$$Vol_C \cong \sum_{i=1}^{N_C} C_i \cdot \hat{v}_{Ci}^2, \tag{10}$$

where L_i and C_i are values of i inductance and capacitor, N_L is the number of inductors and N_C is the number of capacitors. $\hat{i}_{Li}$ is the peak inductor current and $\hat{v}_{Ci}$ is the peak capacitor voltage.

At the same time, the relative switching and conduction losses are independent of the selection of semiconductors. The relative conduction losses are proportional to the square of the switch current. As a result, the total conduction losses (CL) can be scaled to:

$$CL \cong \sum_{i=1}^{N_S} \tilde{i}_{Si}^2, \tag{11}$$

where $\tilde{i}_{Si}$ is RMS switch current, N_S is the number of switches.

Neglecting the current ripple, both the semiconductor voltage v_{Si} and semiconductor current i_{Si} influence the hard switching losses [41]. The average value of the product v_{Si} and i_{Si} over a fundamental period T is good measure to indicate the switching losses (SL):

$$SL \cong \sum_{i=1}^{N_S} \left\langle \hat{i}_{Si} \cdot \hat{v}_{Si} \right\rangle_T. \tag{12}$$

Finally, alternatively to the number of semiconductors, we can estimate the total voltage stress across the semiconductors:

$$V_T \cong \sum_{i=1}^{N_S} \hat{v}_{Si}, \tag{13}$$

where $\hat{v}_{Si}$ is the peak voltage across a semiconductor. This parameter is very important and in contrast to the simple number of semiconductors, it may indicate the overall cost of the required semiconductors.

Both in the dc-dc and in the dc-ac modes, the input current ripple is defined by the applied product of voltage and its duration. The nominal values of passive components have to be calculated according to (7) and (8), that satisfy predefined operation in both dc-dc and dc-ac modes. In this sense, the Fig. 8 shows the results of the previous theoretical evaluation. The subfigures consider the relative values of the conduction losses (11) and of the switching losses (12), and the total voltage stress across the semiconductors (13) in each conversion mode (Fig. 8 a) for dc-ac and Fig. 8 b) for dc-dc). In addition, the relative values of the overall size of inductors and capacitors are indicated. All the values are presented in relative units (p.u.) and rated to their maximum values.

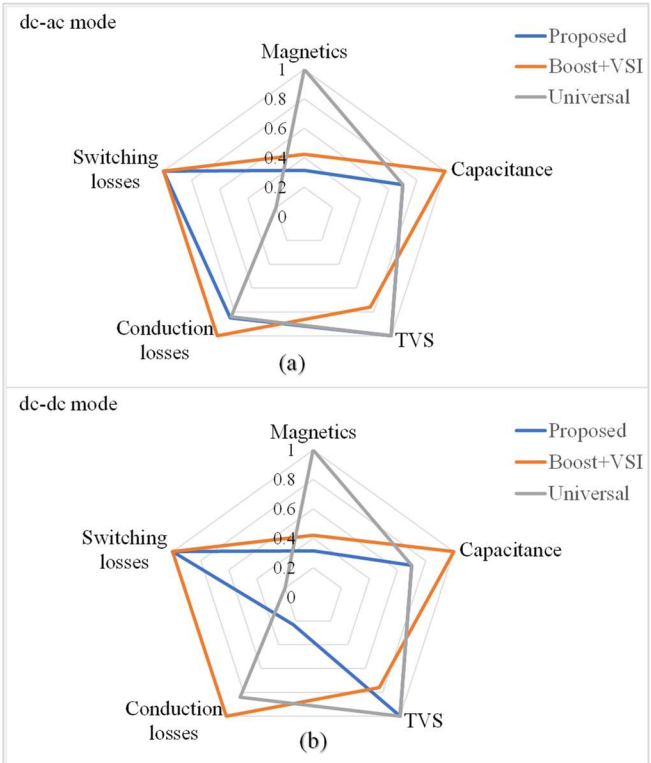

Fig. 8. Comparative evaluation of the proposed solution in dc-ac (a) and dc-dc operation modes (b).

It can be concluded that the proposed solution is very competitive in the dc-ac mode and the best in the dc-dc mode. Despite on the hard switching feature, a very good efficiency and power density are expected mostly due to the interleaved approach and the reduced conduction losses.

VII. Experimental Verification

In order to confirm the preliminary results obtained by simulations, a prototype of the proposed dc-dc/ac universal converter was designed, assembled and tested. The same specification for the passive elements than indicated in Table I, and the same tests than in simulation were planned and conducted.

Fig. 9 shows the experimental laboratory setup. The three-phase universal converter includes as power electronic switches the SiC Mosfet Transistors C2M0080120D. Inductors were designed according to the predefined K_L. The selected core was the ferrite E shape core E70/33/32DG by TDK with a Litz cable wiring. The switching signal generation for the converter were programmed and obtained by using the rapid prototype controller RT Box 1 from Plexim, which is equipped with analogue and digital breakout boards. The system is supplied with a dc input voltage source, the 62000H-S Solar array Simulator from Chroma. The experimental results were obtained by both the PLECS environment through the RT-box 1 and the Tektronix TPS2024B digital oscilloscope with Tektronix P5100A voltage probes and A622 current probes. Finally, the measurement of the efficiency was done in the laboratory with the Newtons4th PPA550 equipment, dedicated for this purpose.

Fig. 10 shows the experimental results in steady state corresponding to the dc-ac mode, similarly to the simulation results presented in Fig. 6. The high-quality sinusoidal output voltages measured in the load ($v_{RL,a}$, $v_{RL,b}$ and $v_{RL,c}$) are depicted in Fig. 10 (a), presenting a total harmonic distortion (*THD*) below than 2.5 %. The load current in phase *a* ($v_{RL,a}$) is also depicted. The theoretical output peak voltage $\hat{V}$ was also achieved, and the differential dc bias voltage is canceled. As expected, the output voltage in the capacitors contains the dc voltage bias together with the sinusoidal component, (Fig. 10 (b)). The inductor currents $i_{L,a}$, $i_{L,b}$ and $i_{L,c}$ shown in Fig. 10 (c) has the same waveform than the simulation waves, including also the common offset and a sinusoidal component. Nevertheless, small differences among the inductor currents ($i_{L,a}$, $i_{L,b}$ and $i_{L,c}$) are appreciated, which are caused by slight differences among load resistances, and the tolerances in capacitors and inductors. Finally, the instantaneous input voltage (v_{IN}) and current (i_{IN}) demanded from the source are represented in Fig. 10 (d). The input current ripple is negligible.

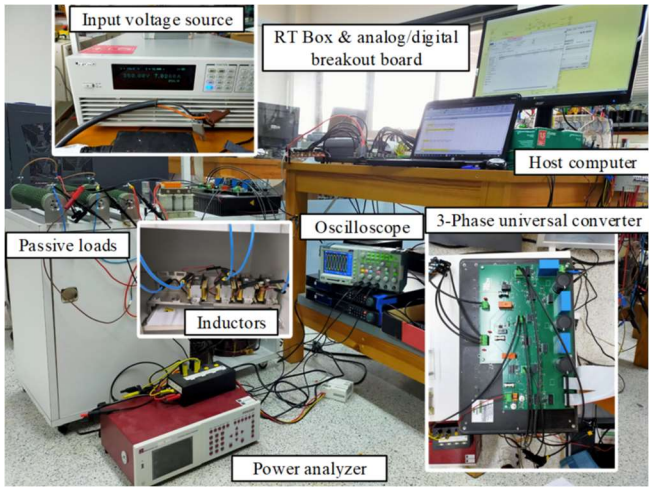

Fig. 9. Experimental setup.

The experimental waveforms in steady state in the dc-dc mode are presented in Fig. 11. The average input voltage (v_{IN}) and the average current (i_{IN}) are depicted in Fig. 11 (a). The average load voltage (V_{Rdc}) and the average load current (i_{Rdc}) are also represented. A very low high frequency ripple is observed in i_{IN}, even lower than in the dc-ac mode. The reason underlies on the high switching frequency and the interleaved strategy switching strategy implemented in this mode. A detailed instantaneous view of v_{IN}, v_{Rdc}, i_{IN} and i_{Rdc} is displayed in Fig. 11 (b). The experimental average inductor currents in dc-dc conversion ($i_{L,a}$, $i_{L,b}$ and $i_{L,c}$) and, in particular, their instantaneous zoomed view allow to appreciate the shifted high frequency ripple due to the interleaved modulation (shifting of 120° each other). These corresponding waveforms are shown in Fig. 11 (c) and Fig. 11 (d) respectively.

Finally, the dc-dc and dc-ac three-phase universal converter efficiency was measured in different input voltage (v_{IN}) and input power (P_{IN}) points. The Newtons4th PPA550 equipment was used to measure efficiency while mathematical calculations along with thermal measurements were used for the losses breakdown analysis. A thermal picture of the power board (detailed in Fig. 12 (a)) during experimental testing at 3 kW is displayed in Fig. 12 (b), corresponding with the dc-ac operation. It can be seen that the average temperature is around 21 ºC, that corresponds to the room temperature and a proper system operation. The hottest points (around 36 ºC) are located at the auxiliary power supplies.

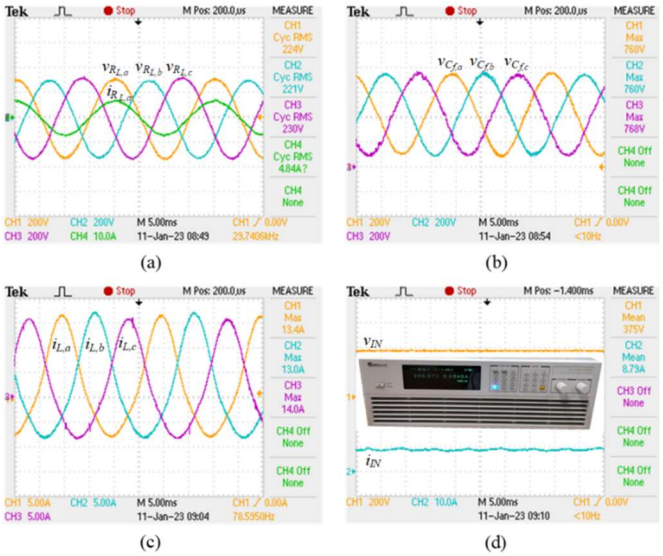

Fig. 10. Main experimental steady state waveforms in the dc-ac mode. (a) Load voltages and phase *a* current ($v_{RL,a}$, $v_{RL,b}$, $v_{RL,c}$ and $i_{RL,a}$). (b) Capacitor voltages ($v_{Cf,a}$, $v_{Cf,b}$ and $v_{Cf,c}$). (c) Inductor currents ($i_{L,a}$, $i_{L,b}$ and $i_{L,c}$). (d) Instantaneous input voltage (v_{IN}) and current (i_{IN}).

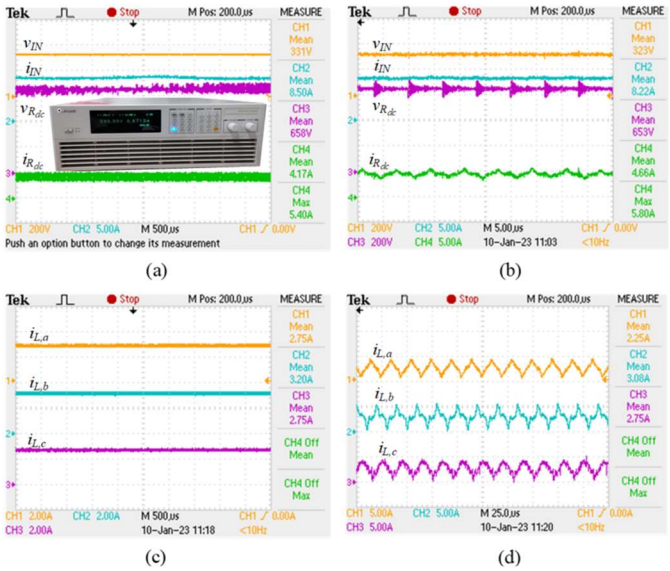

Fig. 11. Main experimental steady state waveforms in the dc-dc mode. (a) Averages load voltage (v_{Rdc}), input voltage (v_{IN}), input current (i_{IN}) and load current (i_{Rdc}). (b) Zoomed instantaneous view of v_{IN}, v_{Rdc}, i_{IN} and i_{Rdc}. (c) Inductor currents ($i_{L,a}$, $i_{L,b}$ and $i_{L,c}$). (d) Zoomed instantaneous view of $i_{L,a}$, $i_{L,b}$ and $i_{L,c}$.

The first efficiency test is focused on different input voltage operation points, but maintaining constant the delivered power (around 3 kW). Note that for the efficiency study, the power was increased significantly compared to the previous simulation and experimental results. In order to maintain a constant power, the duty cycles both in dc-ac and in dc-dc modes were changed accordingly. The efficiency curves are presented in Fig. 13 (a). The obtained efficiency in the dc-dc mode is higher than in the dc-ac, due to the optimized and reduced high frequency ripple thanks to the interleaved parallel operation. The maximum efficiency measured was almost 99 % and 98 % in the dc-dc and the dc-ac mode respectively. The swept input voltage interval allowed to cover points in boost and in buck mode.

The second efficiency test analyses different operation points with different delivered power while maintaining constant the duty cycles. The better efficiencies were obtained closed to the nominal power of the converter, around 3 kW. It is a common approach for selecting the semiconductors and achieve the maximum efficiency at the nominal point [43]. Again, the maximum efficiency was similar than in the previous tests. The efficiency values are collected in Fig. 13 (b). Finally, the losses distribution analysis is presented in Fig. 13 (c). It can be seen that the absence of the double frequency ripple in the dc-dc mode reduces losses in all components. Also, it should be noticed that the impact of SSCB and relays on the overall efficiency is negligible.

Fig. 12. Thermal performance: (a) power board, (b) thermal image of the converter in the ac mode.

VIII. Conclusion

This paper has presented a new member to the universal converter family, being suitable for the dc and the three-phase ac applications. The topology is derived from the phase-modular buck-boost branch concept used to propose one of the single-phase universal solutions. The corresponding modulation methods and operation modes were properly developed for the

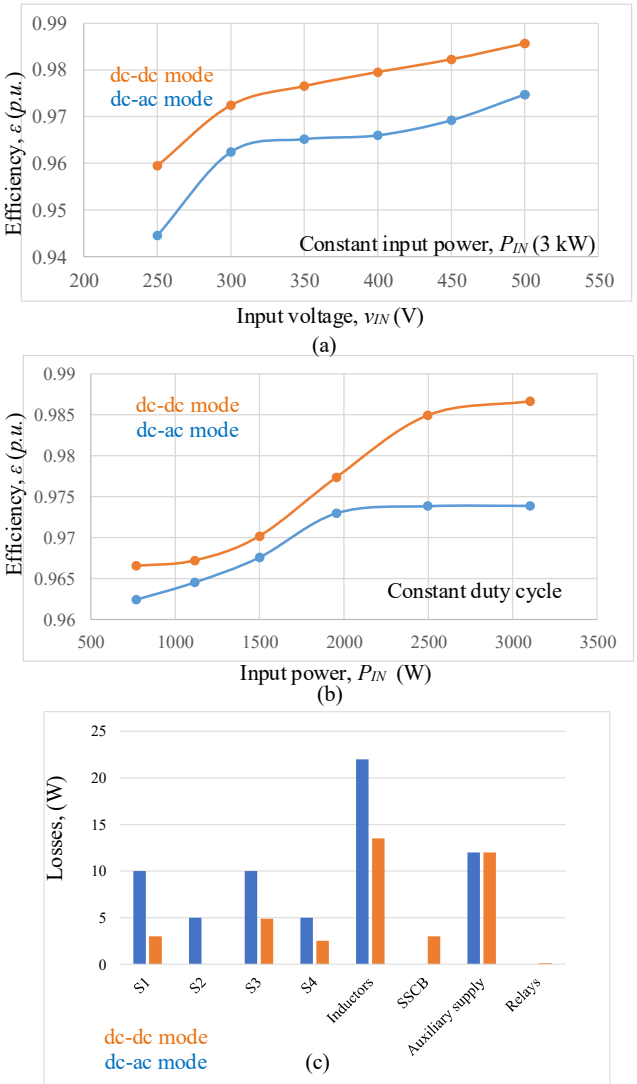

Fig. 13. Efficiency analysis: (a) efficiency versus input voltage with constant input power in ac and dc mode, (b) efficiency versus input power with constant duty cycle, (c) losses breakdown analysis at 3 kW in dc-dc and dc-ac modes in case of 350 V input voltage.

buck and boost cases in the dc-ac and dc-dc operation, considering an interleaving approach to optimize the efficiency in the dc-dc application. The system has shown a proper performance according to the theoretical hypothesis, which are verified by simulation and experiments, achieving an efficiency above 97 % in ac and almost 99 % in dc depending on the power conversion. The universal PC solution is considered quite promising due to its versatile use in the present context with both dc or ac resources, loads and distribution systems. Due to the absence of double frequency ripple in dc mode, the power can be doubled, which in terns means that charging/discharging can be done 2 times faster if a battery storage application is considered.

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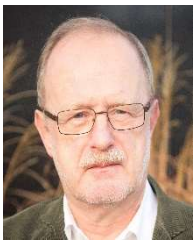

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