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Gate Driver with Overcurrent Protection Circuit for GaN Transistors

Abstract. *The improvement of the gate driver for GaN transistor is presented in this paper. The proposed topology contains the overcurrent protection with the two-stage turning off and independent control of turn on and off time of the GaN transistor. The operation of driver and its application in the half-bridge converter are described using both simulation and prototype measurements. The overcurrent protection was tested in Double Pulse Test (DPT) conditions.*

Streszczenie. *Poniższy artykuł prezentuje zaawansowany sterownik bramkowy do tranzystorów mocy GaN. Proponowane rozwiązanie zawiera zabezpieczenie nadprądowe/przeciwprzeciążeniowe z dwustopniowym wyłączaniem oraz umożliwia niezależne ustawienie czasu włączenia i wyłączenia tranzystora. Działanie sterownika zostało zbadane symulacyjnie i doświadczalnie w układzie przekształtnika półmostkowego. Proponowane zabezpieczenie tranzystora zostało przetestowane w warunkach podwójnego pulsu z obciążeniem indukcyjnym (DPT).* ***(Sterownik bramkowy wraz z obwodem zabezpieczającym dedykowany do tranzystorów mocy GaN)***

Keywords: Wide Bandgap semiconductors, GaN transistors, power transistors, overcurrent protection, SMPS, gate circuit
Słowa kluczowe: półprzewodniki szerokoprzerwowe, tranzystory GaN, tranzystory mocy, zabezpieczenie przeciwprzeciążeniowe, układy impulsowe, obwód bramkowy

Introduction

Nowadays, achieving high efficiency, power density and reduction of overall weight of power electronics devices is the main researcher's topics [1]. The main merits of Wide Bandgap (WBG) devices are low on-state resistance, small inter-terminal capacitances, ability to operate at the high temperature and extremely low switching times (ns-range). All those factors allow to break the limits appointed by the state-of-art Silicon transistors. The subsequent issue is the protection of short-circuit current (SCC) which can lead to thermal and/or electrical damage of semiconductor. The SCC operation depends on the inductance in power stage, gate voltage and voltage of DC-Bus (V_{DC})[2]. The 600 and the 650 V - class GaN transistors have very stable short-circuit (SC) response and relatively large withstand time for V_{DC} below 300 V. For voltage in the range above 400 V the SC withstand time is on the level of hundreds of nanoseconds[3, 4]. Thus, the properly fast protection of WBG semiconductors has a significant impact and should be considered for power converters.

Production process of GaN HEMT transistors is constantly developed. The basis and the simplest technology ensure best performing GaN transistor, however, device structure is "normally-on". In "normally-on" devices negative gate voltage should be apply to switch it off. Moreover, without driving voltage permanent state is "on" and that might cause failure of whole device or system (e.g. short-circuit). Due safety of operation power converters it is recommended to apply normally-off device. Currently there are available three types of "normally-off" GaN Transistor: Enhancement-Mode GaN Transistor (e-HEMT), Gate Injection Transistor (GIT) and Cascode GaN Transistor. Their specific parameters are rather different: gate threshold voltage of e-HEMT is relatively low, GaN GIT transistor is characterized by large current flowing in gate circuit, which is required to switch device and ensure trustworthy on-state and cascode GaN has wide range of gate voltage and low gate charge, however in the structure occur parallel diode. The above mentioned features entail considerable difficulty to propose universal gate driver suitable for all GaN transistors.

In this paper, universal gate driver with the overcurrent protection circuit (OCP) is developed to control and protect the GaN transistor under short circuit current and fault overcurrent conditions. The organization of paper is as follows: in section II project and main features of developed gate driver are presented. Section III provides informations about protection circuit. The structure, simulation and experimental results of driver and OCP circuit are shown in section IV. Section V provides conclusions.

Gate circuit

The important requirements for the WBG semiconductors are short rise and fall time of gate-source and drain-source voltage, the minimal propagation delay and insulation between control signal and gate-source voltage. The recommended asymmetry of the control voltage for wide band-gap devices eliminates the typical drivers of silicon transistors. It is important to assure suitable voltage level during the turn on and turn off, because it depends on the switch structure what is the consequence of different thresholds. Moreover, the value of positive voltage impacts on the transistor channel resistance and conducted power losses. The improper negative voltage can cause uncontrolled switching on of the transistor. For high frequency operation ($f_s \geq$200 kHz), the driver output current should be significantly high in order to fast reload transistor capacitances.

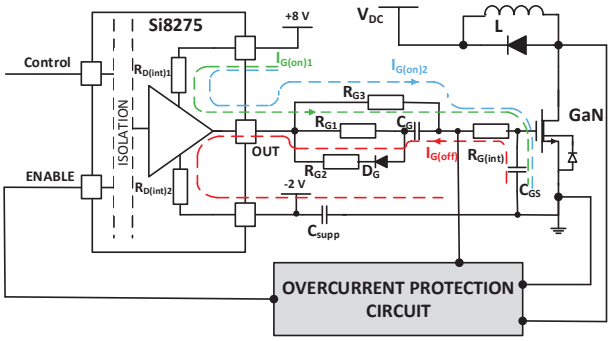

Fig. 1. Entire gate driving system

The main component of presented driver is the integrated circuit Si-8275 form the Silicon Labs, which allows to independent control of two power switches. The Si-8275 isolator provides isolation up to 2.5 kV, possibility to separate pull-up/down outputs with the same or separated grounding and to reduce variation with age or temperature. It allows to obtain the rise time equals 7 ns, the fall time in the range between from 9 to 13 ns. The important parameters of Si-8275 integral circuit are presented in Table 1. The input ENABLE allows to control operation of the integrated circuit by an external signal. The gate circuit of the silicon transistors contains only one resistor which limits the gate current during turn on and off or forward operation. In the WBG gate cir-

cuit, it is necessary to fix the different current for turn on and turn off using extended gate circuits [5]. The connection and conducting track should be as short as possible in order to assure the minimal parasitic inductances. The gate circuit for GaN transistor presented in this paper is shown in Figure 1.

Table 1. Si-8275 main parameters

Parameter	Unit	Value
Input voltage supply	[V]	2.5÷5.5
Output voltage supply (between - and +)	[V]	4.2÷30
Maximal output current	[A]	4
Maximal propagation delay	[ns]	60
Output rise time	[ns]	16
Output fall time	[ns]	18
$\mathrm{d}V/\mathrm{d}t$ immunity	[kV/μs]	200
High output resistance	[Ω]	2,7
Low output resistance	[Ω]	1,0

The dedicated gate circuit includes three resistors R_{G1}, R_{G2}, R_{G3}, capacitor C_G and Schottky diode D_G. The internal gate $R_{G(int)}$ and driver $R_{D(int)1}$, $R_{D(int)2}$ resistances have negligible influence on switching . The turn off process is control by the R_{G2} resistor, despite the Si-8275 has not separated outputs. The turn off starts when gate-source is negative polarized. The current $I_{G(off)}$ starts to flow through the resistance $R_{G(int)}$, $R_{D(int)2}$, the serial capacitor C_G and the turn off equivalent resistance define as parallel connection of R_{G1} and R_{G2}. The gate capacitance C_{GS} is discharged. The time constant of turn off circuit is equal:

$$\tau_{off} = C_{GS} \cdot \left(\frac{R_{G1} \cdot R_{G2}}{R_{G1} + R_{G2}} + R_{G(int)} + R_{D(int)2}\right) \tag{1}$$

The positive voltage initiates the turn on process. The current $I_{G(on)1}$ flows from the integrated circuit through resistor R_{G1}, serial capacitor C_G to the transistor and its internal resistance $R_{G(int)}$. The gate-source capacitance charges with time constant:

$$\tau_{on} = C_{GS} \cdot (R_{G1} + R_{G(int)} + R_{D(int)1}) \tag{2}$$

When the gate voltage V_{GS} is higher than the threshold V_{th}, the transistor channel is opened. When transistor conducts, through resistance R_{G3} flows the slight current (about few mA) which aims to ensure the safe operation of the GaN transistor. The proposed driver has independent adjustable positive (0 ÷ 20 V) and negative (0 ÷ -5 V) output voltage which is applied to the gate of the transistor (minimum value between positive and negative voltage is 4.2 V). This property along with expanded gate circuit allows to drive all types of GaN transistors.

Overcurrent protection circuit

During typical operation of the transistor, unwanted phenomena like short circuit or overload may happen causing damage of devices. The driver should be equipped with failure managing. There are three typical measurement methods:

- using auxiliary resistor in power branch with additional power losses and extension of the current flow path.
- using parasitic inductance of transistor with auxiliary electrode Kelvin source.
- directly measurement of drain-source voltage (desaturation method), where it can achieve high value dangerous for failure managing system devices.

The proposed solution is based on the desaturation method (by direct measurement of V_{DS}). The protection setup consists of three main parts: sensing circuit, ultra fast comparator and signal processing circuit. Sensing circuit is leaned on [6, 7, 8, 9] and consists of three resistors (R_1, R_2, R_3), two diodes (D_1, D_2) and a measuring capacitor C_1. It is recommended that the discrete elements should be produced in SMD technology and the connection layout must be well designed and optimized. Moreover, it is necessary to use fast diodes with as small as possible parasitic capacitance. Above-mentioned rules result minimum delay of sensing circuit. During ON-state of the transistor diode D_1 is forward biased. In this condition the measuring capacitor C_1 is charged up to the level equal to the sum of drain-source voltage and the diode D_1 voltage drop ($V_{C1} = V_{DS} + V_{D1}$). When the transistor is turned-off capacitor is discharged with a time constant equals:

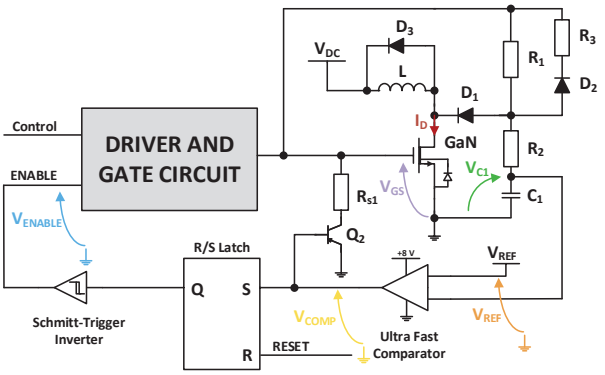

Fig. 2. Overcurrent protection circuit

$$\tau_{scc} = C_1 \cdot \left(\frac{R_1 \cdot R_3}{R_1 + R_3} + R_2\right) \tag{3}$$

In case, when the transistor current increases, the voltage V_{C1} also increases corresponding to the output characteristic of transistor and if it reaches the value higher than V_{REF} then signal from comparator is send to R/S Latch. The positive comparator output signal drives the switch Q_2 and the first stage turn off process starts. Simultaneously the signal ENABLE is pulled down by the Schmitt trigger and the Si-8275 driver goes into the idle state causing a hard turn off of the transistor. The value of blanking time in sensing circuit ensure for selected elements equals 330 ns which ensures safe transistor switching in typical operation (turn on time should be less than 200 ns) and enables operation of a converters with frequency up to 1 MHz.

Simulation and laboratory tests

In order to validate the driver operation, the prototype of half-bridge (phase-leg) converter was built using GaN transistor (GaN Cascode HEMT - Transphorm TPH3207WS) and loaded by inductor 5 mH. Inductive load with the parallel SiC Schottky diode allow attaining relatively large drain current in the Double Pulse Test (DPT) conditions of hard switching with zero and defined current during first pulse.

First, the simulation in LTspice was preformed using the SPICE models of semiconductors provided by its manufacturer. In DPT conditions, the circuit was fed from 400 V DC voltage source and the reference voltage in overcurrent circuit was set to 4 V, which should trigger the protection for drain current equal to 60 A. The simulation results are presented in Figure 3. The voltage V_{C1} depends on the value of drain current and when it reaches the reference voltage value, first-stage turn off starts (in branch R_{s1} and Q_2) and then the signal ENABLE turns off the Si-8275. In consequence, the transistor is turned off before driver changes out-

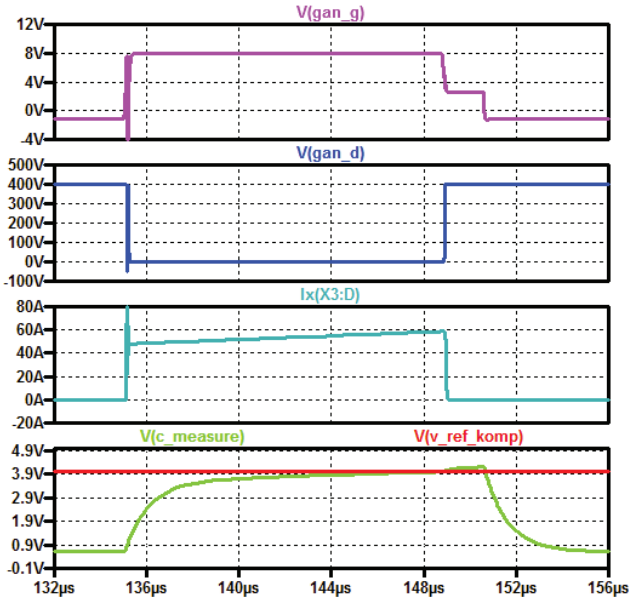

Fig. 3. Overcurrent protection circuit waveforms from LTspice simulation (from the top to bottom): V_{GS}, V_{DS}, I_D and V_{C1} , V_{ref}.

put state from on to off. However, the design of the OCP circuit must be carried out very precisely with retaining several rules:

- R_{s1} should be much smaller than R_{G1} to ensure reliable acting of OCP circuit.
- Diodes D_1 and D_2 should be the ultra fast diodes with extremely low capacitance.
- Comparator, R/S Latch and Schmitt Inverter should have the propagation delays as small as possible .

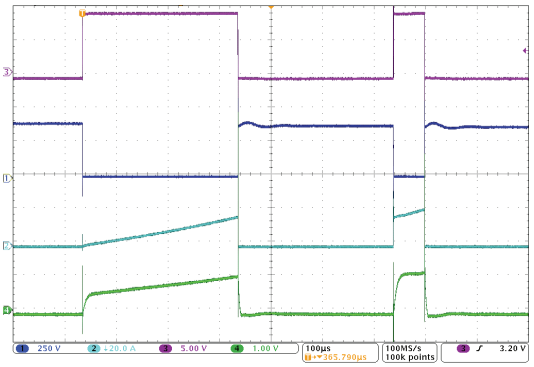

Fig. 4. Measured DPT waveforms - typical operation of the converter: (from the top to bottom): V_{GS}, V_{DS}, I_D , V_{C1}.

The experimental setup (shown in Figure 5) was tested with the DC input voltage in the range 400 V up to 600 V and the OCP circuit reference voltage was set to 1,21 V. The typical operation of the converter (without the active overcurrent protection and DPT) has been investigated - Figure 4. During normal operation, the OCP is enabled but is not triggered, only capacitor voltage V_{C1} is changing, but it is lower than the reference signal. When the transistor is in the off-state, the V_{C1} voltage is equal to zero , whereas during the transistor is turned on, the V_{C1} voltage is rapidly changed to the value equal to the voltage drop on D_1 (measured 500 mV) and further the voltage changes are related with increase of the drain-source voltage as a result of the drain current flow.

In order to activate the overcurrent protection, the converter was fed from 400 V DC voltage, and DPT pulses were set to 350 μs / 70 μs. It allows to rise the drain current up to 25 A, which causes about 720 mV of the voltage drop across

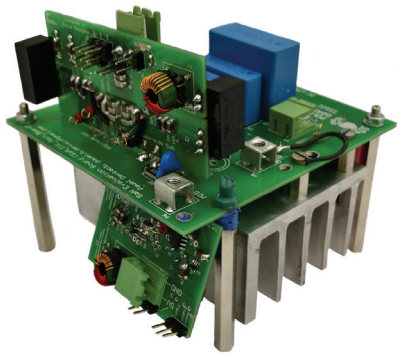

Fig. 5. View of the experimental converter

the GaN transistor. The obtained value of V_{DS} plus the voltage drop on conduction diode D_1 entail exceed OCP reference voltage and rapid triggered of protection circuit. The minimal value of reference signal is determined by the voltage V_{D1}. For turning back on after the OCP turns off the driver, the signal RESET in R/S latch should be set to high level (5V) for a short time. The recorded signals are presented in Figure 6. The two stages of reducing gate-source voltage can be observed: first, it is corresponding with Q_2 turn on circuit (to maintain V_{GS} below the threshold value) and second as the result of driver's state change as it is detailed in Figure 3. The results from measurement agree with ones from the simulation, however an additional oscillations appear which are the result of the existence of parasitic in the converter layout and the high value of $\mathrm{d}v/\mathrm{d}t$ and $\mathrm{d}i/\mathrm{d}t$ in drain branch. The interference caused by high $\mathrm{d}v/\mathrm{d}t$ in power circuit could trigger the OCP. In order to avoid crosstalk of the signals, the OCP circuit should be designed properly maintaining the suitable large distance between the circuits. In the presented driver the OCP was not triggered by noise during the laboratory test.

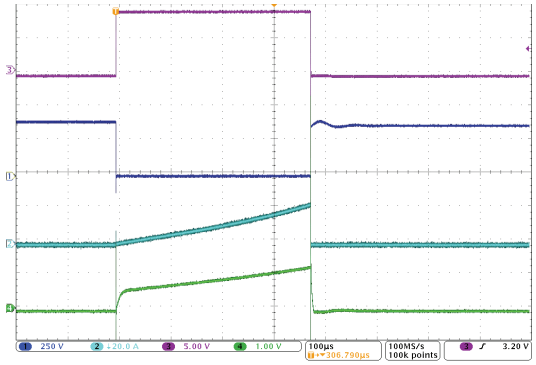

Fig. 6. Measured DPT waveforms with the active overcurrent protection: (from the top to bottom): V_{GS}, V_{DS}, I_D , V_{C1}.

The driver should activate the overcurrent protection as soon as the voltage V_{C1} reaches the reference voltage level. The existing delay depends on the properties of components used in the protection and gate circuits. The failure signal propagation in the OCP circuit is presented in Table 2 related to time intervals are presented in Figure 8. It should be noticed that the present topology allows turning off the gate voltage in 281 ns after the overcurrent is detected instead of 1.1 μs as for the driver without Q_2 branch.

Conclusions

The optimized driver for the GaN transistor with the rapid ability of overcurrent protection has been presented. The detailed analyses of the driver operation shown its properties. The failure detection for OCP with the two-stage turning off

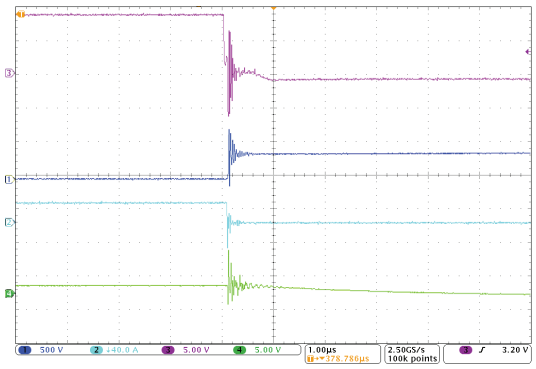

Fig. 7. Zoom of measured DPT waveforms while the overcurrent protection is activated: (from the top to bottom): V_{GS}, V_{DS}, I_D , V_{C1}.

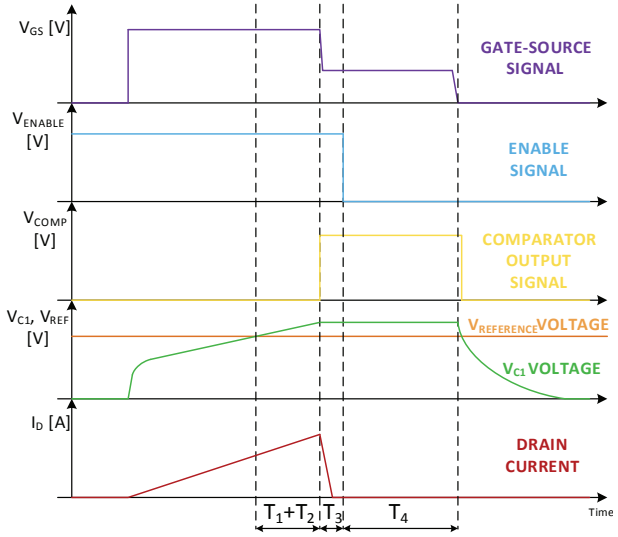

Fig. 8. Propagation delays of OCP and driver operation.

Table 2. Propagation delays of OCP and driver system

Interval	Element name	Unit	Value
T_1	Sensing circuit	[ns]	276
T_2	Ultra Fast Comparator	[ns]	5
T_3	RS Latch and Schmitt Inverter	[ns]	67
T_4	Driver output	[ns]	750

and also the independent control of turn on and off time of the GaN transistor have been described in the analytical investigation, simulation and laboratory test. The results prove that the application of presented driver topology accelerates the overcurrent protection response. The proposed solution could be applied with different types of WBG transistors.

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