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Low-Power Receivers for Wireless Capacitive Coupling Transmission in 3-D-Integrated Massively Parallel CMOS Imager

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***Abstract*— The paper presents pixel receivers for massively parallel transmission of video signal between capacitive coupled integrated circuits (ICs). The receivers meet the key requirements for massively parallel transmission, namely low-power consumption below a single μW, small area of less than 205 μm^2, high sensitivity better than 160 mV, and good immunity to crosstalk. The receivers were implemented and measured in a 3-D IC (two face-to-face stacked chips fabricated in CMOS 180 nm process). The maximum throughput of 20 Mbps of single receiver has been achieved using a return-to-zero (RZ) code. The static and dynamic power consumption of the single receiver are below 0.2 μW and 0.3 μW/MHz, respectively. The design approach for cost-effective inter-chip massively parallel transmission of photosensor signals with pulse position modulation (PPM) has been also performed. With this approach and the developed receivers it is possible to transfer between chips 9-10 bit images at a speed of over 1k fps.**

***Index Terms*— Capacitive coupling transmission, 3-D integrated circuit (3-D IC), vertically integrated circuit, CMOS imager, massively parallel imager, vision chip.**

I. Introduction

MASSIVELY parallel (pixel-parallel) CMOS imagers offer high data throughput due to fully parallel analog-to-digital conversion. An additional benefit is obtaining video signal directly in digital domain, which is more robust to interference, much easier to transfer and further processing. In this kind of image sensors an image frame is captured by a global shutter and then converted into digital form simultaneously in all (or in large group of) pixels [1]–[4]. If high-speed (1k-100k fps) image preprocessing is required, such as in machine vision, so-called vision chips are used which perform this preprocessing at pixel level [5]–[7]. The known pixel-parallel CMOS vision chips are realized planarly i.e. a light-sensitive device, an ADC, an image processor, and the accompanying control circuits are placed together in each pixel [1], [5]–[7]. The pixels are relatively large, even 100 μm × 100 μm [7], and their fill-factor of light-sensitive devices is relatively small, in practice not higher than 15% [5]–[7]. To substantially increase the fill-factor in the pixel-parallel vision chips, the non-planar 3-D integration can be used, which is increasingly used for the realization of still-camera-dedicated imagers [3], [4], [8]–[10]. These chips are fabricated in different technologies, vertically stacked and interconnected. For example, ADCs and digital circuits are fabricated in low-scale CMOS technologies providing high density of layout and low consumption of power. Whereas, the light-sensitive devices and analog circuits are integrated in dedicated technologies providing high quality light-to-voltage converters. The inter-chip connections are realized using through-silicon-via (TSV) [4], [8], micro bumps [9], [10], or Cu-Cu bonding [3] technologies. Unfortunately, these approaches have limitations such as the need for additional process steps which considerable increase manufacturing cost. Besides, these technologies make it difficult to test the chips independently of each other, and in consequence they reduce production yield.

In recent years, a wireless interconnection of chips has been intensively developed as an alternative to TSV. The feasibility of wireless transmission of digital signals between stacked chips has been proven in [11]–[18]. The signals can be transmitted through inductive or capacitive coupling interconnections [17], [18]. The interconnects based on inductive coupling require relatively big area for a single transmission channel, typically more than 100 μm × 100 μm. This big area is occupied by on-chip inductors and cannot be easily reduced. Moreover, such transmission consumes a relatively high power needed to generate current pulses with an amplitude of several mA. The high current pulses also worsen the problem of interference.

A capacitive coupling interconnection (Fig. 1) is more beneficial, because it provides a reliable data transmission through a capacitor formed from electrodes with an area as small as 10 μm × 10 μm. It can also be much better optimized in terms of power consumption for small area communication channels [18]. As the pixel size in vision chips can be as large as 100 μm × 100 μm, the electrodes need not be very small. However, the size of the receiver connected to the electrode must be minimal to fit into the pixel area together with the other circuits.

In this paper, receivers specially designed for wireless capacitive transmission system dedicated for 3D-integrated

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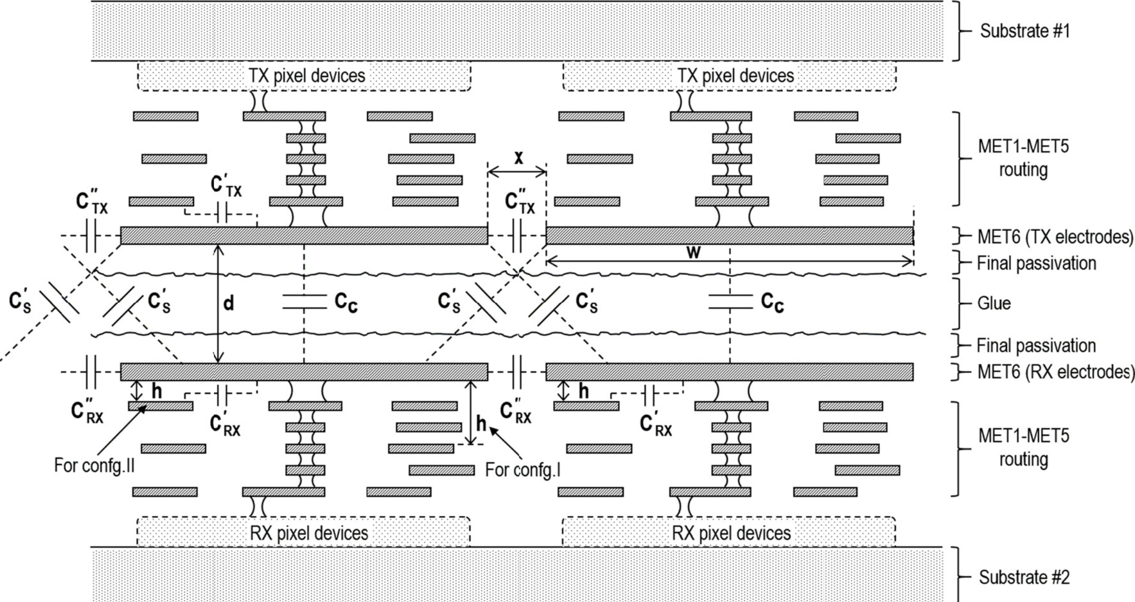

Fig. 1. Capacitive coupling of two chips (simplified view of the cross-section). The picture is drawn not to scale.

back-illuminated vision chips are presented. The proposed receivers take advantage of special features of the signals sent between the analog and digital parts of a single-slope ADC to achieve a reliable and energy-efficient transmission. In the paper remainder the most important features and requirements for the inter-chip vertical transmission of video signal and the outline of existing wireless transmission systems with emphasis on reduction of power supply were presented. In the next part, projects of low-power low-area receivers were presented together with the results of measurements carried out for the prototype fabricated in standard CMOS 180 nm technology.

II. PPM Wireless Transmission in 3-D-Integrated CIS

A. System Architecture and Requirements

The wireless transmission of video signals between stacked chips can be relatively easy established by utilizing a single-slope ADC. A simplified scheme for converting light intensity to a digital word using a single-slope ADC is shown in Fig. 2 [19]–[22]. The circuit consists of an analog part (an integration-mode photodiode, reset switch and a comparator) converting light intensity to a pulse V_2 of T_{pulse} width, and a digital part that converts the pulse width to an output digital word. The pixels of such topology, when implemented in classic planar manner, suffer from a low photodiode fill-factor because the digital part occupies most of the pixel area [1], [2], [5]–[7].

The analog and digital parts of the converter from Fig. 2 can be separated between two chips [8]—then the pulses V_2 can be transmitted through the capacitive coupling in two manners shown in Figs. 3(a) and 3(b). The coupling capacitors C_C are formed, when two chips are close to each other, as depicted in Fig. 1 [13], [14], [16], [18]. For proper operation of the ADC, only the ends (the final edges) of V_2 pulses must

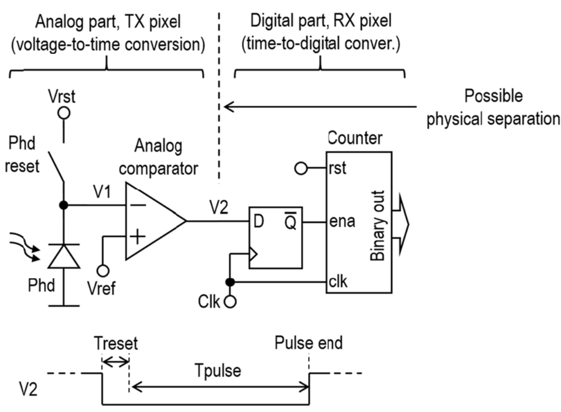

Fig. 2. Simplified schematic of a light-to-digital conversion using a single-slope ADC. The typical parameters of V_2 pulse are shown also.

be transmitted. This fact simplifies the system topology and reduces power consumption. The ending edge of V_2 pulse can be transmitted as a falling edge of V_{TX} (Fig. 3(a)) or as a rising edge of V_{TX} (Fig. 3(b)). The signal V_2 is pulse width modulated (PWM) and V_{TX} is pulse position modulated (PPM). Both chips must have the common ground potential.

The previous works on capacitive coupling interconnections [11]–[17] have mainly focused on achieving high data throughput up to Gbits per seconds. The capacitive interconnection intended for massively parallel vision chips requires much less throughput, but has to meet different requirements. When the vision chips acquire and process up to 1k fps with a dynamic range of 9 bits, a single pixel-channel should transmit V_2 pulses at 512 kbps with a time resolution of 1.95 μs and maximum jitter below 975 ns. However, high number of pixel-channels in an imaging array requires very low power consumption and high immunity to interference from adjacent channels.

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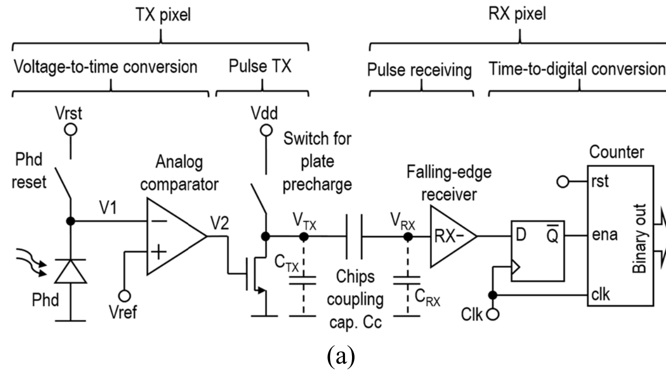
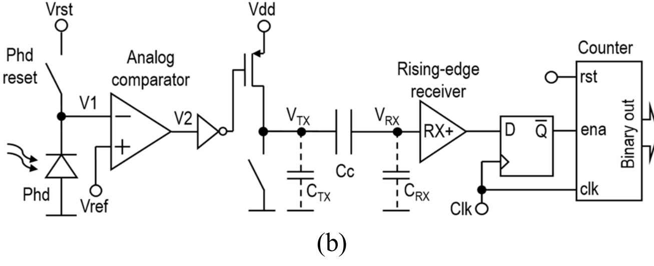
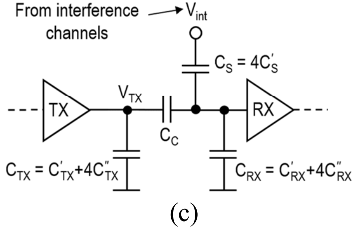


(a)



(b)



(c)

Fig. 3. Application of capacitive coupling and single-slope ADC for wireless PPM transmission of photosignal between chips: (a) the single pixel-channel for a falling-edge type transmission, (b) the single pixel-channel for a rising-edge type transmission, (c) the simplified model of the pixel-channels.

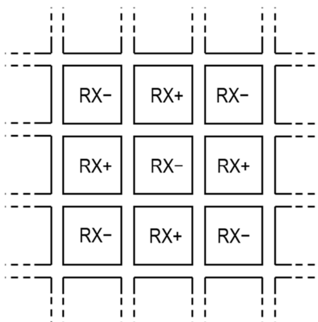


Fig. 4. Arrangement of the pixel-channels to minimize parasitic crosstalk.

A simplified model of a single transmitting pixel-channel is shown in Fig. 3(c). It consists of a transmitter TX, coupling capacitance C_C and a receiver RX. The capacitances C_{TX} and C_{RX} represent parasitic capacitances between the electrodes and the system ground. Based on Fig. 1 and Fig. 4, they are equal to $C_{TX} = C'_{TX} + 4\ C''_{TX}$ and $C_{RX} = C'_{RX} + 4C''_{RX}$. The total crosstalk from all neighboring channels is modeled by $C_S = 4C'_S$.

Transmission of timing pulses consumes power, which can be approximated by

$$P_{diss} \cong P_{TX} + P_{RX} + P_{SW} = P_{TX} + P_{RX} + \frac{f_{RST}}{2}\Big(C_{TX}\Delta V_{TX}^2 + C_C\left(\Delta V_{TX} - \Delta V_{RX}\right)^2 + C_{RX}\Delta V_{RX}^2\Big) \quad (1)$$

where P_{TX}, P_{RX} are respectively power dissipated in the transmitter and receiver without capacitive load ($C_{TX} = C_{RX} = C_C = 0$), whereas P_{SW} represents the power consumed for charging and discharging the capacitances in the pixel-channel (Fig. 3(c)), ΔV_{RX}, ΔV_{TX} are the voltage swings at the transmitter output and the receiver input, f_{RST} is the timing pulse repetition frequency. The configuration of the electrodes on the transmitting and receiving chips is similar, which means that C_{TX} and C_{RX} capacitances have similar values and are several times greater than C_C due to the relatively long distance d between the electrodes. The power P_{TX} dissipated in the transmitter is small, because the transmitter is usually realized as a dynamic inverter with low leakage current (Fig. 3(a) and Fig. 3(b)). For a system with a highly sensitive receiver, the last component in (1) may be omitted because of small amplitude ΔV_{RX} (typically $\Delta V_{RX} < 0.25\Delta V_{TX}$, thus $C_{Rx}\Delta V_{RX}^2 < C_{Tx}\Delta V_{TX}^2/16$). Therefore, the total power consumed by the transmission system depends mainly on power dissipated in the receiver P_{RX} and consumed for charging capacitance C_{TX} on the transmitter side. For that reason, to reduce power consumption, the main focus was put on designing receivers with high sensitivity and low power consumption.

The signals transmitted in each channel are particularly susceptible to interference from signal crosstalk due to dense arrangement of the pixels and relatively long distance d between the electrodes. For this reason, effective attenuation of interference from adjacent channels is especially important to ensure error-free transmission. The suppression methods proposed in the literature are based mainly on differential signaling and advanced arrangements of the capacitor electrodes [16]. In such solutions, interference from adjacent channels is attenuated in two ways, by compensation of complementary signals, and by converting interference into common-mode signals that are attenuated by differential receivers. Despite high effectiveness of interference attenuation, these solutions need differential transmitters and receivers occupying relatively big area that is needed for other pixel circuits. Furthermore, the receivers need additional tuning circuit outside the pixel array and require connections that must be distributed to each receiver inside the array. These additional connections would exacerbate the problem of high density of interconnections in the pixel array. For these reasons a new solution dedicated to pixel arrays has been developed.

To minimize the impact of interference from adjacent channels, two types of the transmission channels, falling-edge (Fig. 3(a)) and rising-edge (Fig. 3(b)), are arranged alternately as shown in Fig. 4. With this arrangement, each receiver is surrounded by channels where transmission is realized using

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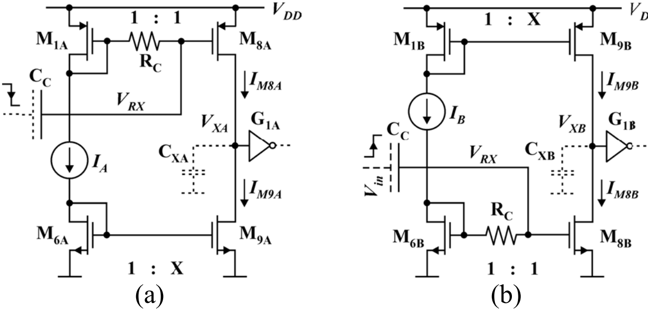

Fig. 5. General concept of the receivers: (a) sensitive to falling-edge (RX−), (b) sensitive to rising-edge (RX+). 1:X and 1:1 mean the current mirror gain, not the transistor aspect ratio.

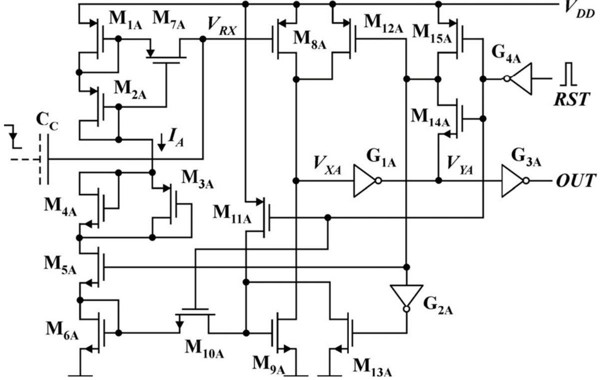

Fig. 6. Circuit diagram of the receiver sensitive to falling edge (RX−).

an opposite edge, which allows for a reduction of transmission errors.

B. Receivers Design

In high-throughput transmission systems [12]–[16] three main types of receivers are used, highly sensitive receivers (with sensitivity better than 200 mV_{pp}) containing a high gain preamplifier [12], [13], [16], receivers with adaptive mechanism to remove DC offset for precise sampling of the input signal [15], [16], and low sensitivity receivers (with sensitivity worse than 200 mV_{pp}) using a subthreshold-biased inverter as an input stage [14]. The highly sensitive receivers consume relatively high static power needed for proper biasing of the input preamplifier or the adaptive sampling circuit. Much less power is consumed by the low sensitivity receivers but they require stronger capacitance coupling between the chips. Strong coupling in 3-D-integrated vision chips is difficult to achieve due to limitations in reducing the distance between chips. For these reasons, only high-sensitivity receivers can be applied.

The general idea of the proposed highly sensitive, low-power receivers is explained in Fig. 5. Each receiver is based on two current mirrors biased by a common current I_A (I_B). In the receiver sensitive to falling-edge (Fig. 5(a)), the input signal is applied to the upper current mirror, whereas in the receiver sensitive to rising-edge (Fig. 5(b)) to the bottom one. In both receivers, the amplifying stage, composed of M_{8A} (M_{8B}), is in high gain common source configuration loaded by M_{9A} (M_{9B}). The input differentiating circuit, composed of R_C and C_C, makes the receivers sensitive only to signal edges. In idle, the output V_{XA} of the receiver in Fig. 5(a) is low, because the bottom current mirror gain is X times greater than the upper one. Notice, that only a falling edge of the input signal increases the drain current I_{M8A} and therefore can change V_{XA} output voltage to high. All the transistors are biased with very small current, and work in the subthreshold region, with the drain current defined by [23]

$$I_D = \left(\frac{W}{L}\right) I_T \exp\left(\frac{V_{GS}-V_{TH}}{nU_T}\right)\left(1-\exp\left(\frac{-V_{DS}}{U_T}\right)\right) \quad (2)$$

where $I_T = \mu(n\text{-}1)C_{OX}U_T^2$ is the technology current, n is the subthreshold slope factor (typically $1 < n < 2$), U_T is the thermal voltage, V_{TH} is a transistor threshold voltage, μ is the mobility in the channel, and C_{OX} is the oxide capacitance per unit area. The output voltage V_{XA} can only change to high if the drain current of M_{8A} increases X times or more. Neglecting in (2) the last component ($\exp(-V_{DS}/U_T) \ll 1$) one can derive a simple expression for the required change in the gate-source voltage $|\Delta V_{GS}|$ necessary to switch V_{XA} output voltage to high.

$$\begin{aligned} |\Delta V_{GS}| &= nU_T \left[\ln\left(\frac{I_A X}{I_T\,(W/L)}\right) - \ln\left(\frac{I_A}{I_T\,(W/L)}\right)\right] \\ &= nU_T \ln(X) \end{aligned} \quad (3)$$

Equation (3) shows that the receiver sensitivity can be adjusted by changing the ratio X. For example, for $n = 1.5$ and $U_T = 25$ mV one can achieve a receiver with sensitivity about 25 mV when $X = 1.95$.

The receiver output V_{XA} must be switched in a sufficiently short time Δt, therefore I_{M8A} current must be greater by ΔI than the minimum value $X \cdot I_{M9A}$ to allow for fast enough charging the parasitic capacitance C_{XA}, (C_{XB}). Assuming that the output inverter G_{1A} has negligible small delay and its threshold voltage is V_{THI}, the required excess current can be estimated from

$$\Delta I = \frac{V_{THI}}{\Delta t} C_{XA} \quad (4)$$

Under such conditions, the sensitivity of the receiver is

$$|\Delta V_{GS}| = nU_T \ln\left(X + \frac{\Delta I}{I_A}\right) = nU_T \ln\left(X + \frac{V_{THI} C_{XA}}{I_A \Delta t}\right) \quad (5)$$

where $\Delta I/I_A$ is typically below 1%.

In practical receiver realizations, the maximum achievable sensitivity (5) is limited by the influence of process, voltage and temperature (PVT) variation.

The detailed schematics of the proposed receivers are shown in Fig. 6 and 7. In the receiver sensitive to falling-edge (RX−), shown in Fig. 6, M_{1A}, M_{8A} and M_{6A}, M_{9A} form the upper and bottom current mirrors respectively. M_{7A} biased by the voltage drop on M_{2A} together with the coupling capacitance C_C works as the input differentiating circuit. The diode connected transistors M_{3A} and M_{4A} set the biasing current I_A. In each processing cycle the receiver is reset by a high level of RST signal. After reset, V_{XA} is set to low, the biasing current I_A is

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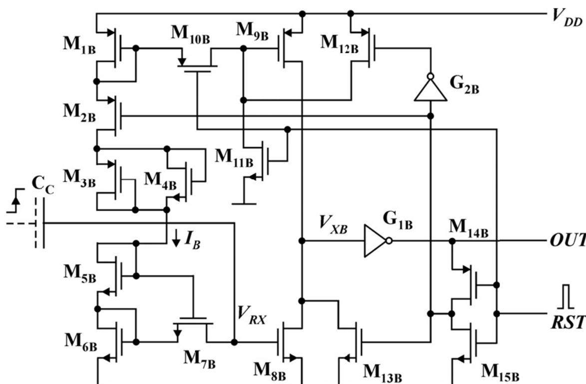

Fig. 7. Circuit diagram of the receiver sensitive to rising edge (RX+).

TABLE I

DIMENSIONS OF TRANSISTORS IN FIGS. 6 AND 7

RX+		RX-	
M_{1B} 1/1	M_{9B} 2/0.5	M_{1A} 2/0.5	M_{9A} 3/0.5
M_{2B} 1/1	M_{10B} 3/0.5	M_{2A} 1/1	M_{10A} 3/0.5
M_{3B}, M_{4B} 0.5/2	M_{11B} 3/0.5	M_{3A} 0.5/2	M_{11A} 3/0.5
M_{5B} 1/1	M_{12B} 1/0.3	M_{4A} 2/0.5	M_{12A} 0.3/0.18
M_{6B} 5/0.5	M_{13B} 0.5/0.5	M_{5A}, M_{6A} 1/1	M_{13A} 0.3/0.18
M_{7B} 0.5/1 (*)	M_{14B} 0.3/0.3	M_{7A} 0.3/1 (*)	M_{14A} 0.3/0.18
M_{8B} 1/0.5	M_{15B} 0.3/0.18	M_{8A} 2/0.5	M_{15A} 0.3/0.18

(*) M_{7B} and M_{7A} are medium V_T (V_{TN} = 0.25V, V_{TP} = -0.25V). The other transistors are normal V_T (V_{TN} = 0.42V, V_{TP} = -0.5V).

TABLE II

RECEIVER PARAMETERS FOR EXTREME CORNERS

	RX+			RX-		
	min	typ	max	min	typ	max
Threshold sensitivity (mV)	126 corner: SF/1.7V/ -20°C	153 corner: TT/1.8V/ 27°C	158 corner: FF/1.9V/ 50°C	40 corner: FF/1.7V/ -20°C	73 corner: TT/1.8V/ 27°C	91 corner: FF/1.9V/ 50°C
Static supply current (nA)	15 corner: SS/1.7V/ -20°C	120 corner: TT/1.8V/ 27°C	508 corner: FF/1.9V/ 50°C	22 corner: SS/1.7V/ -20°C	168 corner: TT/1.8V/ 27°C	730 corner: FF/1.9V/ 50°C
Transmiss. delay (ns)	19 corner: FF/1.9V/ 50°C	46 corner: TT/1.8V/ 27°C	185 corner: SF/1.7V/ -20°C	22 corner: FF/1.9V/ 50°C	96 corner: TT/1.8V/ 27°C	667 corner: SS/1.7V/ -20°C

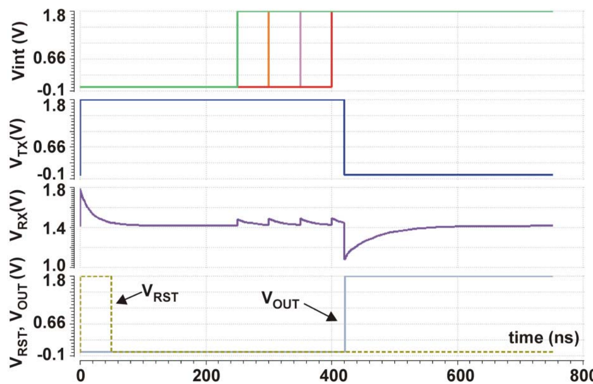

Fig. 8. Simulation results for RX− receiver when the interference pulses appear earlier than the useful pulse.

switched on by M_{5A}, and M_{9A} is biased by the voltage drop on M_{6A}. From this moment the receiver is ready to detect a transition of the input signal. A falling edge of the input signal, amplified by M_{8A}, generates a short rising V_{XA} pulse. As a result V_{YA} drops to low and switches on M_{14A} and M_{12A}, which in turn latches V_{OUT} output signal at a high level. At the same time M_{5A} switches off and disables biasing current I_A to reduce supply power consumption.

In an analogous way operates the receiver sensitive to rising-edge (RX+), shown in Fig. 7. In this case, the processing cycle begins with resetting V_{XB} to a high level. The input signal after differentiation by C_C and M_{7B} is amplified by M_{8B}. When a falling V_{XB} pulse occurs, M_{14B} and M_{13B} switch on and latch V_{XB} at low, and V_{OUT} at high levels.

Typical waveforms in the RX− receiver (Fig. 6) driven by the pixel channel (Fig. 3(c), $C_C = 43$ fF, $C_S = 7.5$ fF, $C_{RX} = 133$ fF) are presented in Fig. 8 and 9. The figures show two cases, when interference pulses V_{int} appear earlier or later than useful pulse V_{TX}. A high level of V_{RST} pulse sets the voltage V_{RX} to a standby value that biases M_{8A}. From this moment the receiver can detect a transition of the input signal. The rising edge of interference pulses V_{int}, after the differentiating, causes V_{RX} voltage jumps, which does not switch the output of the receiver. Only a falling edge of the useful V_{TX} pulse causes V_{RX} voltage to drop, resulting in switching the receiver output V_{OUT} to a high level. Notice that when the interference pulses appear earlier than useful, they slightly decrease receiver's sensitivity, as they reduce the gate-source voltage of the amplifying transistor M_{8A}. On the other hand, the later pulses slightly accelerate the rate of V_{XA} voltage increase, due to the crosstalk of the input voltage V_{RX} through the gate-drain capacitance of M_{8A}. The receiver's immunity to such interference pulses can be improved by reducing the time constant of the differentiating circuit (by increasing M_{7A} transistor width), however, if the time constant is too short, the receiver's sensitivity decreases. Therefore, when designing the receiver it is necessary to find a trade-off between immunity and sensitivity.

As the receivers are intended for pixel array and must fit into the pixel area together with the other pixel circuits, the main effort was focused on minimizing area occupied by the receiver on a chip, power consumption and maximizing receiver's sensitivity. Such conditions forced the use of transistors of the smallest possible size and minimum biasing currents I_A (I_B). The dimensions of transistors used in Fig. 6 and 7 are given in Table I. These conditions increase susceptibility of the receivers to PVT variations, therefore, the analysis of the receiver parameters for extreme operating conditions was carried out. Table II summarizes the parameters achieved for TSMC 180 nm CMOS technology, 1.8 ± 0.1 V supply voltage and temperature range from -20°C to +50°C. The receivers' threshold sensitivity varies from 40 mV to 158 mV

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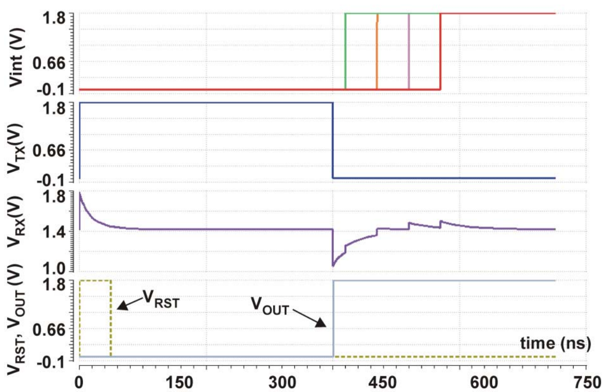

Fig. 9. Simulation results for RX− receiver when the interference pulses appear later than the useful pulse.

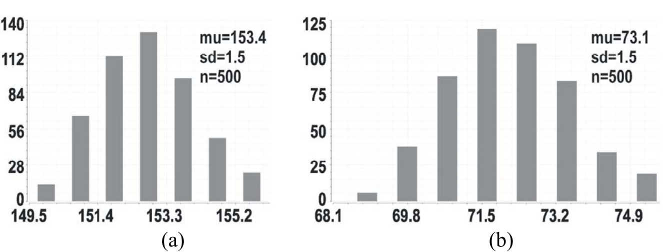

Fig. 10. Results of Monte Carlo simulation (TT corner, 27°C, $V_{DD} = 1.8$ V) of receiver sensitivity: (a) for RX+, (b) for RX−.

and typically is 153 mV and 73 mV respectively for RX+ and RX−. The transmission delay even in the worst case (667 ns) is less than the required limit 975 ns. The main reason for the wide spread of the receivers sensitivity is a large variation in static supply current, which varies from 15 nA to 730 nA. The improvement in sensitivity constancy can be achieved by using a more advanced circuit to generate a more constant I_A (I_B) bias current. Such a solution was not applied as it significantly increased complexity of the circuit and area occupied on a chip. The influence of random variation of technology parameters and transistor dimensions on the receivers' threshold sensitivity is shown in Fig. 10. The results obtained with 500 runs of Monte Carlo simulations show good constancy of the receivers' threshold sensitivity, the standard deviation *sd* is 1.5 mV for both receivers.

C. Assessment of the System Capabilities

To assess the contribution of the particular components in the total dissipated power (1), a transmission system designed in CMOS technology with 6 metal layers is assumed (Fig. 1). The top metal layer of 0.6 μm thickness, is separated from other metal layers by SiO_2 dielectric with thickness of 1 μm and relative dielectric permeability of $\varepsilon_{SiO2} = 3.9$. The distance between the electrodes of the two bonded chips is $d = 8$ μm, which consists of two thicknesses of 2 μm passivation layer and an adhesive layer of 4 μm thickness with relative dielectric permeability of $\varepsilon_{glue} = 3$. Moreover, it is assumed that the distance between the edges of the adjacent electrodes is $x = 3$ μm, and the two chips are aligned with each other with accuracy of 3 μm. The capacitor

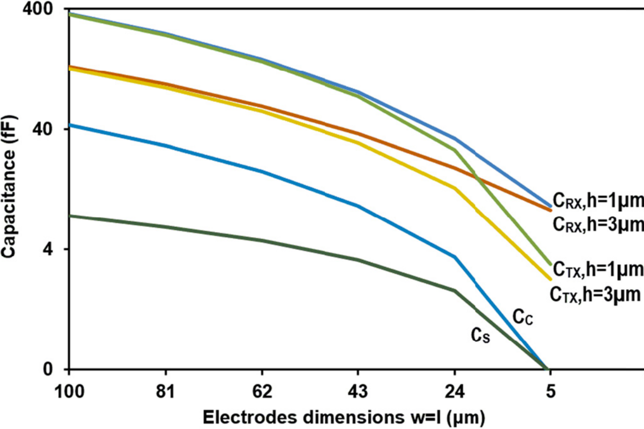

Fig. 11. Capacitances of the model in Fig. 3 as a function of electrode size (w = l) and distance h from a grounded metal.

electrodes are formed from the highest 6-th metal layer. The following two options of using the remaining metal layers are considered. Configuration I: the 5-th and 4-th metals (located directly under the capacitor electrode) are floating, and the 3-rd to 1-st metals are used for routing; Configuration II: all the metal layers from 5-th to 1-st are used for routing. Thus, the distance between the capacitor electrode and the nearest metal that is grounded for AC signals is $h = 3$ μm in the configuration I and $h = 1$ μm in the configuration II. The configuration I is more advantageous in terms of reducing the parasitic capacitances C_{TX} and C_{RX}, but the use of this variant is limited because it limits the number of possible metal layers to make connections inside pixels. The method described in [18] is applied to calculate the capacitances in the model in Fig. 3(c). Figure 11 shows capacitances values as a function of the size of the square ($w = l$) capacitor electrodes, assuming that the input capacitance of the receiver is $C_{in} = 6$ fF.

For electrodes of sizes $w = l = 100$ μm, the capacitances are $C_{RX} \cong 133$ fF, $C_{TX} \cong 127$ fF for the configuration I, and $C_{RX} \cong 366$ fF, $C_{TX} \cong 360$ fF for the configuration II. The coupling and crosstalk capacitances are $C_C \cong 43$ fF and $C_S \cong 7.5$ fF, respectively, and they are the same for both configurations. With the reduction of the electrodes size the reduction of all capacitances is observed, but their change is not proportional, in effect the signal transmittance $H_C = C_C/(C_C + C_{RX} + C_S + C_{in})$ decreases and the interference transmittance $H_S = C_S/\ (C_S + C_{RX} + C'_C + C_{in})$, where $C'_C = C_C C_{TX}/(C_C + C_{TX})$, increases causing deterioration of the signal-to-interference ratio, as shown in Fig. 12.

For both configurations of metal usage, Fig. 13 shows amplitudes of the useful and interference signals, $V_C = H_C V_{TX}$ and $V_S = H_S V_{TX}$ respectively, at the input of the receiver, under the assumption that $V_{TX} = 1.8$ V. The V_{RX} represents effective signal at the receiver input as the difference between V_C and V_S. The figure also shows the highest sensitivity threshold of 158 mV of the designed receivers. The transmission is possible when the dimensions of the electrodes are greater than 100 μm and 27 μm for configuration II and I respectively.

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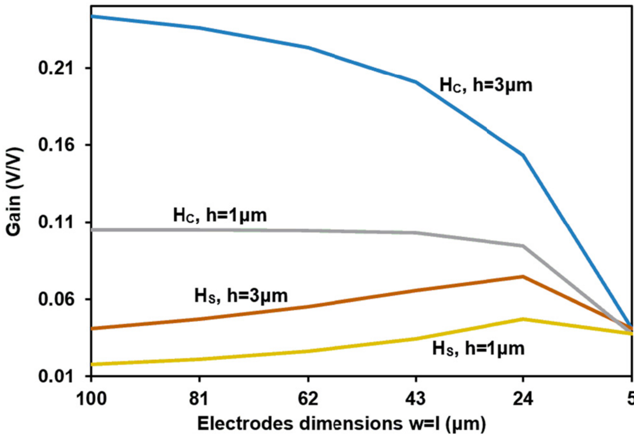

Fig. 12. Amplitude of the channel-signal H_c and interference-signal H_S transmittances as a function of electrode size (w = l) and distance h from a grounded metal.

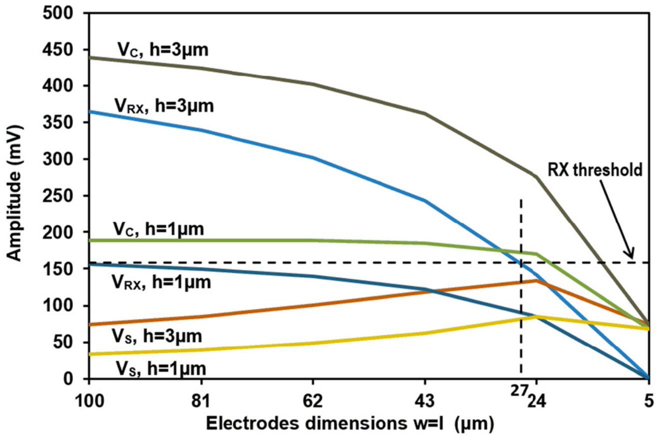

Fig. 13. Calculated amplitudes of the useful V_C and interference V_S signals as a function of electrode size (w = l) and distance h from a grounded metal.

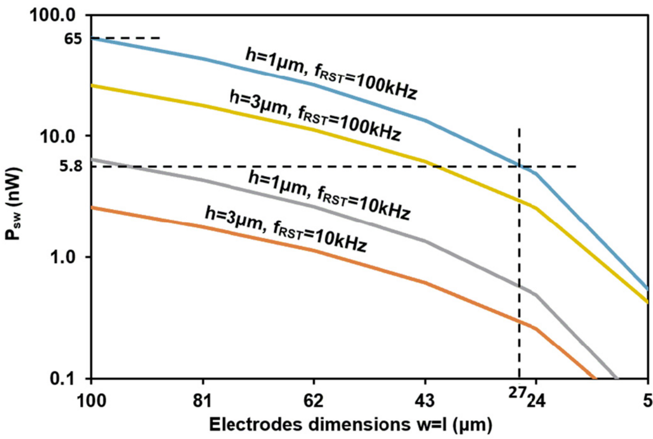

Fig. 14. Power dissipated on capacitor charging as a function of electrode size (w = l) and distance h from a grounded metal. (Calculation results).

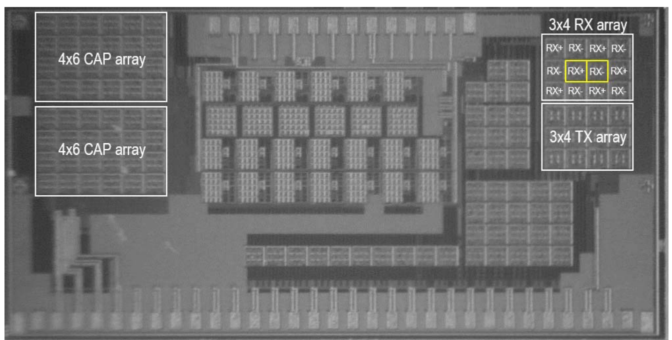

Fig. 15. Photo of the prototype chip surface with visible electrode arrays (chip size 1.6 mm × 3.2 mm).

The power dissipated to charge the capacitors as a function of electrode size for f_{RST} equal to 10 and 100 kHz is shown in Fig. 14. Notice, that even for a relatively high image acquisition rate of 100k fps, the power is 5.8 nW and 65 nW for the minimum (27 μm) and maximum (100 μm) electrode sizes, respectively. Hence, this power represents only a small fraction of the power consumed by the designed receivers (Table II: 216 nW, 302 nW respectively for RX+, RX−).

III. Experimental Results

This section presents measurement results of the receivers designed for transmission of PPM signals in 3-D-integrated vision chips. The prototype contains only a set of transmitters and receivers, without photosensors and associated circuits, allowing for practical verification of transmissions at reduced chip fabrication costs. Fig. 15 shows a single prototype chip fabricated in the standard 180 nm CMOS technology of TSMC, whereas Fig. 16 shows two face-to-face glued chips mounted on a PCB in Fraunhofer Institute for Reliability and Microintegration IZM, Berlin. The single chip contains two electrode arrays of 4 × 6 and 3 × 4 size. All the electrodes are of $w = l = 100$ μm dimension, and the distance between their edges is $x = 10$ μm. The 5-th and 4-th metal layers (located directly under the capacitor electrode) are floating, therefore the structure of the chip corresponds to the configuration I considered earlier. The 4×6 arrays are used to measure capacitive couplings between the upper and bottom chips. The electrodes in the upper array are connected to the transmitters, which simplified schematic are shown in Fig. 3(a) and Fig. 3(b). The bottom array electrodes are connected to the chip pad via source followers and analogue multiplexers to allow voltage measurement at the receiving end. The 3×4 arrays represent a model solution of the transmission system consisting of a matrix of receivers and transmitters in the configuration of Fig. 4.

The main tests were performed using RX+ and RX− receivers centrally located in the rectangle in the upper 3×4 array in Fig. 15. The results of measurements of H_C transmittance amplitude between each of the pairs of transmitting and receiving electrodes in the 4×6 matrix are shown in Fig. 17(a). Figure 17(b) illustrates the amplitude of the parasitic coupling H_S between the electrode with coordinates of (2, 2) and the adjacent electrodes. The measurements show that the average values of the coupling between the transmitter and receiver, and the parasitic coupling to the adjacent channels are 0.217 and 0.005, respectively. Note that H_S interference

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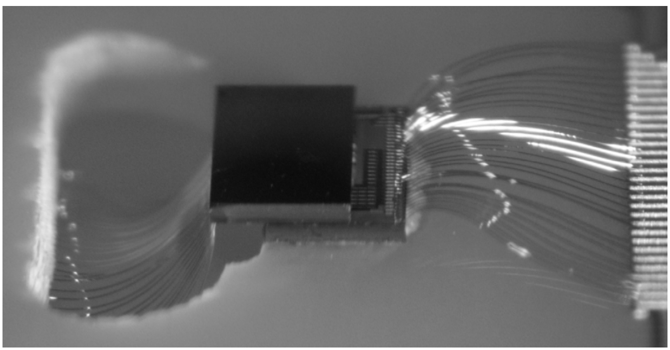

Fig. 16. Photo of the glued chips used for transmission testing.

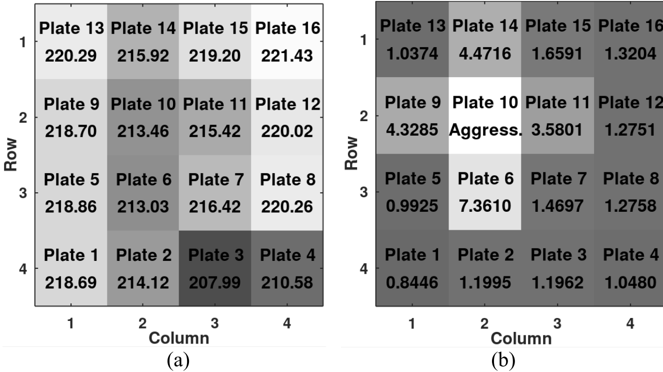

Fig. 17. Measured transmittance amplitude (mV/V): (a) between each pair of transmitting and receiving electrodes, (b) between the electrode with coordinates (2,2) and adjacent electrodes in a portion of 4×6 array.

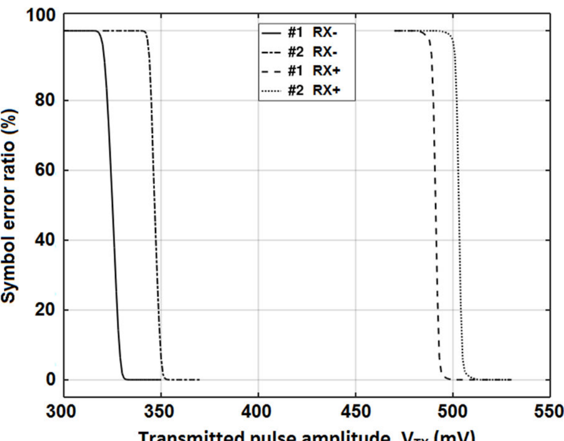

Fig. 18. Measured symbol error ratio in RX+ and RX− receivers as a function of transmitted pulse amplitude (pseudo random data 16-PPM, 10^7 symbols for every measurement with $f_{RST} = 1$ MHz). The #1 and #2 mean respectively that the top or bottom chip is transmitting.

transmittance, shown in Fig. 12, includes coupling from 4 adjacent channels, thus $H_S = 4 \cdot 0.005 = 0.02$. The observed spread of the amplitude of the coupling results mainly from the heterogeneity of the adhesive layer and inaccurate positioning of both chips.

The threshold sensitivity of the receivers was determined by measuring the symbol error ratio as a function of V_{TX} transmitted pulse amplitude. Figure 18 shows the ratio recorded

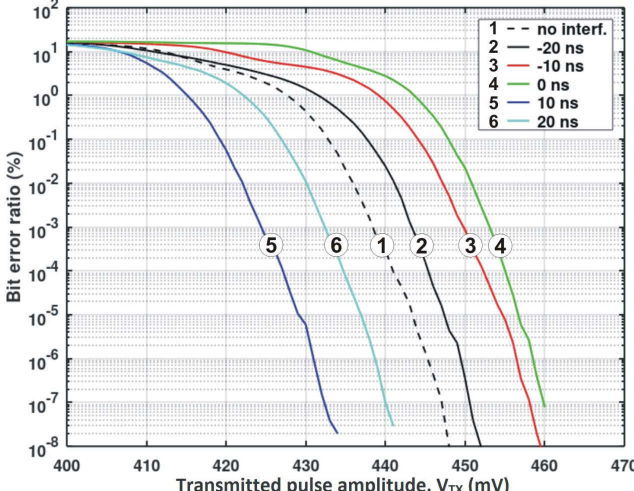

Fig. 19. Measured BER in RX− receiver as a function of the amplitude of transmitted useful signal (pseudo random data in RZ-code, 20 Mbps, $f_{RST} = 20$ MHz). The interference signals amplitude is constant and equal to 600 mV. The times -10 ns and 10 ns mean that the useful and interference edges are respectively delayed or speed-up relative to each other.

during the transmission of a pseudo random digital data sequence encoded using 16-PPM. The 10^7 symbols has been sent for every measurement with frequency 1 MHz. A steep increase in the error ratio arises when the transmitter signal amplitude is less than 350 mV and 510 mV for RX− and RX+, respectively. Therefore, the threshold sensitivity of the receivers, determined taking into account the magnitude of the coupling, is 70 mV and 102 mV for RX− and RX+ respectively. The measured average static currents supplying RX+ and RX− receivers in standby are respectively 78 nA and 106 nA. The dynamic power associated with switching is about 167nA·1.8V/MHz.

To investigate the influence of interference from adjacent channels, pulses with a falling edge, representing a useful signal, were applied to the transmitting electrode above the RX− receiver (centrally located in rectangle in Fig. 15), whereas interfering pulses with a rising edge were applied to the adjacent electrodes. The measurement results of the bit error ratio (BER) as a function of amplitude of the useful signal transmitted at the maximum speed of 20 Mbps are depicted in Fig. 19. The plots show that the highest BER appears when the falling edge of the useful pulse coincides with the rising edge of the interfering pulses. Under such conditions, practically error-free transmission—from the point of view of the vision-chip applications—can be achieved for transmitter pulse amplitude V_{TX} greater than 460 mV (BER $< 10^{-7}$). Comparing BER changes with respect to non-interference conditions, one can see that BER increases when the interfering pulses are earlier (−10 ns, −20 ns) than useful, otherwise (10 ns, 20 ns) BER decreases. These effects result from the fact that earlier interference pulses cause a slight decrease of the receiver's sensitivity, while later pulses slightly speed up switching of the receiver, which in effect also increases its sensitivity. Note that the reported results refer to extreme transmission conditions when the speed is

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TABLE III
PARAMETERS OF RECEIVERS INTENDED FOR CAPACITIVE TRANSMISSION

	[12]	[13]	[14]	[15]	[16]	This work
CMOS tech. (nm)	180	130	130	180	65	180
Supply (V)	1.8	1.2	1.2	1.8	1.2	1.8
Throughput (Gbps/ch)	3	0.93	2.46	2	2.31	0.02
Electr. size $w{\times}l$ (μm×μm)	60×60	8×8	8×8	80×80	11×11	100×100
Electr. dist. x (μm)	na	8-25	na	4	2	10
Electr. spac. d (μm)	1	1	1	na	1	8
Rx area (μm^2)	675	na	1300 Rx&Tx	2900	na	205 Rx+ 190 Rx-
Rx sens. (mV)	120	na	400	25	110	140(*) Rx+ 97(*) Rx-
Power (μW)	10000 @3Gb/s	15-23 static	1.6 static	1630 @2Gb/s	83 static	0.14 Rx+ 0.19 Rx- static

(*)Measured at 20 Mbps. Bit error ratio BER = 10^{-8} (transmitted signal amplitude V_{TX} reduced from 1.8 V to 460 mV and 660 mV respectively for RX- and RX+).

20 Mbps, while the receivers were designed for only 512 kbps (as explained in Sec. II.A).

Measurement of the error ratio for RX+ and RX− receivers at transmitter pulse amplitude V_{TX} greater than 660 mV showed practically error-free transmission (the symbol error ratio below 10^{-8}). These results confirm the conclusions given in section II.C that at maximum $V_{TX} = 1.8$ V, the electrodes dimensions can be reduced more than threefold in size (from 100 μm × 100 μm to 27 μm × 27 μm) while maintaining the same error level.

IV. COMPARISON

It is difficult to make a direct comparison, because our wireless transmission system is the first published solution of this kind designed for vision chips. We can only give an idea of how our results look like against the existing no-vision-chips-intended Gbps-throughput solutions. Table III presents the main parameters of our low-throughput receivers (*this work*) and receivers for high-speed digital data transmissions. While comparing, note that the receivers in [12]–[16] were optimized with regard to power consumption at high transmission speed and area of the electrodes, while area occupied by the receivers on a chip, was not the main concern. The proposed receivers were designed for vision chips, where the main criterion was to minimize the receiver area and the number of interconnections to other circuits. Besides, the receivers are suited for transmission over a longer distance ($d = 8$ μm) compared to the other solutions ($d = 1$ μm). With such requirements, it was much more difficult to achieve a favorable power to speed ratio. The post-measurement analysis shows that relatively big electrodes used in the proof-of-concept chips can be reduced to 27 μm × 27 μm when two metal layers below the coupling electrodes remain floating. Further reduction can be achieved by reducing the distance between the chips, a four-fold reduction of the distance allows the use of electrodes with approximately 14 μm × 14 μm dimensions. The designed receivers consume 140-190 nW of static power. By using a more advanced circuit to stabilize the biasing current I_A (I_B) the power can be reduced below several dozen nW.

V. CONCLUSION

A design and an IC realization of the CMOS receivers for capacitive transmission between vertically stacked chips has been presented. The prototype receivers were specialized for mixed-signal 3-D structures with a transmit chip containing analog back-illuminated photopixel array and with a receive chip containing array of ADCs, image processors, and control circuits. Contrary to known high-throughput receivers for digital 3-D structures, the presented solutions occupy smaller chip area, consume lower power and are highly sensitive. Moreover, they meet the specific constraints of the chip stack assembly for 3D-integrated back-illuminated vision chips, namely relatively large distance between chip surfaces. The error-free transmission was established due to the high sensitivity of receivers and due to the reduction of interference using PPM-type transmission based on the opposite-type pulses and receivers. With this realization of vertically integrated imagers, it is possible to reduce manufacturing costs and increase the production yield compared to other known realizations.

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