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# Rapid and reliable re-design of miniaturized microwave passives by means of concurrent parameter scaling and intermittent local tuning

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Re-design of microwave passive components for the assumed operating frequencies or substrate parameters is an important yet a tedious process. It requires simultaneous tuning of relevant circuit variables, often over broad ranges thereof, to ensure satisfactory performance of the system. If the operating conditions at the available design are distant from the intended ones, local optimization is typically insufficient, whereas global search entails excessive computational expenses. The problem is aggravated for miniaturized components, typically featuring large numbers of geometry parameters. Furthermore, owing to their tightly-arranged layouts, compact structures exhibit considerable cross-coupling effects. In order to reliably evaluate electrical characteristics under such conditions full-wave electromagnetic (EM) analysis is mandatory. Needless to say, EM-driven design over broad ranges of operating frequencies is an arduous and costly endeavor. In this paper, we introduce a novel procedure for rapid and reliable re-design of microwave passives. Our methodology involves concurrent scaling of geometry parameters interleaved with local (gradient-based) tuning. The scaling stage allows for low-cost relocation of the operating frequencies of the circuit, whereas the optimization stage ensures continuous (iteration-wise) alignment of the performance figures with their target values. The presented framework is validated using several miniaturized microstrip couplers, re-designed over extended ranges of the center frequencies. For all considered structures, satisfactory designs are successfully identified despite the initial designs being distant from the targets, whereas local tuning turns out to be demonstrably inferior. Apart from its efficacy, one of the most important advantages of the proposed framework is its simplicity, and the lack of problem-dependent control parameters.

There is no doubt that optimization methods have now become an intrinsic part of the microwave design process. For many classes of circuits, rough initial designs can usually be obtained by means of the traditional, e.g., circuit theory methods (either in the form of explicit analytical formulas[1], or equivalent networks[2]). Notwithstanding, conventional techniques and circuit models lack the accuracy whenever phenomena like dielectric and radiation losses or electromagnetic (EM) cross-coupling, have non-negligible effects on the system characteristics. Securing the best achievable performance requires cautious tuning of circuit dimensions[3]. Intricacy of modern microwave systems made experience-driven parametric studies virtually obsolete. Instead, rigorous numerical optimization is recommended[4], which enables efficient handling of multiple variables, objectives, and constraints[5,6]. Unfortunately, optimization of microwave devices faces serious difficulties on its own. On the one hand, it is often necessary to handle large numbers of system variables, which is numerically demanding. On the other hand, accurate evaluation of circuits often involves CPU intensive full-wave EM analysis. Both factors contribute to considerable costs associated with parameter tuning[7], as well as limited efficacy of conventional algorithms[8]. These problems are particularly pronounced for compact passive components constructed by meandering transmission lines (TL)[9–13], compact microwave resonant cells (CMRCs)[14], slow-wave phenomenon[15], defected ground structures (DGS)[16,17], electronic bandgap structures (EBG)[18,19], or a variety of geometrical alterations (slots[20], stubs[21],

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shorting pins[22], etc.). Miniaturization using the aforementioned approaches multiplies the number of degrees of freedom within the structures (e.g., a typical CMRC unit is described by at least four parameters versus two for a TL), which further exacerbates their design process, including optimization. In many cases, local algorithms[23] have to be replaced by global procedures[24–29], often leading to unmanageable computational expenses.

The literature provides a plethora of algorithmic solutions primarily aiming at the improvement of both the computational efficiency and reliability of the EM-driven optimization procedures. Acceleration methods include the incorporation of techniques for fast evaluation of circuit response gradients (adjoint sensitivities[30,31], mesh deformation[32], parallelization[33]), replacing numerical derivatives by updating formulas[34], as well as utilization of sparse sensitivity updates[35–37]. In a more generic setting, surrogate-assisted procedures have been gaining considerable attention[38–41], both in the context of physics-based (space mapping[42], adaptive response scaling[43], manifold mapping[44]), and data-driven models (radial basis functions[45], kriging[46], artificial neural networks[47], ensemble learning[48], support vector regression[49]), along with variable-resolution methods (co-kriging[50], Bayesian model fusion[51]). Surrogate-based methods are applied for both local[52, 90–93] and global optimization[53–55], but also multi-criterial design[56–59], and uncertainty quantification[60–62]. In terms of reliability improvements, in some cases combined with acceleration, some of the worth-mentioning techniques include efficient global optimizers (EGO)[63], machine learning frameworks[64], response feature technology[65], cognition-driven design[66], frequency-based regularization[67], or adaptive design specification strategies[68]. Some of these approaches aim at facilitating exploration of the parameter space[63,69], whereas others alleviate the difficulties pertinent to local routines (e.g., sensitivity to initial design[67,68]).

A particular type of an optimization task, which is of significant practical importance, is a re-design of a given microwave component to a different set of operating conditions (e.g., center frequency, power division ratio, etc.) or material parameters (e.g., substrate permittivity or thickness). The need for re-design may arise due to employing a circuit in a new application area, or implementing it on a different substrate. The associated numerical challenges are similar to those elaborated on at the beginning of this section: high computational cost, and potential reliability issues, especially for local search, or when the structure is to be scaled for operating parameters considerably misaligned with those at the current design. A number of frameworks have been developed to facilitate the dimension scaling process, including analytical design curves[70], utilization of inverse surrogate models[71,72], response features[73], as well as more sophisticated frameworks that enable control of both the major operating conditions (e.g., center frequencies) and supplementary performance figures (e.g., power split ratios)[74]. The major drawback of the aforementioned techniques constitutes a high initial cost necessary to construct the surrogate models, which are typically rendered using pre-optimized reference designs[71]. Utilization of generic surrogate modeling techniques is another option[75–78]; however, setting up dependable metamodels over extended ranges of cicuit dimensions and material parameters (otherwise necessary to ensure design utility) is exacerbated by the curse of dimensionality and highly nonlinear microwave components characteristics. A possible workaround is a utilization of performance-driven modeling methods, which permit a rendition of accurate surrogates at a fraction of CPU costs incurred by conventional techniques[79–81].

This article introduces a novel technique for fast and reliable re-design of passive microwave devices. Our methodology employs a concurrent scaling of geometry parameters, which is interleaved with local tuning. The role of the scaling stage is to perform large-scale design relocation of the circuit operating frequency at low computational cost. The tuning stage aims at improving the performance parameters of the circuit before launching the next scaling step. Eventually, i.e., upon relocating the operating frequency near the target, the process defaults to gradient-based optimization. The efficacy of the introduced technique is verified using several compact microstrip couplers, which are re-designed for center frequencies distant from those at the initial designs. Comparative experiments also indicate that straightforward local search normally fails under these conditions. Apart from its reliability, the proposed framework exhibits other attractive features, including simple implementation, easy handling, in particular, the lack of problem-dependent control parameters that need to be tuned, and low cost. The latter is related to the fact that our method does not utilize any surrogate models, and, consequently, there is no initial cost associated with the acquisition of either training data or pre-optimized reference designs.

## Circuit re-design using concurrent scaling and intermittent local tuning

This section explains the constituent parts of the introduced re-design methodology. We start by formulating the design problem in Sect. "Problem statement". Section "Concurrent parameter scaling" discusses the concurrent parameter scaling stage. Section "Intermittent local tuning" describes the local (gradient-based) tuning step, which is carried out to ensure sufficient performance of the circuit before executing the subsequent scaling step. The complete optimization procedure has been summarized in Sect. "Complete optimization procedure".

**Problem statement.** In the following, $\boldsymbol{x} = [x_1 \ldots x_n]^T$ represents the vector of design parameters of the considered circuit (i.e., its dimensions). We will also denote by $\boldsymbol{S}(\boldsymbol{x})$ the EM-simulated scattering parameters. For individual $S$-parameters, we will use the symbol $S_{jk}(\boldsymbol{x}, f)$ to denote the value of $S_{jk}$ at the design $\boldsymbol{x}$ and frequency $f$. Finally, we denote by $\boldsymbol{F}_t = [F_{t.0} \; F_{t.1} \ldots F_{t.N}]^T$ the target vector of operating parameters with the first entry, $F_{t.0}$, being the operating frequency. The remaining entries denote the target values for other figures of interest, such as bandwidth, footprint area, power split ratio, material parameters of the substrate the circuit is to be implemented on, etc. At this point, it should be emphasized that the optimization technique introduced in this paper pertains to single-band structures. A generalization for multi-band systems will be discussed elsewhere.

The quality of design $\boldsymbol{x}$ with respect to the target vector $\boldsymbol{F}_t$ is quantified using the objective function $U(\boldsymbol{x}, \boldsymbol{F}_t)$, which should be defined so that lower values of $U$ correspond to better designs, i.e., those that meet the design specifications to the fuller extent. Having the objective function, the optimization task is formulated as

$$\boldsymbol{x}^* = U^*(\boldsymbol{F}_t) = \arg \min_{\boldsymbol{x} \in X} U(\boldsymbol{x}, \boldsymbol{F}_t) \tag{1}$$

Here $\boldsymbol{x}^*$ is the optimum design to be identified. The optimum solution is sought for in the design space $X$, which is normally delimited using the lower bounds $\boldsymbol{l} = [l_1 \ldots l_n]^T$ and the upper bound $\boldsymbol{u} = [u_1 \ldots u_n]^T$ for the system parameters, i.e., $l_k \leq x_k \leq u_k$, $k = 1, \ldots, n$. In some cases, we also have additional constraints: inequality or equality ones. However, in the following, we assume for simplicity that the only geometrical constraints are those related to $\boldsymbol{l}$ and $\boldsymbol{u}$.

Table 1 gathers a few exemplary design tasks for microwave components. Note that in the presented formulations, some of the design objectives are treated as constraints, and handled using a penalty function approach[82]. For more information about penalty functions see, e.g.,[82,83].

**Concurrent parameter scaling.** The physical size of conventional (transmission-line-based) microstrip components affects the guided wavelength[1,2]. Consequently, approximate re-design of circuit parameters, aimed at relocating the operating frequency of the system, can be achieved through a concurrent dimension scaling, i.e., jointly increasing or decreasing the geometry parameters. In this work, we describe this process as a transformation $M_S(\boldsymbol{x}, \alpha)$, defined as

$$M_S(\boldsymbol{x}, \alpha) = M_S([x_1 \ldots x_n]^T, \alpha) = [\min(u_1, \max(l_1, \alpha x_1)) \ldots \min(u_n, \max(l_n, \alpha x_n))]^T \tag{2}$$

| Task description | Target operating vector | Objective function$^\$$ |
|---|---|---|
| Improve matching $\lvert S_{11} \rvert$ of impedance transformer over the frequency range $f_L$ to $f_H$ | $\boldsymbol{F}_t = [F_{t.0} \; F_{t.1}]^T$ where $F_{t.0} = (f_L + f_H)/2$ – center frequency $F_{t.1} = [f_H - f_L]$ – bandwidth | $U(\boldsymbol{x}, \boldsymbol{F}_t) = \max \left\{ F_{t.0} - \frac{F_{t.1}}{2} \leq f \leq F_{t.0} + \frac{F_{t.1}}{2} : \lvert S_{11}(\boldsymbol{x}, f) \rvert \right\}$ |
| Improve matching $\lvert S_{11} \rvert$ and isolation $\lvert S_{41} \rvert$ of a microwave coupler, and ensure power split $d_S(\boldsymbol{x}, f) = \lvert \lvert S_{21}(\boldsymbol{x}, f) \rvert - \lvert S_{31}(\boldsymbol{x}, f) \rvert \rvert = K$, both at the center frequency $f_0$; the circuit is to be implemented on the substrate of permittivity $\varepsilon_r$ | $\boldsymbol{F}_t = [F_{t.0} \; F_{t.1} \; F_{t.2}]^T$ where $F_{t.0} = f_0$ – center frequency $F_{t.1} = K$ – power split ratio $F_{t.2} = \varepsilon_r$ – substrate permittivity | $U(\boldsymbol{x}, \boldsymbol{F}_t) = \max \{ \lvert S_{11}(\boldsymbol{x}, F_{t.0}) \rvert, \lvert S_{41}(\boldsymbol{x}, F_{t.0}) \rvert \}$ $+ \beta c(\boldsymbol{x}, \boldsymbol{F}_t)^2$ where $c(\boldsymbol{x}, \boldsymbol{F}) = \lvert S_{31}(\boldsymbol{x}, F_{t.0}) \rvert - \lvert S_{21}(\boldsymbol{x}, F_{t.0}) \rvert - F_{t.1}$ |
| Reduce footprint $A(\boldsymbol{x})$ of a microstrip coupler while maintaining matching and isolation at −20 dB or better, and equal power split ratio, both over the bandwidth $[f_0 - B/2, f_0 + B/2]$ | $\boldsymbol{F}_t = [F_{t.0} \; F_{t.1} \; F_{t.2}]^T$ where $F_{t.0} = f_0$ – center frequency $F_{t.1} = B$ – target bandwidth $F_{t.2} = -20$ dB – acceptance threshold for $\lvert S_{11} \rvert$ and $\lvert S_{41} \rvert$ | $U(\boldsymbol{x}, \boldsymbol{F}_t) = A(\boldsymbol{x}) + \beta_1 c_1(\boldsymbol{x}, \boldsymbol{x}_t)^2 + \beta_2 c_2(\boldsymbol{x}, \boldsymbol{F}_t)^2$ where $c_1(\boldsymbol{x}, \boldsymbol{F}_t) = \max \left\{ \begin{array}{l} F_{t.0} - \frac{F_{t.1}}{2} \leq f \leq F_{t.0} + \frac{F_{t.1}}{2} : \\ \max \left\{ \frac{\max \{ \lvert S_{11}(\boldsymbol{x}, f) \rvert, \lvert S_{41}(\boldsymbol{x}, f) \rvert \} + F_{t.2}}{F_{t.2}} \right\} \end{array} \right\}$ $c_2(\boldsymbol{x}, \boldsymbol{F}_t) = \max \left\{ \begin{array}{l} F_{t.0} - \frac{F_{t.1}}{2} \leq f \leq F_{t.0} + \frac{F_{t.1}}{2} : \\ \lvert \lvert S_{31}(\boldsymbol{x}, f) \rvert - \lvert S_{21}(\boldsymbol{x}, f) \rvert \rvert \end{array} \right\}$ |

**Table 1.** Selected examples of design tasks for passive microwave components. $^\$$The coefficient $\beta > 0$ is a penalty factor that controls the contribution of the penalty terms to the merit function[82].
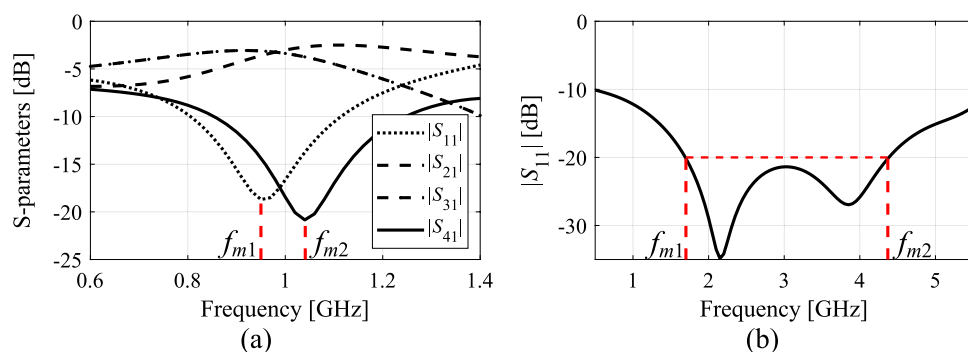


**Figure 1.** Extracting approximate center frequency $f_{a.0}$ of a circuit: (**a**) microwave coupler: $f_{a.0} = (f_{m1} + f_{m2})/2$, where $f_{m1}$ and $f_{m2}$ are the frequencies of the minima of $\lvert S_{11} \rvert$ and $\lvert S_{41} \rvert$, respectively; (**b**) impedance matching transformer: $f_{a.0} = (f_{m1} + f_{m2})/2$, where $f_{m1}$ and $f_{m2}$ are the frequencies corresponding to the left- and right-hand-side edges of the −20 dB bandwidth of the circuit, respectively.

Recall that $\mathbf{l} = [l_1 \ldots l_n]^T$ and $\mathbf{u} = [u_1 \ldots u_n]^T$ stand for the lower and upper bounds for geometry parameters. The transformation $M_S$ is defined to ensure that the scaling process leaves the design within the assumed design space $X$.

Let $f_{a.0}(\mathbf{x})$ be the actual center frequency of the circuit at hand at a certain design $\mathbf{x}$. It can be extracted from the EM-simulated system responses, and defined depending on the particular type of a circuit. Typically, it would be the arithmetic average of the frequencies corresponding to the specific features of the system responses, e.g., the minima of the matching and isolation response for a coupler (cf. Figure 1a), or the frequencies determining the bandwidth for a broadband impedance transformer (cf. Figure 1b).

Here, the concurrent dimension scaling is executed to re-align the operating frequency of the circuit with its target value $F_{t.0}$. The scaling coefficient $\alpha$ is computed as

$$\alpha = \min \left\{ \alpha_{\max}, \max \left\{ \alpha_{\min}, \frac{f_{a.0}(\mathbf{x})}{F_{t.0}} \right\} \right\} \tag{3}$$

where $\alpha_{\min}$ and $\alpha_{\max}$ are user-defined lower and upper bounds. These are introduced to avoid excessive scaling, which may be detrimental to the shape of the circuit characteristics. This is particularly important for compact structures, where interrelations between geometry parameters and electrical responses are rather complex. Concurrent scaling usually leads to response distortion if carried out using $\alpha$ which is significantly different from the unity. Figure 2 illustrates this for an exemplary microstrip coupler scaled using $\alpha = 1.2$, 1.4, and 1.6. Typically, we would set $\alpha_{\min} = 0.7$, and $\alpha_{\max} = 1/\alpha_{\min}$, to be on a safe side.

Concurrent scaling is followed by the extraction of the center frequency $f_{a.0}$. If the extraction is impossible due to heavy distortion of the circuit characteristics, the scaling is repeated with an updated coefficient $\alpha/m_\alpha$ (for $\alpha > 1$) or $m_\alpha \alpha$ (for $\alpha < 1$), where $m_\alpha$ is a control parameter, normally set to $\alpha_{\max}^{1/2}$. If repeated scaling still fails, it is abandoned altogether in a current iteration of the optimization process, and the design is improved using local tuning (cf. Sect. "Intermittent local tuning") before attempting the scaling process again.

**Intermittent local tuning.** Local tuning is executed after applying the concurrent dimension scaling of Sect. "Concurrent parameter scaling". Its role is to improve the quality of the current design before launching the scaling again, or to finalize the optimization process if the current operating frequency $f_{a.0}$ is sufficiently close to the target $F_{t.0}$. The tuning is realized as the iterative gradient-based algorithm with numerical derivatives[84].

Given the design $\mathbf{x}^{(i)}$ obtained using the scaling procedure (or the previous application of the tuning routine), the new candidate design $\mathbf{x}^{(i+1)}$ is rendered as

$$\mathbf{x}^{(i+1)} = \arg \min_{\substack{\mathbf{x} \in X \\ ||\mathbf{x} - \mathbf{x}^{(i)}|| < d^{(i)}}} U_L(\mathbf{x}, \mathbf{F}_a) \tag{4}$$

where the objective function $U_L$ is defined similarly as the original function $U$ (cf. Sect. "Problem statement"); yet, it is calculated using the linear expansion model of the circuit characteristics

$$\mathbf{L}^{(i)}(\mathbf{x}) = \mathbf{S}(\mathbf{x}^{(i)}) + \mathbf{J}_S(\mathbf{x}^{(i)}) \cdot (\mathbf{x} - \mathbf{x}^{(i)}) \tag{5}$$

The Jacobian matrix $\mathbf{J}_S$ is evaluated using finite differentiation[85]. The vector $\mathbf{F}_a$ is the current target objective vector, defined as
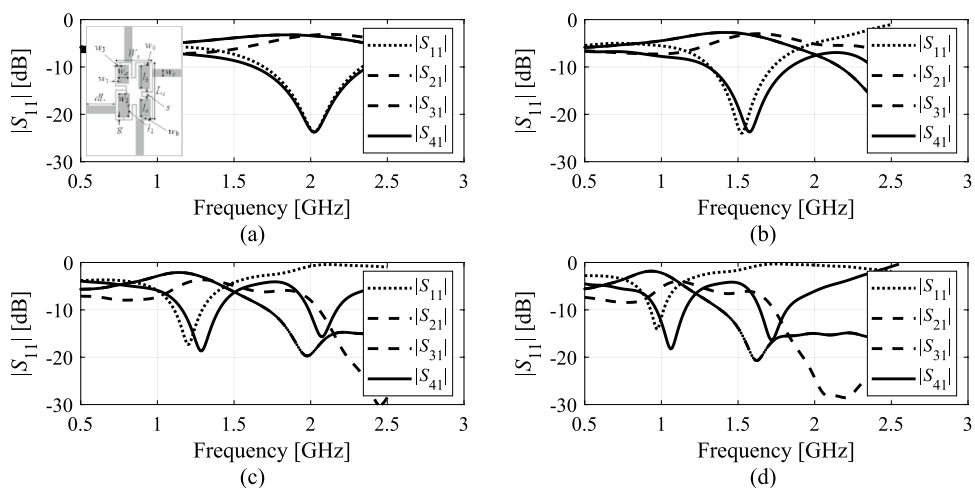


**Figure 2.** Concurrent dimension scaling of a compact branch-line coupler. EM-simulated $S$-parameters at: (**a**) initial design $\mathbf{x}$, (**b**) design obtained as $M_S(\mathbf{x},1.2)$, (**c**) design obtained as $M_S(\mathbf{x},1.4)$, (**d**) design obtained as $M_S(\mathbf{x},1.6)$. Note increasing distortion of electrical characteristics, especially for $\alpha > 1.4$.

$$\boldsymbol{F}_a = \begin{bmatrix} f_{a.0} & F_{t.1} & ... & F_{t.N} \end{bmatrix}^T \tag{6}$$

i.e., it coincides with $\boldsymbol{F}_t$ except the first entry, which is replaced by the existent operating frequency of the circuit extracted at the design $\boldsymbol{x}^{(i)}$. As mentioned before, the tuning step (4), (5) aims at improving the design quality in terms of its performance parameters with respect to the current operating parameters, and prior to executing another round of concurrent scaling.

The size $d^{(i)}$ of the search region is adaptively adjusted contingent upon the gain ratio $r = [U(\boldsymbol{x}^{(i+1)}, \boldsymbol{F}_a) - U(\boldsymbol{x}^{(i)}, \boldsymbol{F}_a)]/[U_L(\boldsymbol{x}^{(i+1)}, \boldsymbol{F}_a) - U_L(\boldsymbol{x}^{(i)}, \boldsymbol{F}_a)]$ (i.e., increased if $r$ is close to 1, and decreased if it is close to zero[84]). Also, the tried design is retained if $r > 0$, i.e., the improvement of the original objective function $U$ (computed using EM simulation data) has been observed.

If $f_{a.0}$ is sufficiently close to $F_{t.0}$, concurrent scaling is no longer executed, and the tuning process (4), (5) is continued until convergence. Here, the termination condition is $\|\boldsymbol{x}^{(i+1)} - \boldsymbol{x}^{(i)}\| < \varepsilon_x$ (when converging in argument), or $d^{(i)} < \varepsilon_x$ (search region reduction); we set $\varepsilon_x = 10^{-3}$.

**Complete optimization procedure.**    This section puts together the entire optimization procedure involving the concurrent scaling of Sect. "Concurrent parameter scaling", and local tuning of Sect. "Intermittent local tuning". The major assumption here is that the initial design $\boldsymbol{x}^{(0)}$ is of sufficient quality to allow successful scaling, i.e., so that the scaled circuit has identifiable operating frequency (cf. Sect. "Concurrent parameter scaling"). This assumption normally holds, because the purpose of the described procedure is circuit re-design. Otherwise, the execution of the procedure should be preceded by local optimization with respect to the current (actual) operational frequency of the circuit.

Table 2 gathers the control parameters of the presented algorithm. It should be noted that we only have three independent parameters $\alpha_{\min}$, $\varepsilon_x$, and $dF_0$. None of these is critical. For example, setting $\alpha_{\min}$ sufficiently close to unity is a safer option (to avoid abrupt design relocations), and the performance of the optimization process will be more or less invariant of the choice. The second parameter decides upon the resolution of the optimization process, whereas the last one can be set as a small fraction (e.g., five percent) of $F_{t.0}$. As a matter of fact, setting $dF_0$ to anything less than half of the expected circuit bandwidth is normally sufficient to ensure adequate operation of the procedure.

Figure 3 presents the pseudocode of the re-design procedure. It can be noted that the concurrent scaling is only performed (Step 6) if the actual center frequency is too far from to the target, i.e., if $|f_{a.0} - F_{t.0}| > dF_0$. If the scaling is unsuccessful, that is, the operating frequency cannon be extracted at the candidate design, it is repeated with the updated scaling coefficient $\alpha_{update}$ (Step 8).

The next stage is local tuning (Step 11), which aims at improving the design quality in terms of the objective function value. At this stage, the circuit is optimized using the objective function $U$ computed for the current center frequency $f_{a.0}$. Local tuning is performed intermittently, following subsequent rounds of concurrent scaling. If the operating frequency of the circuit becomes sufficiently close to the target, concurrent scaling is no longer executed, and the final design is produced through local optimization. For additional explanation, Fig. 4 provides a flow diagram of the proposed algorithm.

## Verification case studies

This section summarizes the results of the numerical experiments conducted to demonstrate the operation and performance of the introduced optimization technique. The experiments were designed to verify the capability of our procedure to handle circuit re-design over wide range of operating frequencies, with the initial design corresponding to the center frequency significantly different from the target one. Under such conditions, conventional local tuning normally fails, which was also corroborated by carrying out the appropriate optimization runs. A remark should be made that all of the benchmark microwave components have been already experimentally validated (both in the source papers[86–89], as well as in our previous work, e.g.,[81]). Thus, the experimental validation of the optimized designs has not been provided, as being immaterial to the scope of the paper.

**Verification circuits.**    Verification experiments have been performed using four compact microstrip couplers shown in Fig. 5. The computational models are implemented and simulated using the time-domain solver of CST Microwave Studio. The important data concerning the structures in Fig. 5 (material parameters of the substrate, independent and dependent geometry parameters, target operating frequencies, initial designs) have been shown in Fig. 6. For all verification structures, we aim at re-designing the circuit from the given initial

| Parameter | Recommended value | Comments |
|---|---|---|
| $\alpha_{\min}$ | 0.7 | Minimum value of the scaling coefficient $\alpha$ for concurrent scaling (cf. Sect. "Concurrent parameter scaling") |
| $\alpha_{\max}$ | $1/\alpha_{\min}$ | Maximum value of the scaling coefficient $\alpha$ for concurrent scaling (cf. Sect. "Concurrent parameter scaling") |
| $m_\alpha$ | $\alpha_{\max}^{1/2}$ | Updating factor for the scaling coefficient $\alpha$ |
| $\varepsilon_x$ | $10^{-3}$ | Termination threshold (cf. Sec. "Intermittent local tuning") |
| $dF_0$ | $0.05 \cdot F_{t.0}$ | Concurrent scaling threshold (scaling enabled if $|f_{a.0} - F_{t.0}| > dF_0$) |

**Table 2.** Proposed optimization procedure: Control parameters.

1.  Input arguments:
    - $\boldsymbol{x}^{(0)}$ – initial design,
    - $\boldsymbol{F}_t$ – target operating vector,
    - $X$ – parameter space,
    - $U$ – objective function;
2.  Set the iteration index $i = 0$;
3.  Evaluate circuit responses $\boldsymbol{S}(\boldsymbol{x}^{(i)})$;
4.  Evaluate response Jacobian $\boldsymbol{J}_S(\boldsymbol{x}^{(i)})$;
5.  Extract operating frequency $f_{a.0}(\boldsymbol{x}^{(i)})$;
6.  **If** $|f_{a.0} - F_{t.0}| > dF_0$
    > Obtain scaled design $\boldsymbol{x}_{tmp} = M_S(\boldsymbol{x}^{(i)}, \alpha)$;

    **else**
    > Set $f_{a.0} = F_{t.0}$;
    > Go to 11;

    **end**
7.  Extract operating frequency $f_{a.tmp}(\boldsymbol{x}_{tmp})$;
8.  **If** Operating frequency extraction failed (e.g., due to distorted response)
    > Obtain scaled design $\boldsymbol{x}_{tmp} = M_S(\boldsymbol{x}^{(i)}, \alpha_{updated})$;
    > Extract operating frequency $f_{a.tmp}(\boldsymbol{x}_{tmp})$;
    > **If** Operating frequency extraction failed
    > > Go to 11;

    > **end**

    **end**
9.  Set $\boldsymbol{x}^{(i)} = \boldsymbol{x}_{tmp}$ and $f_{a.0} = f_{a.tmp}$;
10. Set $\boldsymbol{F}_a = [f_{a.0}\ F_{t.1}\ \dots\ F_{t.N}]^T$;
11. Find candidate design $\boldsymbol{x}^{(i+1)}$ (cf. (4), (5))

$$\boldsymbol{x}^{(i+1)} = \arg \min_{\substack{\boldsymbol{x} \in X \\ \|\boldsymbol{x} - \boldsymbol{x}^{(i)}\| < d^{(i)}}} U_L(\boldsymbol{x}, \boldsymbol{F}_a)$$

12. Evaluate circuit responses $\boldsymbol{S}(\boldsymbol{x}^{(i+1)})$;
13. Evaluate gain ratio $r = [U(\boldsymbol{x}^{(i+1)},\boldsymbol{F}_a) - U(\boldsymbol{x}^{(i)},\boldsymbol{F}_a)]/[U_L(\boldsymbol{x}^{(i+1)},\boldsymbol{F}_a) - U_L(\boldsymbol{x}^{(i)},\boldsymbol{F}_a)]$;
14. Update search radius $d^{(i)}$;
15. **If** $r > 0$
    > Set $i = i + 1$;

    **end**
16. **If** Termination condition
    > Go to 17;

    **else**
    > Go to 4;

    **end**
17. END.

**Figure 3.** Pseudocode of the proposed re-design algorithm with concurrent parameter scaling and intermittent local tuning.

design to the center frequency listed in the table as $F_{t.0}$. The design task is formulated as in Table 1 (second row). For Circuits I through III, the target power split ratio is 0 dB, whereas for Circuit IV, it is 3 dB. The target operating vector is $\boldsymbol{F}_t = [F_{t.0}\ F_{t.1}\ F_{t.2}]^T$, where $F_{t.0} = f_0$ is the center frequency, $F_{t.1} = K$ is the target power split ratio, whereas $F_{t.2} = \varepsilon_r$ is the substrate permittivity.

Observe that the proposed optimization method is a general one and may be successfully applied for design optimization of verification structures other than those presented in Fig. 5, such as, e.g., antenna structures. The sole limitation of the introduced optimization technique is that it is capable of handling single-band structures. A generalization for multi-band systems will be a focus of the future work.
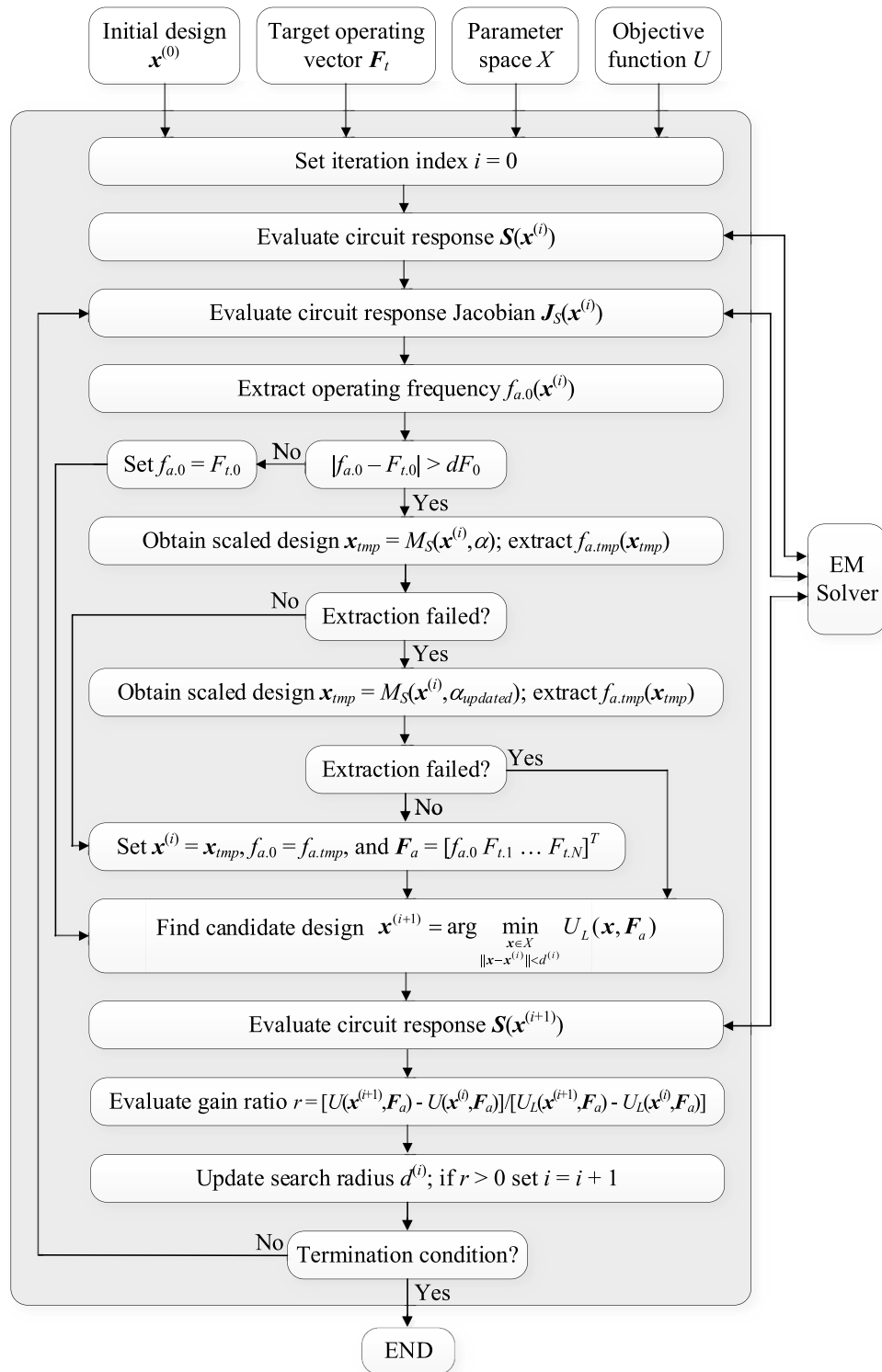
**Figure 4.** Flow diagram of the proposed re-design algorithm with concurrent parameter scaling and intermittent local tuning.

**Numerical results and discussion.** The procedure of Sect. "Circuit re-design using concurrent scaling and intermittent local tuning" along with the conventional gradient-based search[84] have been applied to optimization of Circuits I, II, III, and IV. In all cases, local tuning starting from the initial designs listed in Table 3 failed, i.e., the algorithm was unable to identify the designs featuring the required operating frequency. On the other hand, the proposed procedure turned successful for all circuits. Table 3 provides information about the final designs, as well as the actual operating conditions therein.
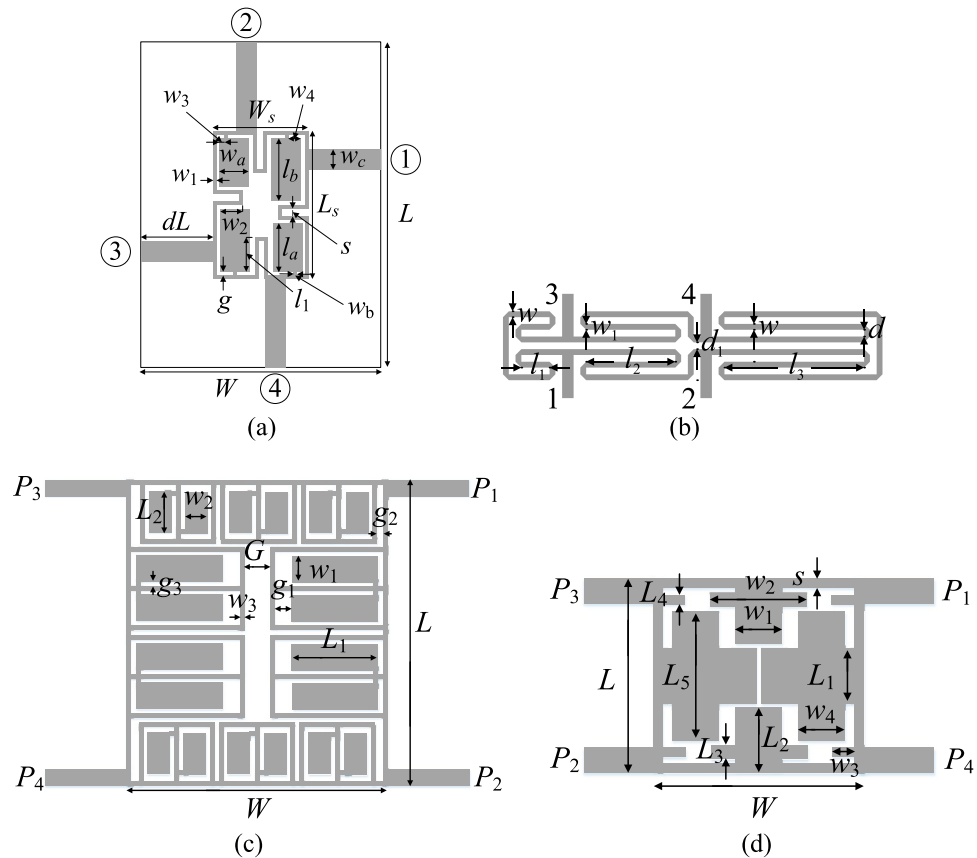
**Figure 5.** Microstrip couplers employed as verification case studies to validate the re-design procedure proposed in this work: (**a**) Circuit I: miniaturized branch-line coupler (BLC)[86], (**b**) Circuit II: rat-race coupler of transmission lines folded[87], (**c**) Circuit III: BLC with microstrip cells[88], (**d**) Circuit IV: compact BLC (non-equal power split)[89].

It can be observed that both the operational frequency as well as power split ratio are well aligned with the targets. The misalignment of the center frequency is less than one percent, whereas the power division error is below or equal to 0.15 dB (it is much lower for Circuits III and IV). It should also be emphasized that the latter can be further reduced by increasing the penalty coefficient associated with the power-split-related penalty function (at the expense of slightly misaligned center frequency). At the same time, the circuit matching and isolation is also well controlled (typically, $|S_{11}|$ and $|S_{41}|$ are well below –20 dB at the target frequency $F_{t.0}$). Finally, computational efficiency of our algorithm is excellent. The cost of the optimization process corresponds to only 104, 130, 61, and 135 EM simulations of Circuits I through IV, respectively (the average of 107). This corresponds to the typical cost of local gradient-based tuning. These expenses are low given significant relocation of the designs, normally achievable with the use of global search procedures.

A comment should be made concerning the scalability of the presented method. Based on the presented evidence of four test cases of the dimensionality ten, six, nine, and twelve parameters, as well as the cost of design optimization procedure (104, 130, 61 and 135 EM analyses per design), it might be estimated that the computational expenses are around ten times larger than the number of the design variables, which can be considered as low. In general, our procedure exhibits complexity typical for gradient-based algorithms employing first-order sensitivities, i.e., the dependence of the computational cost on the number of design variables is slightly higher than linear. In other words, the cost of the proposed procedure is comparable to that of the local optimization routines, and, as such, may be considered as practically acceptable, even for problems described by as high as twenty parameters.

Figures 7, 8, 9 and 10 show the circuit responses at the initial and final designs, as well as the responses at the designs obtained by the first round of concurrent scaling, along with the evolution of the current operational frequency of the coupler throughout the optimization run. It should be emphasized that despite large discrepancies between the operating frequency at the initial designs and the targets, the proposed algorithm ensures good alignment of $f_{a.0}$ and $F_{t.0}$ after just five iterations. The remaining computational budget is utilized to improve the objective function value at $F_{t.0}$. Finally, it should also be mentioned that the results are consistent

| | Case study | | | |
|---|---|---|---|---|
| | Circuit I | Circuit II | Circuit III | Circuit IV |
| Substrate | AD300 $(\varepsilon_r = 2.97, h = 0.76$ mm) | RO4003 $(\varepsilon_r = 3.38, h = 0.762$ mm) | FR4 $(\varepsilon_r = 4.4, h = 1.0$ mm) | FR4 $(\varepsilon_r = 4.4, h = 1.0$ mm) |
| Design parameters | $\boldsymbol{x} = [g \; l_{1r} \; l_a \; l_b \; w_1 \; w_{2r} \; w_{3r} \; w_{4r} \; w_a \; w_b]^T$ | $\boldsymbol{x} = [l_1 \; l_2 \; l_3 \; d \; w \; w_1]^T$ | $\boldsymbol{x} = [G \; g_1 \; g_2 \; g_3 \; w_1 \; w_3 \; L_1 \; L_2]^T$ | $\boldsymbol{x} = [W \; w_{1\_r} \; w_{2\_r} \; w_3 \; w_4 \; L \; L_{1\_r} \; L_{2\_r} \; L_3 \; L_4 \; L_{5\_r} \; s]^T$ |
| Other parameters | $L = 2dL + L_s$, $L_s = 4w_1 + 4g + s + l_a + l_b$, $W = 2dL + W_s$, $W_s = 4w_1 + 4g + s + 2w_a$, $l_1 = l_b l_{1r}$, $w_2 = w_a w_{2r}$, $w_3 = w_{3r} w_a$, and $w_4 = w_{4r} w_a$, $w_c = 1.9$ mm | $d_1 = d + |w - w_1|$, $d = 1.0$, $w_0 = 1.7$, and $l_0 = 15$ mm | $L = 4w_1 + 10w_3 + 15g_3 + 2L_2$, $W = 4w_3 + 2L_1 + G + 2g_1 + 2g_3$ | - |
| Target operating frequency | $f_0 = 1$ GHz | $f_0 = 1$ GHz | $f_0 = 2$ GHz | $f_0 = 1.2$ GHz |
| Target power division ratio | $K = 0$ dB | $K = 0$ dB | $K = 0$ dB | $K = 3$ dB |
| Initial design | $\boldsymbol{x}^{(0)} = [0.5 \; 0.52 \; 7.0 \; 8.5 \; 0.5 \; 0.4 \; 0.15 \; 0.15 \; 2.0 \; 0.3]^T$ | $\boldsymbol{x}^{(0)} = [5.3 \; 13.3 \; 21.5 \; 0.96 \; 0.89 \; 0.90]^T$ | $\boldsymbol{x}^{(0)} = [1.0 \; 1.0 \; 0.6 \; 0.25 \; 2.4 \; 0.25 \; 9.0 \; 3.75]^T$ | $\boldsymbol{x}^{(0)} = [12.0 \; 0.5 \; 0.8 \; 3.0 \; 2.4 \; 12.0 \; 0.4 \; 0.6 \; 1.2 \; 1.0 \; 0.8 \; 0.51]^T$ |
| Operating parameter at $\boldsymbol{x}^{(0)}$ | $f_{a.0} = 2.2$ GHz $K = 1.2$ dB | $f_{a.0} = 2.1$ GHz $K = 0.2$ dB | $f_{a.0} = 1.05$ GHz $K = 1$ dB | $f_{a.0} = 2.7$ GHz $K = 3$ dB |

**Figure 6.** Microwave couplers used for validating of the proposed re-design procedure.

for all considered circuits. On the one hand, this demonstrates the overall efficacy of the presented framework. On the other hand, it shows that problem-specific tuning of the control parameters (cf. Table 2) is not necessary.

The procedure introduced in this work has been developed for handling single-band structures. Its generalization for multi-band circuits poses certain challenges, because concurrent parameter scaling as described in Sect. "Concurrent parameter scaling" would be inadequate here, due to synchronized relocation of the operating bands it would incur. The aim of the forthcoming work will be to generalize this stage of the process to allow "orthogonal" scaling of geometry variables in order to enable independent control over several center frequencies.

## Conclusion

The paper outlined a novel technique for reliable re-design of microwave passives over broad ranges of operating frequencies. Our methodology utilizes a scope-controlled concurrent scaling of geometry parameters interleaved with local tuning. The former enables large design relocations at minimum computational expenses, whereas the latter allows for a continuous improvement of the design with regard to the assumed performance figures. Both mechanisms have been incorporated into an optimization framework controlled by a few user-defined and easily adjustable parameters. Comprehensive verification involving four compact microstrip couplers demonstrated superior efficacy of the procedure, both in terms of reliability, and computational efficiency. In particular, it permits a precise control of the center frequencies and other electrical performance figures (here, a power division ratio), while being able to re-design the structures to operating frequencies distant from those at the initial designs. The cost of the optimization procedure slightly exceeds one hundred EM evaluations of the device under design, thus, it is equivalent to the expenses associated with a local gradient-based search. At the same time, straightforward local optimization failed for all test circuits, which indicates, that—for the considered design scenarios—global search routines would normally be necessary.

The presented technique has been developed to handle single-band circuits, which is a practical limitation as contemporary applications often require dual-, triple-, or even quad-band structures. Generalization of the method for multi-band systems poses considerable challenges. In particular, simple concurrent parameter scaling results in more-or-less synchronized adjustment of the operating bands. Enabling independent control requires more sophisticated strategies, involving a number of scaling directions, which are "orthogonal" to each other in terms of their effects on particular operating frequencies. The focus of the future work will be the conceptual development and implementation of the respective design framework, as well as its verification using real-world test cases.

| Circuit | Target operating parameters | | Actual operating parameters | | Geometry parameter values | Computational cost |
|---|---|---|---|---|---|---|
| | Center frequency $f_0$ [GHz] | Power split ratio $K$ [dB] | Center frequency $f_0$ [GHz] | Power split ratio $K$ [dB] | | |
| I | 1.0 | 0.0 | 1.0 | 0.15 | $x^* = [0.72\ 0.62\ 11.7\ 15.9\ 1.37\ 0.68\ 0.41\ 0.35\ 4.53\ 0.60]^T$ | 104 |
| II | 1.0 | 0.0 | 1.0 | 0.1 | $x^* = [5.53\ 14.4\ 22.0\ 1.07\ 0.90\ 0.85]^T$ | 130 |
| III | 2.0 | 0.0 | 2.0 | 0.0 | $x^* = [1.10\ 1.01\ 0.74\ 0.11\ 1.23\ 0.35\ 6.09\ 2.02]^T$ | 61 |
| IV | 1.2 | 3.0 | 1.2 | 3.0 | $x^* = [21.7\ 0.53\ 0.69\ 3.86\ 0.64\ 23.0\ 0.22\ 0.45\ 0.56\ 0.55\ 0.52\ 0.33]^T$ | 135 |

| | Case study | | | |
|---|---|---|---|---|
| | Circuit I | Circuit II | Circuit III | Circuit IV |
| Substrate | AD300 ($\varepsilon_r = 2.97$, $h = 0.76$ mm) | RO4003 ($\varepsilon_r = 3.38$, $h = 0.762$ mm) | FR4 ($\varepsilon_r = 4.4$, $h = 1.0$ mm) | FR4 ($\varepsilon_r = 4.4$, $h = 1.0$ mm) |
| Design parameters | $x = [g\ l_{1r}\ l_a\ l_b\ w_1\ w_{2r}\ w_{3r}\ w_{4r}\ w_a\ w_b]^T$ | $x = [l_1\ l_2\ l_3\ d\ w\ w_1]^T$ | $x = [G\ g_1\ g_2\ g_3\ w_1\ w_3\ L_1\ L_2]^T$ | $x = [W\ w_{1\_r}\ w_{2\_r}\ w_3\ w_4\ L\ L_{1\_r}\ L_{2\_r}\ L_3\ L_4\ L_{5\_r}s]^T$ |
| Other parameters | $L = 2dL + L_s$, $L_s = 4w_1 + 4\,g + s + l_a + l_b$, $W = 2dL + W_s$, $W_s = 4w_1 + 4\,g + s + 2w_a$, $l_1 = l_b l_1{}_r$, $w_2 = w_a w_{2r}$, $w_3 = w_{3r} w_a$, and $w_4 = w_{4r} w_a$, $w_c = 1.9$ mm | $d_1 = d + |w - w_1|$, $d = 1.0$, $w_0 = 1.7$, and $l_0 = 15$ mm | $L = 4w_1 + 10w_3 + 15g_3 + 2L_2$, $W = 4w_3 + 2L_1 + G + 2g_1 + 2g_3$ | - |
| Target operating frequency | $f_0 = 1$ GHz | $f_0 = 1$ GHz | $f_0 = 2$ GHz | $f_0 = 1.2$ GHz |
| Target power division ratio | $K = 0$ dB | $K = 0$ dB | $K = 0$ dB | $K = 3$ dB |
| Initial design | $x^{(0)} = [0.5\ 0.52\ 7.0\ 8.5\ 0.5\ 0.4\ 0.15\ 0.15\ 2.0\ 0.3]^T$ | $x^{(0)} = [5.3\ 13.3\ 21.5\ 0.96\ 0.89\ 0.90]^T$ | $x^{(0)} = [1.0\ 1.0\ 0.6\ 0.25\ 2.4\ 0.25\ 9.0\ 3.75]^T$ | $x^{(0)} = [12.0\ 0.5\ 0.8\ 3.0\ 2.4\ 12.0\ 0.4\ 0.6\ 1.2\ 1.0\ 0.8\ 0.51]^T$ |
| Operating parameter at $x^{(0)}$ | $f_{a.0} = 2.2$ GHz $K = 1.2$ dB | $f_{a.0} = 2.1$ GHz $K = 0.2$ dB | $f_{a.0} = 1.05$ GHz $K = 1$ dB | $f_{a.0} = 2.7$ GHz $K = 3$ dB |

**Table 3.** Optimization results for Circuits I through IV.
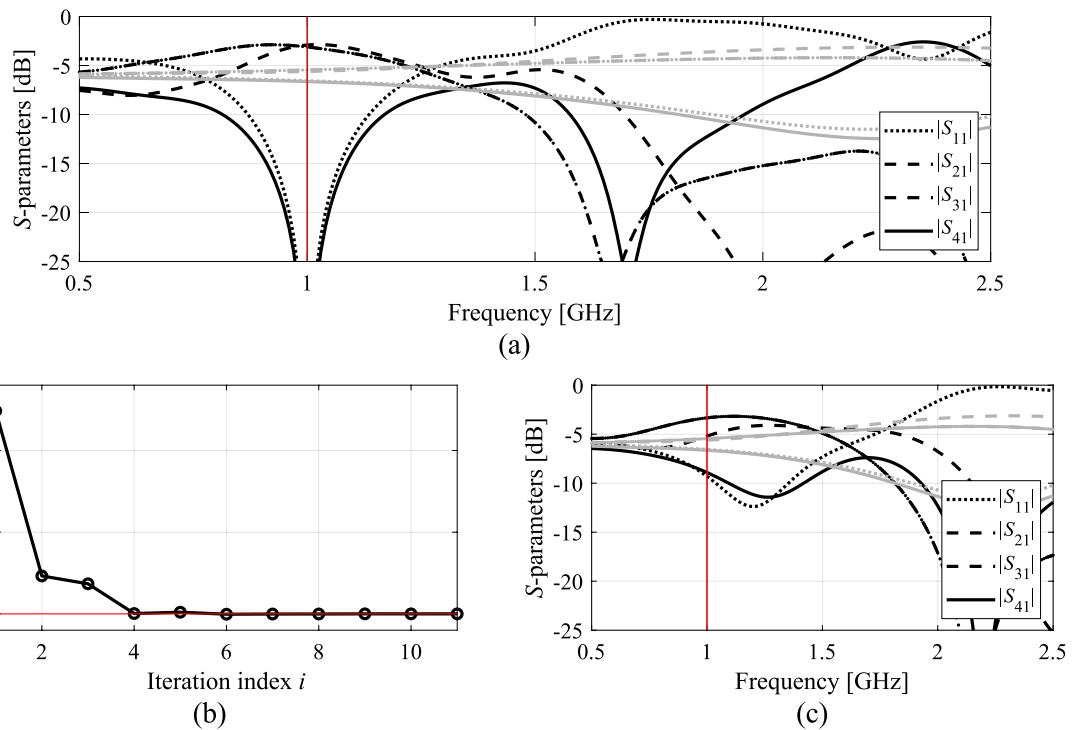


**Figure 7.** Optimization results for Circuit I: (**a**) EM-evaluated $S$-parameters at the optimized (black) and initial design (grey); (**b**) evolution of the operating frequency $f_{a.0}$; (**c**) $S$-parameters upon first concurrent scaling (black) versus responses at the initial design (grey).
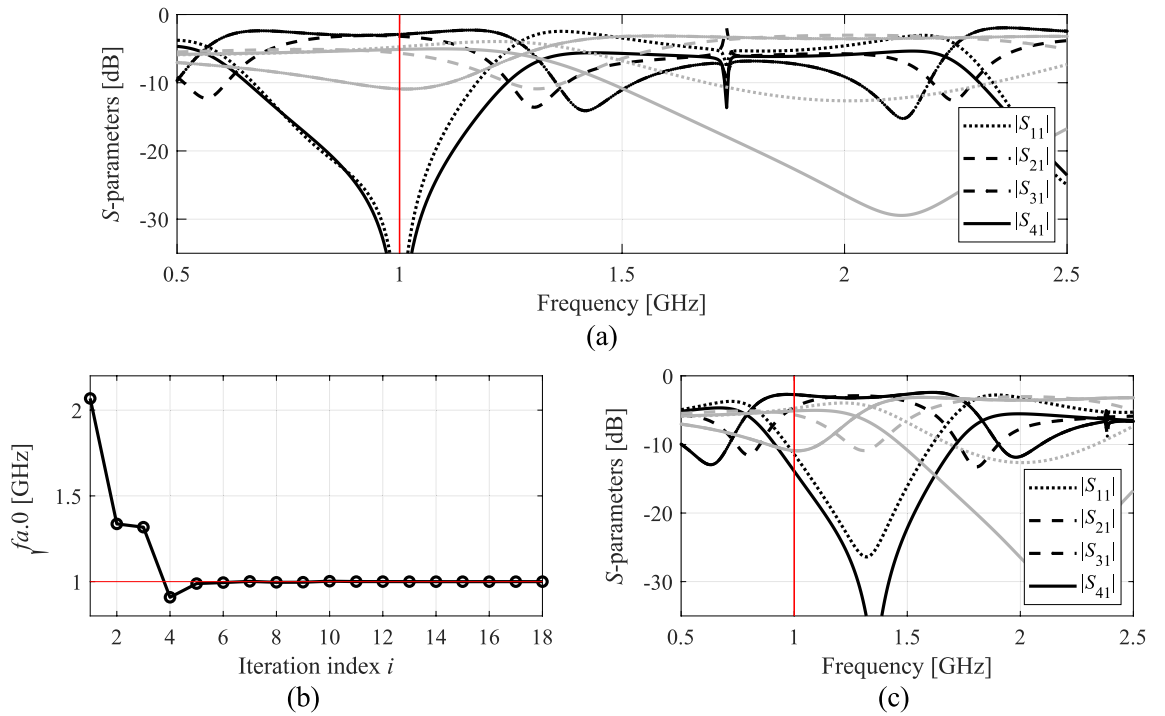
**Figure 8.** Optimization results for Circuit II: (**a**) EM-evaluated *S*-parameters at the optimized (black) and initial design (grey); (**b**) evolution of the operating frequency $f_{a.0}$; (**c**) *S*-parameters upon first concurrent scaling (black) versus responses at the initial design (grey).
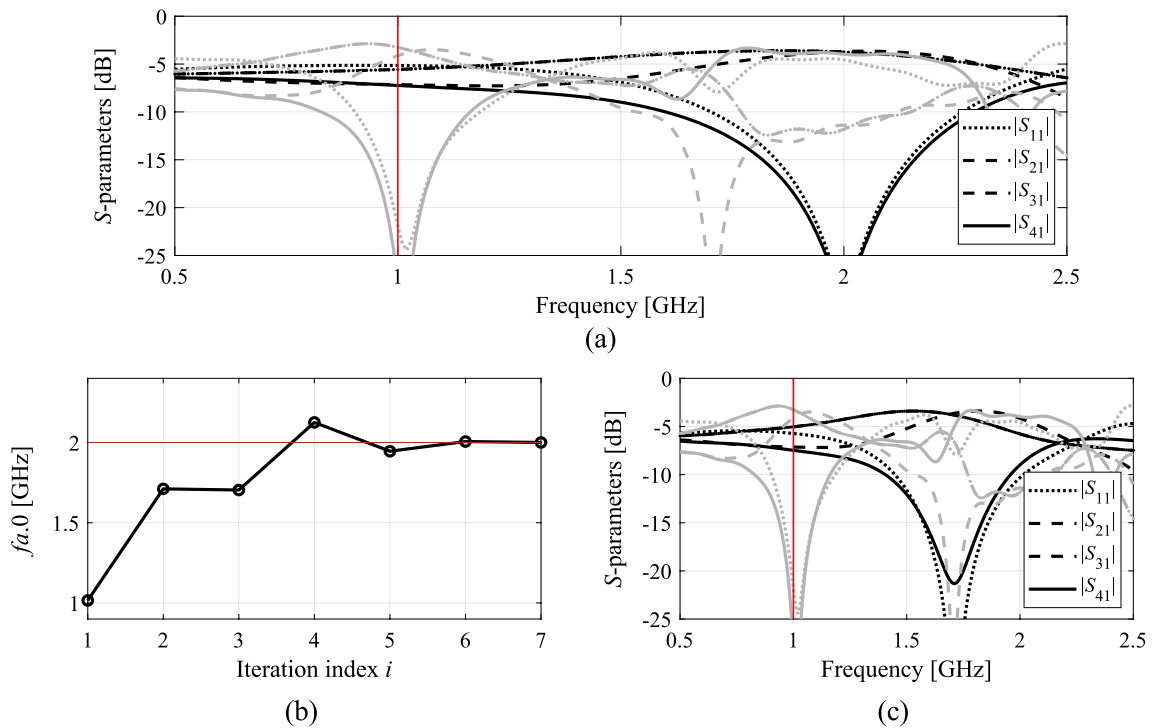


**Figure 9.** Optimization results for Circuit III: (**a**) EM-evaluated *S*-parameters at the optimized (black) and initial design (grey); (**b**) evolution of the operating frequency $f_{a.0}$; (**c**) *S*-parameters upon first concurrent scaling (black) versus responses at the initial design (grey).
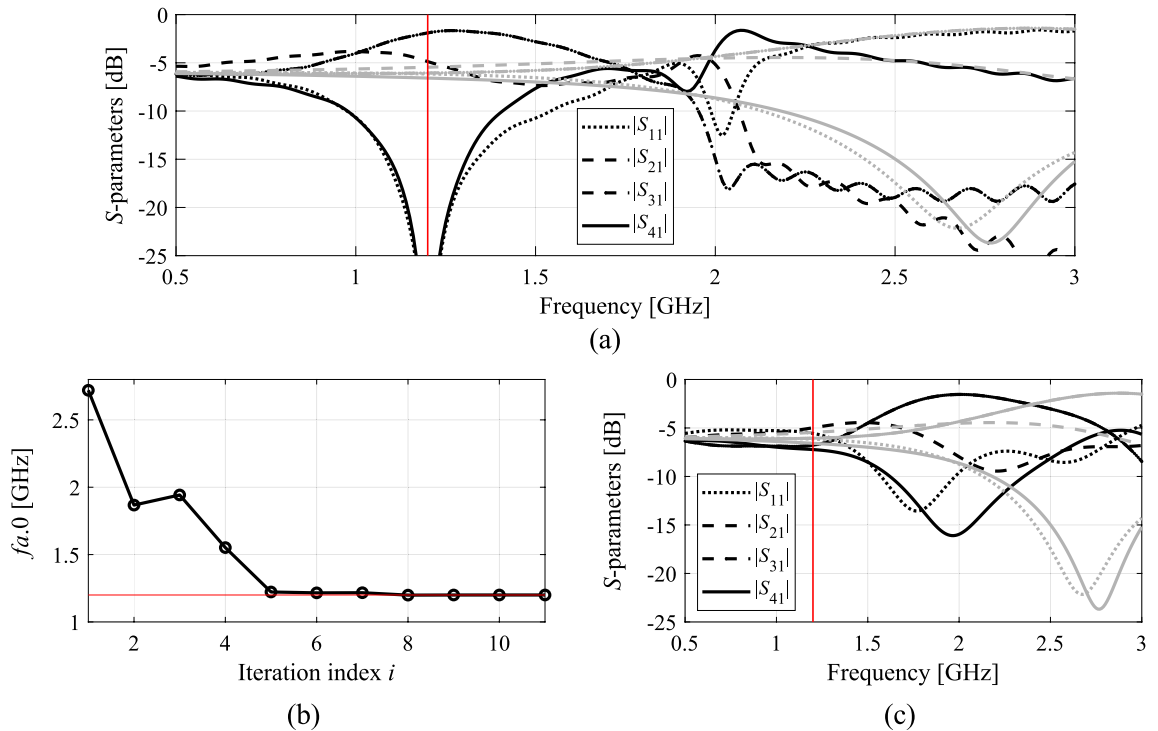
**Figure 10.** Optimization results for Circuit IV: (**a**) EM-evaluated *S*-parameters at the optimized (black) and initial design (grey); (**b**) evolution of the operating frequency $f_{a.0}$; (**c**) *S*-parameters upon first concurrent scaling (black) versus responses at the initial design (grey).

## Data availability
The datasets generated during and/or analysed during the current study are available from the corresponding author on reasonable request.

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Conceptualization, A.P. and S.K.; methodology, A.P. and S.K.; software, A.P. and S.K.; validation, A.P. and S.K.; formal analysis, S.K.; investigation, A.P. and S.K.; resources, S.K.; data curation, A.P. and S.K.; writing—original draft preparation A.P. and S.K.; writing—review and editing, A.P. and S.K.; visualization, A.P. and S.K.; supervision, S.K.; project administration, S.K.; funding acquisition, S.K, All authors reviewed the manuscript.

## Competing interests

The authors declare no competing interests.

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