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# Space-vector pulsewidth modulation for a seven-level cascaded H-bridge inverter with the control of DC-link voltages

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**Abstract.** A control strategy of DC-link voltages for a seven-level cascaded H-bridge inverter is proposed in this paper. The DC-link voltage balancing is accomplished by an appropriate selection of H-bridges and control of their duty cycles in space-vector modulation (SVM) algorithm. The proposed SVM method allows to maintain the same voltage level on all inverter capacitors. Regardless of the balancing function, the SVM strategy makes it possible to generate the output voltage vector properly also in the case where the DC-link voltages are not balanced. The results of simulation and experimental investigations are presented in the paper.

**Key words:** cascaded H-bridge inverter, DC-link voltage control, space vector modulation.

## 1. Introduction

The main advantages of multilevel (ML) inverters are the improved quality of voltage waveforms and an increase in the output voltage for a given blocking voltage capacity of the semiconductors. One of the most interesting constructions can be found in the cascaded H-bridge (CHB) converters [1]. They are composed of low-voltage H-bridges connected serially, with the semiconductor blocking voltages much lower than the nominal output voltage of the converter. The inverter output voltage is the sum of the output voltages of individual H-bridges. Increasing the value of inverter output voltage requires only an increase in the amount of H-bridges connected in a series.

The CHB converters require galvanically isolated power sources [2]. The DC-link circuits of the H-bridges can be supplied by rectifiers connected to a multi-pulse transformer [1] as well as to single-phase transformers [3]. The energy can also be delivered to the DC-links using isolated dual-active bridges (DABs) with high frequency (HF) or medium frequency (MF) transformers [4]. Compared to classic transformers, the HF and MF transformers are smaller, lighter and cheaper.

The DC-link voltages of the CHB converter should be maintained at the same level. These voltages depend on delivered energy and the load. In the case of the CHB converters, where the electrical energy is transferred between rectifier and inverter through the DAB converters, the ability to maintain the same voltages on all DC-link capacitors also depends on DAB nominal power and on modulation strategies applied to both CHB inverter and CHB rectifier.

The most popular modulation strategies, applied to CHB converters, are carrier-based sinusoidal pulse width modulation (SPWM) [5, 6] and non-carrier-based selective-harmonic-elimination pulse width modulation (SHE-PWM) [7]. The space-vector pulse width modulation (SVM) strategies for more than three-level inverters are more complex due to the large amount of space vectors [8, 9]. Usually, the SVM strategies for CHB converters utilize three space vectors nearest to the sector in which the reference voltage vector is located [10, 11]. Some of proposed SVM strategies concentrate on generating the output voltage vector in the CHB inverters, wherein the DC-link voltages are not equalized [12].

The changes in DC-link voltages of CHB inverter are the results of current flow through the DC-link capacitors. The DC-link voltages can be balanced in several ways. The most popular methods are based on managing the H-bridges used to compose the inverter output voltage [7], on modifying the individual reference voltages as well as on changing modulation indexes of the H-bridges [8, 13, 14]. The DC-link voltages are usually balanced using controllers [8, 15], but it is also possible to rotate the carrier signals for every modulation cycle between H-bridges of CHB converter in carrier-based modulation strategies [16].

The CHB inverters are mainly applied in medium and high-power applications, where it is particularly important to convert electrical energy with maximum efficiency. In CHB inverters, it is possible to assume maximum value of the modulation indexes for selected H-bridges [17]. The output voltage is modulated in one H-bridge only in each of the inverter phases. The other H-bridges are positively or negatively connected or are bypassed [18]. Since their transistors do not switch, they do not generate commutation loses.

In this paper, the DC-link balancing method and SVM strategy for seven-level CHB converters is proposed. Because the SVM strategies for more than three-level inverters are relatively complex [8, 9], the topology of the seven-level CHB converter is analyzed as a set of 3 three-level CHB converters connected in series. Each of them is composed using three H-bridges (one H-bridge in each phase of the inverter) and controlled using one of the three proposed SVM patterns.

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In medium and high-power applications, it is particularly important to convert electrical energy with reduced losses. In phase-disposition SPWM strategies, it is possible to assume maximum value of the modulation indexes for selected H-bridges of CHB inverter [17], while the other H-bridges modulate their output voltages. The balancing of DC-link voltages is usually carried out based on managing the H-bridges used to build the inverter output voltage [7]. In the proposed SVM strategy, the DC-link voltage balancing is realized by appropriate selection of the H-bridges used to compose the three-level converters, and also by control of their duty cycles. The choice of SVM pattern, used to generate the inverter output voltage also provides reduction of the DC-link voltage unbalance. In the proposed solution, only three H-bridges modulate the output voltages. The other H-bridges are forced to be in active state (positively or negatively connected) or bypassed.

Regardless of the balancing function, the asymmetric DC-link voltage distribution is taken into account and the output voltage is generated correctly, also when the DC-link voltages are not the same. The results of simulation and experimental tests of the proposed control method are presented in this paper.

## 2. The structure of a seven-level CHB converter

The seven-level CHB converter is composed of three H-bridges connected in series in any of the phases (Fig. 1). The DC-link circuits of the H-bridges have to be galvanically isolated. It can be achieved using dual-active bridges (DABs) with HF or MF transformers used to energy transfer between DC-link capacitors of CHB inverter and rectifier. The topology of the seven-level CHB converter with DABs is shown in Fig. 1, and a detailed configuration of DAB coupler is presented in Table 1. The structure of H-bridges of CHB inverter and CHB rectifier is presented in Fig. 2.

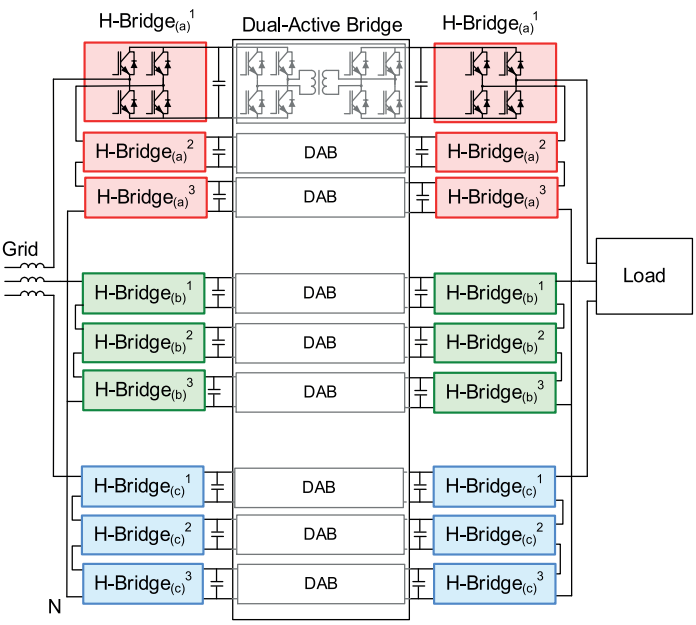


Fig. 1. The structure of seven-level CHB converter with isolated dual-active bridges

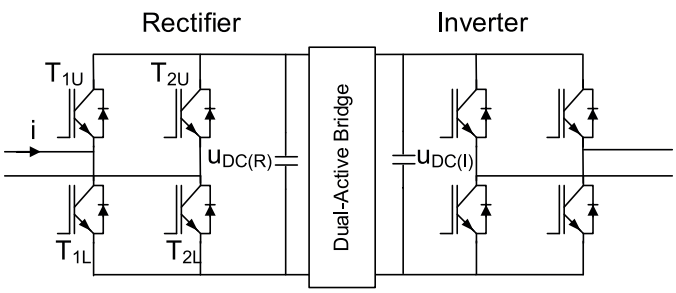


Fig. 2. The H-bridges of CHB inverter (I) and rectifier (R)

Table 1
The configuration of a seven-level CHB converter with isolated dual active bridges (DABs)

| H-Bridge$_{(q)}^{j}$ (recitifier) | connected to (via the DAB) | H-Bridge$_{(p)}^{i}$ (inverter) |
|---|---|---|
| H-Bridge$_{(a)}^{1}$ | ↔ | H-Bridge$_{(a)}^{1}$ |
| H-Bridge$_{(b)}^{1}$ | ↔ | H-Bridge$_{(b)}^{1}$ |
| H-Bridge$_{(c)}^{1}$ | ↔ | H-Bridge$_{(c)}^{1}$ |
| H-Bridge$_{(a)}^{2}$ | ↔ | H-Bridge$_{(b)}^{2}$ |
| H-Bridge$_{(b)}^{2}$ | ↔ | H-Bridge$_{(c)}^{2}$ |
| H-Bridge$_{(c)}^{2}$ | ↔ | H-Bridge$_{(a)}^{2}$ |
| H-Bridge$_{(a)}^{3}$ | ↔ | H-Bridge$_{(c)}^{3}$ |
| H-Bridge$_{(b)}^{3}$ | ↔ | H-Bridge$_{(a)}^{3}$ |
| H-Bridge$_{(c)}^{3}$ | ↔ | H-Bridge$_{(b)}^{3}$ |

Any of the H-bridges can be configured to operate in active and zero state. While the zero state is activated, both upper or both lower transistors are switched on. The DC-link capacitor is bypassed and its voltage does not change.

When the active state is switched-on, two transistors $T_{1U}$, $T_{2L}$ (for the positive output voltage) or $T_{2U}$, $T_{1L}$ (for the negative output voltage) are activated (Fig. 2). The current flow causes a change in the DC-link voltage depending on the current value and H-bridge output voltage:

$$\begin{aligned} &\text{if } i \cdot u_0 > 0 \Rightarrow u_{dc} \uparrow\uparrow, \\ &\text{if } i \cdot u_0 < 0 \Rightarrow u_{dc} \downarrow\downarrow, \end{aligned} \tag{1}$$

where: $i$ is the H-bridge current, $u_o$ is H-bridge output voltage.

The DC-link voltages also depend on the DAB currents. In the presented solution, the DAB currents are not taken into account.

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## 3. The output voltage of a single H-bridge

The H-bridge output voltage can be adjusted by controlling the duty cycle. The durations of active and zero states can be determined as:

$$t_{active} = \gamma \cdot T_{pulse}, \qquad t_{zero} = T_{pulse} - t_{active}, \tag{2}$$

where: $t_{active}$, $t_{zero}$ are the durations of active and zero states, $T_{pulse}$ is a pulse period.

The duty cycle $\gamma$ can be calculated as:

$$\gamma = \frac{|u_0|}{u_{DC}}, \tag{3}$$

where: $u_{DC}$ is a DC-link voltage, and:

$$0 \leq \gamma \leq 1. \tag{4}$$

If the duty cycle is equal to zero or to one ($\gamma = 0$ or $\gamma = 1$) the zero or active state is turned on throughout the entire pulse period $T_{pulse}$ and the H-bridge transistors are not switched. The H-bridge output voltage can be calculated as:

$$u_o = u_{DC} \cdot (T_{1U} - T_{2U}), \tag{5}$$

where: $T_{1U}$, $T_{2U}$ are the gate signals for the upper transistors (Fig. 2) with the values: 1 – upper transistor is switched on, 0 – lower transistor is activated.

The output voltage of actively connected or bypassed H-bridge can be equal to:

$$\begin{aligned} u_o &= \phantom{-}u_{DC} \Leftrightarrow T_{1U} = 1,\ T_{2U} = 0, \\ u_o &= -u_{DC} \Leftrightarrow T_{1U} = 0,\ T_{2U} = 1, \\ u_o &= \phantom{-}0 \quad \Leftrightarrow T_{1U} = 0,\ T_{2U} = 0, \text{ or } T_{1U} = 1,\ T_{2U} = 1. \end{aligned} \tag{6}$$

If the duty cycle is within the range ($0 < \gamma < 1$), the zero and active states are switched-on during the pulse period. The choice of zero state should provide a minimum amount of transistor switching required to generate the H-bridge output voltage.

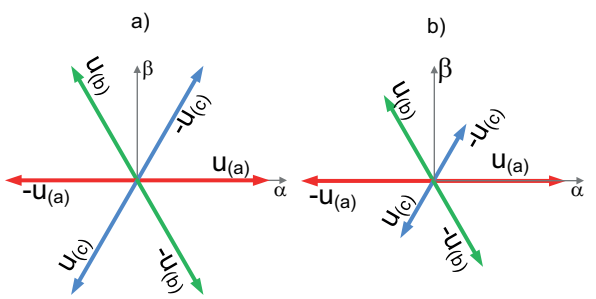


Fig. 3. Output voltage vectors generated by three H-bridges in the case of balanced ($u_{DC(a)} = u_{DC(b)} = u_{DC(c)}$) (a) and unbalanced ($u_{DC(c)} < u_{DC(b)} < u_{DC(a)}$) (b) DC-link voltages

## 4. The output voltages of three H-bridges

The output voltages can be generated simultaneously in three H-bridges (one H-bridge in any of the CHB phases). The components of output voltage vectors, generated in these three H-bridges, can be determined using (5) and the Clarke's transformation. As a result, it can be written as:

$$\begin{aligned} u_{\alpha(a)} &= \sqrt{\frac{2}{3}} \cdot u_{DC(a)} \cdot \left(T_{1U(a)} - T_{2U(a)}\right), \quad u_{\beta(a)} = 0, \\ u_{\alpha(b)} &= \sqrt{\frac{2}{3}} \cdot u_{DC(b)} \cdot cos\left(\frac{2\pi}{3}\right) \cdot \left(T_{1U(b)} - T_{2U(b)}\right), \\ u_{\beta(b)} &= \sqrt{\frac{2}{3}} \cdot u_{DC(b)} \cdot sin\left(\frac{2\pi}{3}\right) \cdot \left(T_{1U(b)} - T_{2U(b)}\right), \\ u_{\alpha(c)} &= \sqrt{\frac{2}{3}} \cdot u_{DC(c)} \cdot cos\left(\frac{4\pi}{3}\right) \cdot \left(T_{1U(c)} - T_{2U(c)}\right), \\ u_{\beta(c)} &= \sqrt{\frac{2}{3}} \cdot u_{DC(c)} \cdot sin\left(\frac{4\pi}{3}\right) \cdot \left(T_{1U(c)} - T_{2U(c)}\right), \end{aligned} \tag{7}$$

where: $u_{\alpha(p)}$, $u_{\beta(p)}$ are the components of output voltage vector generated in the "$p$" phase H-bridge ($p = a,\ b\ or\ c$), $T_{1U(p)}$, $T_{2U(p)}$ are the gate signals for the upper transistors in $p$-phase H-bridge, $u_{DC(p)}$ are the DC-link voltages.

If the H-bridges are in active states ($T_{1U(p)} - T_{2U(p)} = \pm 1$), the active voltage vector components can be rewritten as:

$$\begin{aligned} u_{\alpha(a)} &= \pm\sqrt{\frac{2}{3}} \cdot u_{DC(a)}, \quad u_{\beta(a)} = 0, \\ u_{\alpha(b)} &= \pm\sqrt{\frac{2}{3}} \cdot u_{DC(b)} \cdot cos\left(\frac{2\pi}{3}\right), \\ u_{\beta(b)} &= \pm\sqrt{\frac{2}{3}} \cdot u_{DC(b)} \cdot sin\left(\frac{2\pi}{3}\right), \\ u_{\alpha(c)} &= \pm\sqrt{\frac{2}{3}} \cdot u_{DC(c)} \cdot cos\left(\frac{4\pi}{3}\right), \\ u_{\beta(c)} &= \pm\sqrt{\frac{2}{3}} \cdot u_{DC(c)} \cdot sin\left(\frac{4\pi}{3}\right), \end{aligned} \tag{8}$$

The lengths of obtained active vectors depend on the DC-link voltages (Fig. 3).

The output voltages can be simultaneously generated in three H-bridges giving the active voltage vectors shown in

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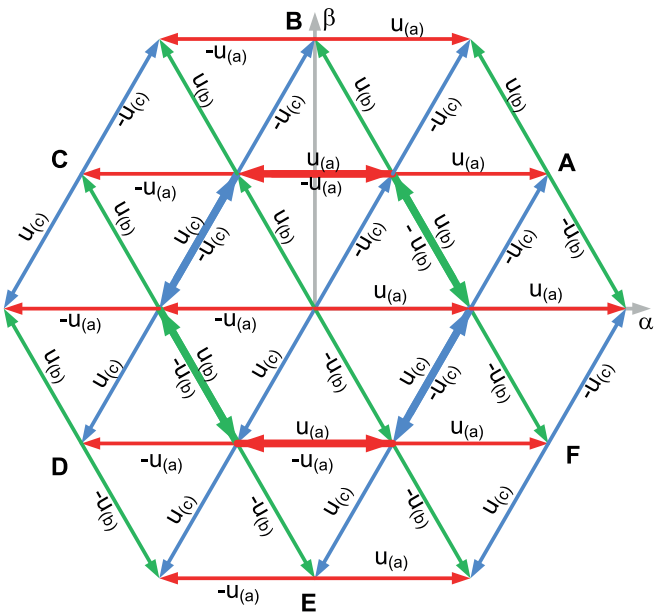


Fig. 4. Active voltage vectors generated in three H-bridges in the case of balanced DC-link voltages

Fig. 4. Any three H-bridges (one in any CHB inverter phase) can be treated as a three-level CHB inverter. The seven-level CHB inverter with 3 H-bridges connected in series can be considered as a set of 3 three-level CHB inverters. The output voltage of seven-level inverter can be calculated as:

$$u_{o\alpha(7L)} = \sum_{j=1}^{3} u_{o\alpha(3L)}{}^{j}, \quad u_{o\beta(7L)} = \sum_{j=1}^{3} u_{o\beta(3L)}{}^{j}, \tag{9}$$

where: $u_{o\alpha(7L)}$, $u_{o\beta(7L)}$ are the components of the output voltage vector of the seven-level CHB inverter, $u_{o\alpha(7L)}{}^{j}$, $u_{o\beta(7L)}{}^{j}$ are the components of the output voltage vectors generated in three level CHB converters.

## 5. The selection of H-bridges for three-level CHB inverters

If the DC-link voltages are equal, the H-bridges, used to construct the three-level CHB inverters, can be selected arbitrarily. Otherwise, the impact of H-bridge exploitation on its DC-link voltage has to be analyzed. In the proposed solution, the H-bridges with lowest DC-link voltages (considered for each phase separately) will be used before all others to compose the first of the three-level CHB inverters if the following condition is be fulfilled:

$$i_{(p)} \cdot u_{ref(p)} > 0, \tag{10}$$

where: $i_{(p)}$ is the "$p$"- phase current $(p = a, b \text{ or } c)$, $u_{ref(p)}$ is the reference phase voltage of a seven-level CHB inverter, determined using reverse Clarke's transformation.

If the condition is not satisfied, the three-level inverter will be constructed using the H-bridges with the highest DC-link voltages. This three-level CHB inverter will be used as the first to compose the seven-level CHB inverter output voltage. As a result, the voltage unbalance will be reduced in the first place in the H-bridges with highest or lowest DC-link voltages.

The next three-level inverters will be constructed in the same manner, utilizing the available (previously unused) H-bridges and taking into consideration their DC-link voltages and condition.

## 6. The space vector modulation for the three-level CHB inverter

The output voltage vector of three-level CHB inverter can be generated using one of the three proposed SVM strategies. For all modulation strategies, the choice of the sector (and the choice of active voltage vectors) depends on the angular position of the reference voltage of the seven-level CHB inverter. The length of the reference voltage is not relevant. Because the three-level inverters are considered to generate the seven-level CHB reference voltage vector, the end of the reference vector may be located outside the area shown in Fig. 4.

All the modulation strategies are calculated at the same time and the best one is selected to generate the output voltage vector. The selection method is described in Section 8. The proposed modulation strategies are described below.

**6.1. Modulation strategy I.** If the position of the reference voltage vector is in the range of $0$ to $^{2\pi}/_{6}$ rad, the reference voltage vector is assigned to sector $A$ (Fig. 4). In this case the active states are in the H-bridges in phase "$a$" (positive output voltage) and phase "$c$" (negative output voltage) (Fig. 5b). The H-bridge in phase "$b$" is bypassed. The duty cycles for all exploited H-bridges can be calculated as (Fig. 5a):

$$\begin{aligned} \gamma_{(a)} &= \frac{u_{ref\alpha} \cdot u_{\beta(c)} - u_{ref\beta} \cdot u_{\alpha(c)}}{u_{\beta(c)} \cdot u_{\alpha(a)} - u_{\alpha(c)} \cdot u_{\beta(a)}}, \\ \gamma_{(b)} &= 0, \\ \gamma_{(c)} &= \frac{u_{ref\beta} \cdot u_{\alpha(a)} - u_{ref\alpha} \cdot u_{\beta(a)}}{u_{\beta(c)} \cdot u_{\alpha(a)} - u_{\alpha(c)} \cdot u_{\beta(a)}}, \end{aligned} \tag{11}$$

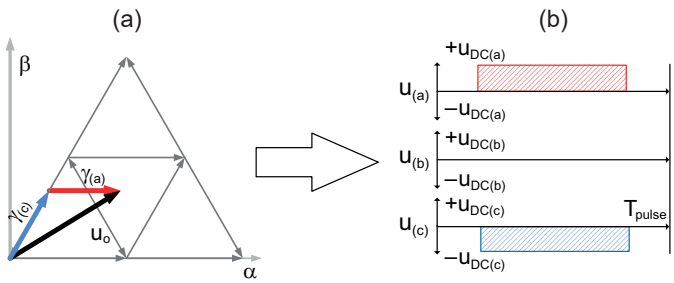


Fig. 5. a) the duty cycles in modulation strategy I; b) corresponding phase voltage waveforms



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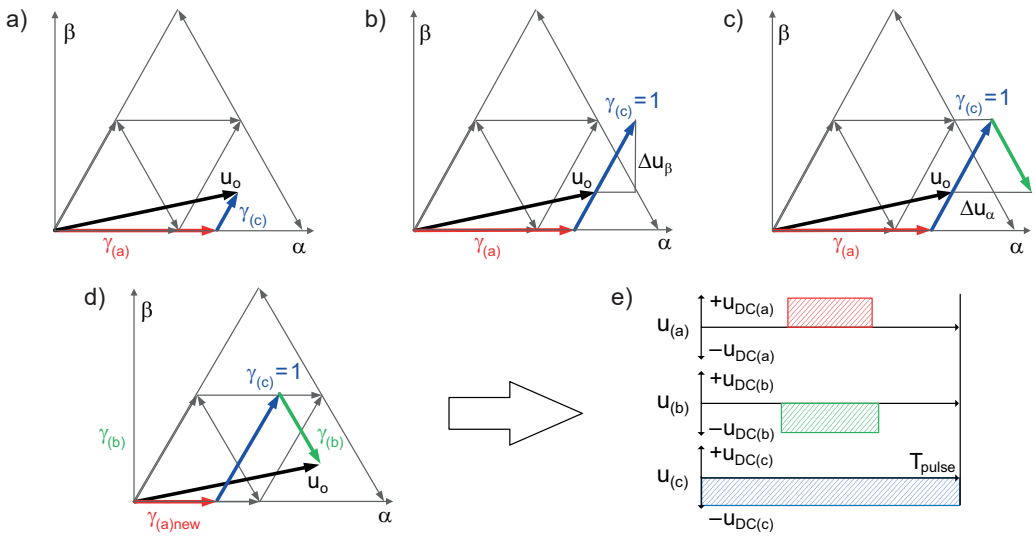


Fig. 6. The duty cycle selection steps in modulation strategy II (a–d) and resulting phase voltage waveforms (e)

where: $u_{refa}$, $u_{ref\beta}$ are the reference voltage vector components of the seven-level CHB inverter.

The components of active voltage vectors $u_{\alpha(a)}$, $u_{\beta(a)}$, $u_{\alpha(b)}$, $u_{\beta(b)}$ are determined taking into account the actual DC-link voltages. The output voltage will be generated correctly also in the case of unequal DC-link voltages.

Equations allow to determine the duty cycles for three-level CHB inverter (three H-bridges), while the reference voltage is defined for the multilevel CHB inverter. As an result, the calculated duty cycles can be greater than one. They will be limited in the next step of the algorithm, described in Section 7.

**6.2. Modulation strategy II.** Modulation strategy II is determined simultaneously with modulation strategy I. If the reference voltage vector is assigned to sector A (Fig. 4), the following active vectors are utilized:

- main active vector: $u_{(a)}$,
- complementary active vector: $-u_{(c)}$,
- auxiliary active vector: $-u_{(b)}$.

The duty cycles for the H-bridges in phases "*a*" and "*c*" (main and complementary active vector) are determined in the same manner as in modulation strategy I , assuming zero state for the H-bridge in phase "*b*" (auxiliary active vector). If the duty cycle for the H-bridge in phase "*c*" (complementary active vector) is less than 1 (Fig. 6a), it is assumed that this duty cycle is equal to "1" (Fig. 6b). Thus, this duty cycle is increased by the value:

$$\Delta\gamma_{(c)} = 1 - \gamma_{(c)}. \tag{12}$$

This operation affects the length and position of the output voltage vector. The change in the $\beta$-component of the output voltage vector (Fig. 6b) can be calculated as:

$$\Delta u_\beta = (\Delta\gamma_{(c)} \cdot |u_{(c)}|) \cdot sin\left(\frac{\pi}{3}\right), \tag{13}$$

and can be compensated by the auxiliary vector of the H-bridge in phase "*b*" (Fig. 6c). The duty cycle for this H-bridge can be calculated as:

$$\gamma_{(b)} = \frac{\Delta u_\beta}{|u_{(b)}| \cdot \sin\left(\frac{\pi}{3}\right)}. \tag{14}$$

Substitution of (13) in (14) yields:

$$\gamma_{(b)} = \Delta\gamma_{(c)} \cdot \frac{|u_{(c)}|}{|u_{(b)}|}. \tag{15}$$

The change in the $\beta$-component of the output voltage vector is now compensated, while the $\alpha$-component is increased by the value (Fig. 6c):

$$\Delta u_\alpha = \left(\Delta\gamma_{(c)} \cdot |u_{(c)}| + \gamma_{(b)} \cdot |u_{(b)}|\right) \cdot cos\left(\frac{\pi}{3}\right). \tag{16}$$

It can be compensated by modifying the duty cycle for the H-bridge in phase "*a*" (main active vector). The new duty cycle can be calculated as:

$$\gamma_{(a)new} = \gamma_{(a)} - \frac{\Delta u_\alpha}{|u_{(a)}|}, \tag{17}$$

where $\gamma_{(a)new}$ is the updated duty cycle (Fig. 6d).

The presented modification of the duty cycles ensures equality of the output voltage vector and the reference voltage vector. The duty cycle for the H-bridge in phase "*c*" is equal to 1 and the transistors are not switched. The resulting phase voltage waveforms are presented in Fig. 6e.

If the new duty cycle $\gamma_{(a)new}$ is negative, it is assumed that this duty cycle is equal to "0". The output voltage vector can be generated using two active voltage vectors (H-bridges in phases

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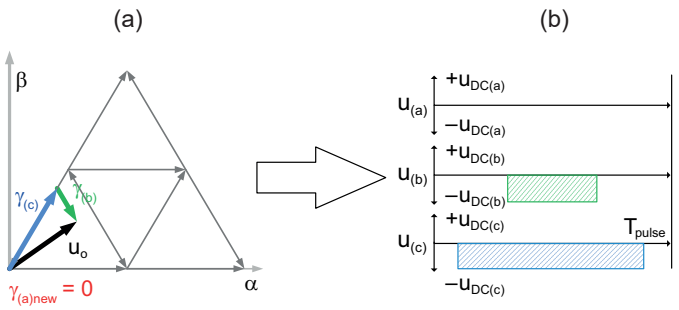


Fig. 7. The duty cycles in modulation strategy II (a) and corresponding phase voltage waveforms (b) in the case of zero duty cycle for phase "*a*" H-bridge

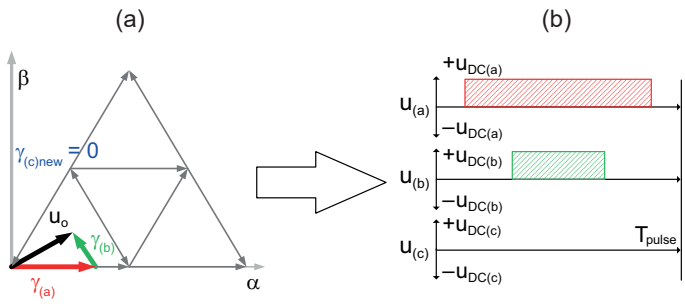


Fig. 9. The duty cycles in modulation strategy III (a) and corresponding phase voltage waveforms (b) in the case of zero duty cycle for H-bridge in phase "*c*"

"*b*" and "*c*"), while the H-bridge in phase "*a*" is bypassed (the transistors are not switched) (Fig. 7). The duty cycles for all three H-bridges can be determined as:

$$\begin{aligned} \gamma_{(a)new} &= 0, \\ \gamma_{(b)} &= \frac{u_{ref\alpha} \cdot u_{\beta(c)} - u_{ref\beta} \cdot u_{\alpha(c)}}{u_{\beta(c)} \cdot u_{\alpha(b)} - u_{\alpha(c)} \cdot u_{\beta(b)}}, \\ \gamma_{(c)} &= \frac{u_{ref\beta} \cdot u_{\alpha(b)} - u_{ref\alpha} \cdot u_{\beta(b)}}{u_{\beta(c)} \cdot u_{\alpha(b)} - u_{\alpha(c)} \cdot u_{\beta(b)}}. \end{aligned} \tag{18}$$

If the duty cycles will be greater than 1, they will be limited in the next step of the algorithm (Section 7).

**6.3. Modulation strategy III.** Modulation strategy III is determined simultaneously with modulation strategies I and II. The only difference between modulation strategies II and III is in the choice of active vectors. Modulation strategy III utilizes replaced main and complementary active vectors and the opposite auxiliary vector, all defined for modulation strategy II (Fig. 8a). If the output voltage vector is assigned to sector *A* (Fig. 4), the following active vectors will be exploited:

- main active vector: $-u_{(c)}$,
- complementary active vector: $u_{(a)}$,
- auxiliary active vector: $u_{(b)}$.

The duty cycles are determined in the same manner as in modulation strategy II, also taking into account actual DC-link voltages. The duty cycles for the H-bridge in phase "*a*" and the H-bridge in phase "*b*" are increased, while the duty cycle for the H-bridge in phase "*c*" is decreased (Fig. 8 a–d). As an result, the duty cycle for the H-bridge in phase "*a*" is equal to one (the transistors are not switched). The phase voltage waveforms of three-level CHB converter with modulation III are shown in Fig. 8e.

If the new duty cycle $\gamma_{(c)new}$ is negative, similarly as in modulation strategy II, it is assumed that this duty cycle is equal to "0". The output voltage vector is generated using two active voltage vectors (H-bridges in phases "*a*" and "*b*"), while the H-bridge in phase "*c*" is in zero state (the transistors are not switched) (Fig. 9). The duty cycles for the remaining H-bridges are recalculated in the same manner as in modulation strategy II (18).

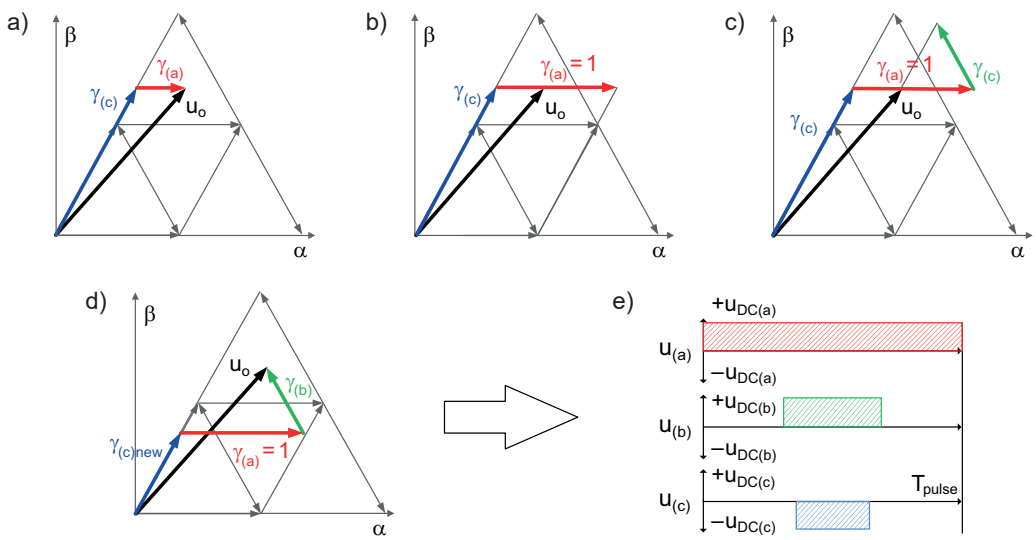


Fig. 8. The duty cycle selection steps in modulation strategy III (a–d) and resulting phase voltage waveforms (e)

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## 7. Limitation of the duty cycles

Since all the proposed modulation strategies are determined for the three-level CHB inverter, while the reference voltage vector is designated for the multilevel CHB inverter, some of (or all) the calculated duty cycles can be greater than "1". It is therefore necessary to limit them:

$$\text{if } \gamma_{(a,b,c)} > 1 \Rightarrow \gamma_{(a,b,c)} = 1. \tag{19}$$

For all proposed modulation strategies, the components of the available output voltage vector are calculated using limited duty factors:

$$\begin{aligned} u_{o\alpha(3L)} &= \gamma_{(a)} \cdot u_{\alpha(a)} + \gamma_{(b)} \cdot u_{\alpha(b)} + \gamma_{(c)} \cdot u_{\alpha(c)}, \\ u_{o\beta(3L)} &= \gamma_{(a)} \cdot u_{\beta(a)} + \gamma_{(b)} \cdot u_{\beta(b)} + \gamma_{(c)} \cdot u_{\beta(c)}, \end{aligned} \tag{20}$$

where: $u_{o\alpha(3L)}$, $u_{o\beta(3L)}$ are the components of the output voltage vector of the three level CHB inverter.

## 8. Choice of the modulation strategy

The output voltage vector can be generated using one of three modulation strategies. If all considered modulation strategies operate on limited duty cycles (20), the choice of the modulation strategy should provide the output voltage vector of three-level CHB inverter as close as possible to the reference voltage vector of seven-level CHB inverter. In this case, the output voltage vector will be generated using this modulation strategy, which ensures the minimum value of the function:

$$\begin{aligned} f\left(u_{o\alpha(3L)}, u_{o\beta(3L)}\right) &= \left(u_{ref\alpha} - u_{o\alpha(3L)}\right)^2 + \\ &+ \left(u_{ref\beta} - u_{o\beta(3L)}\right)^2, \end{aligned} \tag{21}$$

where: $u_{o\alpha(3L)}$, $u_{o\beta(3L)}$ are the components of the output voltage vector of a three-level inverter, calculated using (20) for all proposed modulation strategies, $u_{ref\alpha}$, $u_{ref\beta}$ are the reference voltage vector components of seven-level CHB inverter.

If the voltage vector, obtained in three-level CHB inverter, is not equal to the reference voltage vector of the seven-level CHB inverter, the next three H-bridges are activated (next three-level CHB inverter). The new reference voltage for the next three-level CHB inverter can be calculated as:

$$u'_{ref\alpha} = u_{ref\alpha} - u_{o\alpha(3L)}, \quad u'_{ref\beta} = u_{ref\beta} - u_{o\beta(3L)}. \tag{22}$$

where $u'_{ref\alpha}$, $u'_{ref\beta}$ are the new reference voltage vector components of seven-level CHB inverter used to calculate the duty cycles for the next three-level CHB inverter.

The algorithm described above is repeated until the output and the reference voltage vectors are equal:

$$u'_{ref\alpha} = u_{o\alpha(3L)}, \quad u'_{ref\beta} = u_{o\beta(3L)}. \tag{23}$$

and until the duty cycles, obtained in at least one of the considered modulation strategies I–III, are limited using (19). In this case, the appropriate modulation strategy is selected in a different way. The output voltage is generated using this modulation method, which operates on unlimited duty cycles and ensures minimization of the predicted DC-link voltage unbalance:

$$\begin{aligned} &f\left(u_{DC(a)}, u_{DC(b)}, u_{DC(c)}\right) = \\ &= \left(u_{DC(a)}(k+1) - u_{DC(AV)}\right)^2 + \\ &+ \left(u_{DC(b)}(k+1) - u_{DC(AV)}\right)^2 + \\ &+ \left(u_{DC(c)}(k+1) - u_{DC(AV)}\right)^2, \end{aligned} \tag{24}$$

where

$$u_{DC(AV)} = \frac{u_{DC(a)}(k+1) + u_{DC(b)}(k+1) + u_{DC(c)}(k+1)}{3}, \tag{25}$$

and:

$$u_{DC(p)}(k+1) = u_{DC(p)}(k) + \frac{1}{C} \cdot \gamma_{(p)} \cdot T_{pulse} \cdot i_{(p)}, \tag{26}$$

where: $i_{(p)}$ is phase current, $p$ – the phase of CHB inverter ($p = a$, $b$ or $c$), $C$ is DC-link capacitance, $(k)$ and $(k+1)$ denote actual and predicted DC-link voltages.

## 9. Results of simulation and experimental investigations

The proposed SVM strategy and DC-link balancing method has been tested by simulation and implemented in both inverters of 600 KW seven-level CHB converter (Fig. 10): the CHB inverter and the CHB rectifier used for coupling two medium voltage grids (3.3 kV). The DC-links of both inverters were coupled using 70 kW/1 kV DABs with MF transformers, as in Table 1. The CHB inverter and rectifier contain nine DC-links each with 2.2 mF capacity. Switching frequencies: DABs – 7 kHz, inverter/rectifier – 3.33 kHz. The control systems of the CHB inverter, rectifier and all the DABs were not coupled and worked independently.

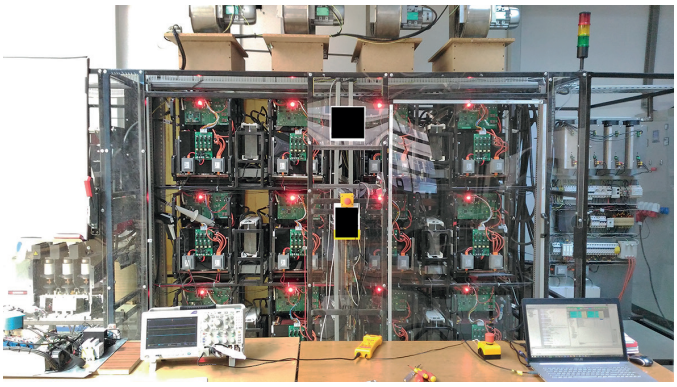

Fig. 10. The 7-level MV CHB converter with dual active bridges



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The proposed solution makes it possible to control the DC-link voltages in steady and transient states. The results of the simulation tests during rapid change in DC-link voltages are shown in Fig. 11.

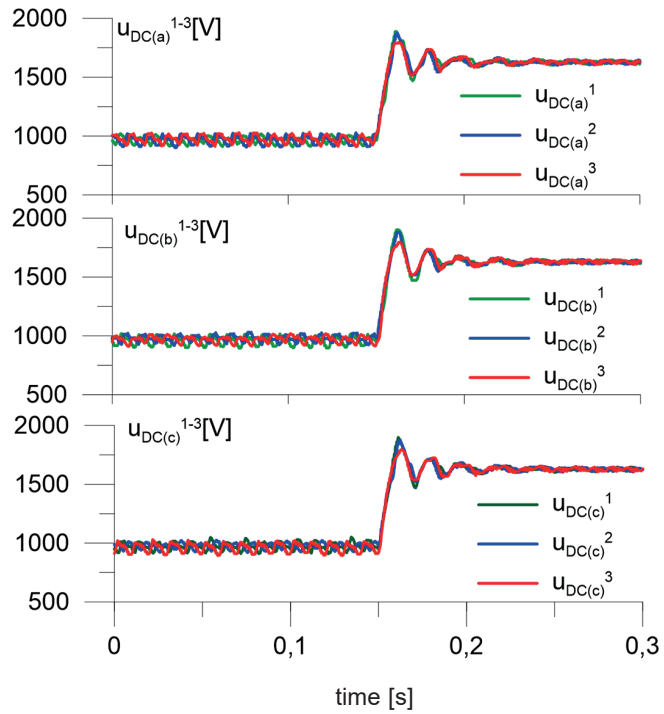


Fig. 11. The change in DC-link voltages in the seven-level CHB inverter. $u_{DC(p)}^{i}$ – DC-link voltages in phase "$p$" ($p = a, b, c$), "$i$" – H-bridge number ($i = 1, 2, 3$). Simulation results

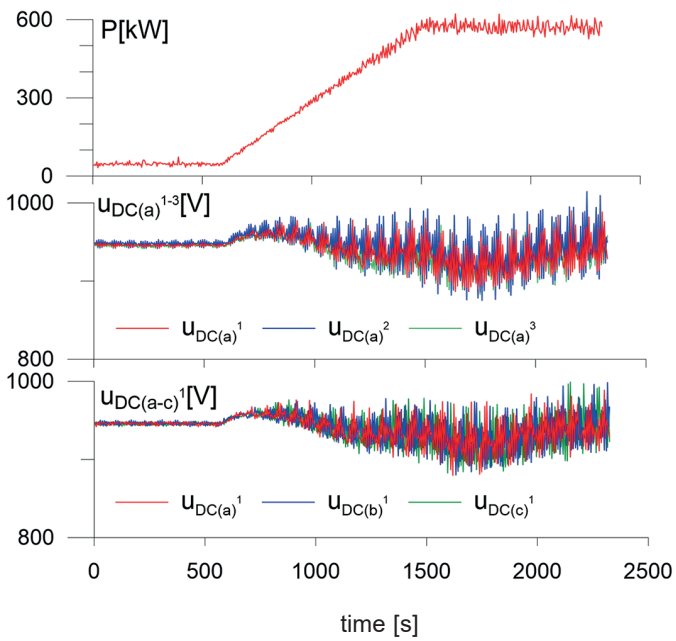


Fig. 12. The change in active power of the seven-level CHB inverter. P – active power, $u_{DC(p)i}$ – DC-link voltages in phase "$p$" ($p = a, b, c$), "$i$" – H-Bridge number ($i = 1, 2, 3$) (Fig. 1). Experimental results

The results of experimental investigations are shown in Figs. 12–17. The DC-link voltages of all H-bridges in one of inverter phases and the DC-link voltages of the first H-bridges in each inverter phase during the change in transferred active power are shown in Fig. 12. Figure 13 presents the input and output DC-link voltages of one of the DABs used for coupling the CHB rectifier and CHB inverter during the change in active power.

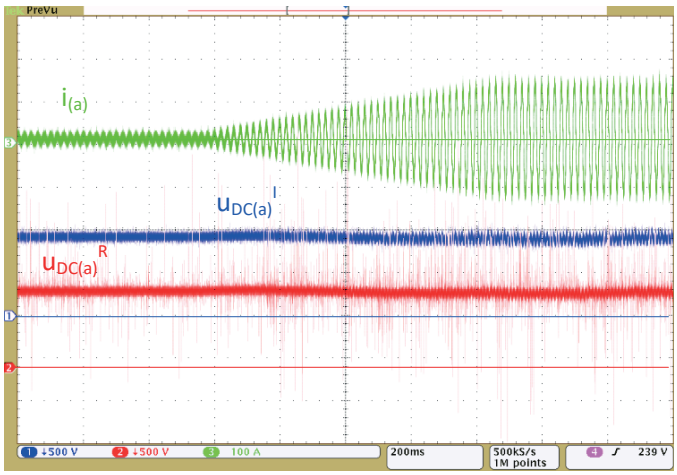


Fig. 13. The phase "a" current ($i_{(a)}$) and the capacitor voltages of dual active bridge: $u_{DC(a)}^{R}$ – the capacitor voltage on the CHB rectifier side, $u_{DC(a)}^{I}$ – the capacitor voltage on the CHB inverter side (Fig. 2) during change in active power 10 kW → 550 kW. Scale: 100 A/div, 500 V/div, 200 ms/div

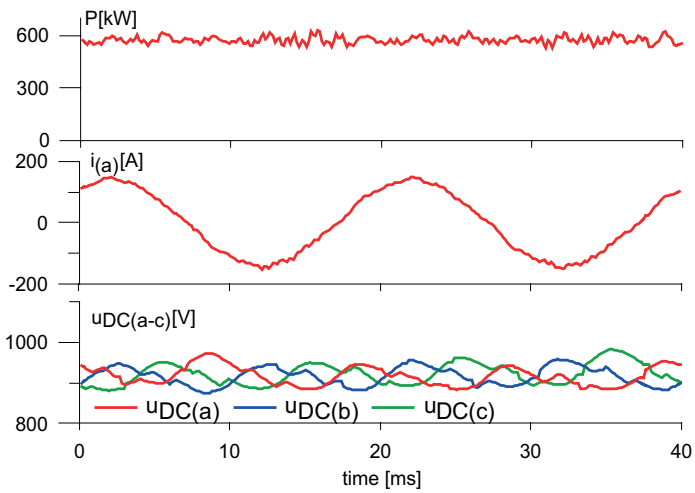


Fig. 14. The active power (P), phase current ($i_{(a)}$) and the DC-link voltages ($u_{DC(a)}^{1}$, $u_{DC(b)}^{1}$, $u_{DC(c)}^{1}$) (Fig. 1) of the H-bridges in phases "a", "b", "c" of the seven-level CHB-inverter. Experimental results

The DC-link voltages in all inverter phases (one H-bridge in each phase) and the waveforms of two DC-link voltages in the same inverter phase obtained in experiments are shown in Figs. 14 and 15, respectively. All the DC-link voltages are almost the same and the output voltage is correctly generated (Fig. 17).

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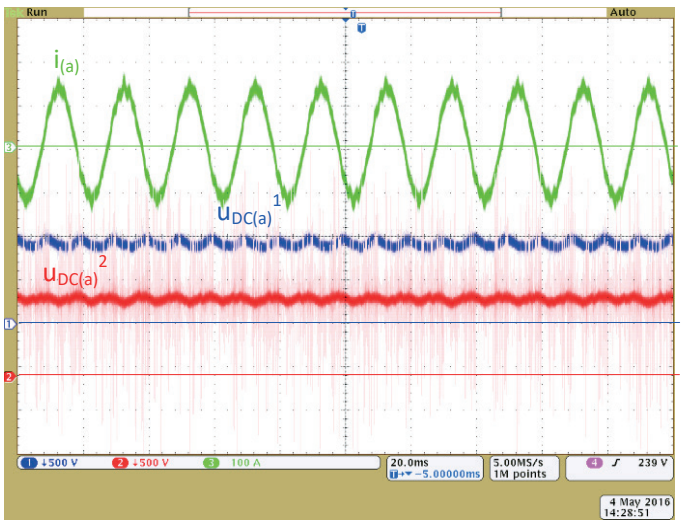


Fig. 15. The phase "a" current $(i_{(a)})$ and the DC-link voltages $(u_{DC(a)}{}^{1-2})$ of two H-bridges in phase *a* (Fig. 1). Active power of CHB converter: 550 kW. Scales: 100 A/div, 500 V/div, 20 ms/div

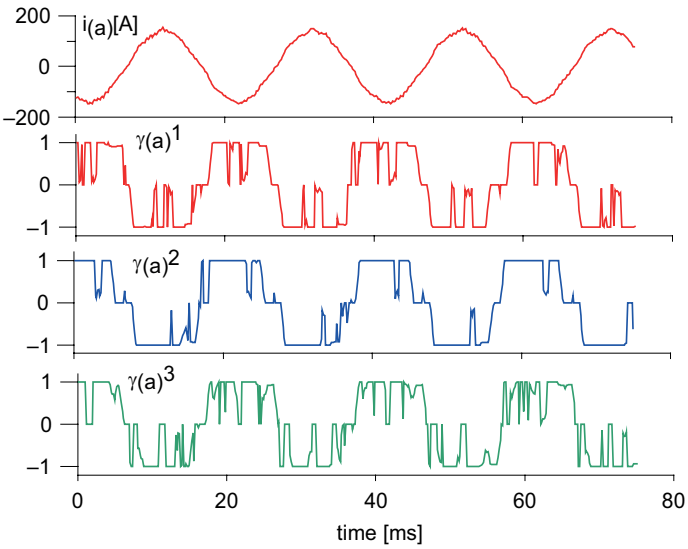


Fig. 16. The duty cycles three H-bridges in phase "a" of the seven-level CHB converter. Active power P = 570 kW. Experimental results

The proposed solution makes it possible to reduce the switching amount of CHB converter transistors. Most of the time, the duty cycles of the H-bridges are equal to ±1 (minus for negative output voltage) or to 0 (Fig. 16). The output voltage is modulated in one of the H-bridges in any of the inverter phases. The other H-bridges are positively or negatively connected or bypassed and the transistors are not switched.

## 10. Conclusions

In this paper, a new SVM strategy for multilevel CHB inverter is proposed. In the presented solution, the selection of DC-link capacitors (the selection of H-bridges) used to build the inverter

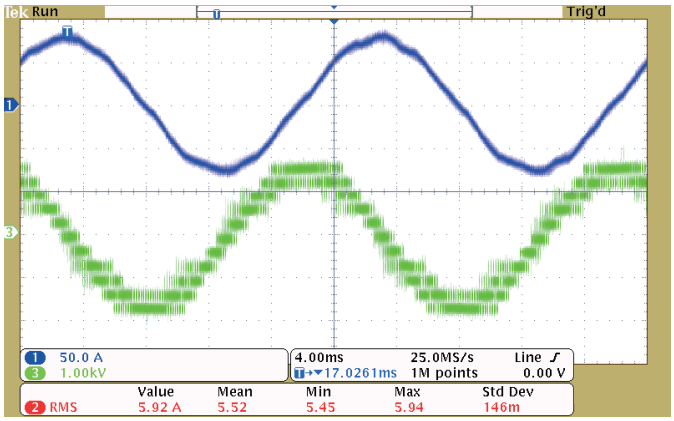


Fig. 17. The output voltage $U_{bc}$ and phase current $i_a$ of the seven-level CHB inverter with proposed modulation strategy. Experimental results. Scales: 50 A/div, 1 kV/div, 4 ms/div

output voltage is based on active power direction and DC-link voltage distribution. This selection is realized for each phase separately. If the active power is transferred to the inverter, the H-bridge with lowest DC-link voltage is used as the first to build the inverter output voltage, and as the last if the energy is taken. Since first chosen H-bridges are in active states for the entire pulse period, the highest dose of energy will be delivered to their capacitors. The decision on the order of H-bridge utilization is taken at the beginning of each loop of the proposed SVM algorithm and the reconfiguration of H-bridge utilization may occur depending on the DC-link voltage unbalance. The H-bridge which has been actively connected during one (or several) pulse period(s) can be modulated or bypassed in the next periods.

The main purpose of the proposed solution is to obtain similar (but not necessarily identical) DC-link voltages with limited quantity of transistor commutations. This is accomplished by forcing the H-Bridges to be actively connected or bypassed for (at least) one pulse period ($\gamma = \pm 1$ *or* $\gamma = 0$ in Fig. 16). Because these H-bridges are in one state only (active or zero state), their transistors are not switched. This limits the possibility to maintain identical voltage on all DC-link capacitors (Fig. 11–15) and reduces the switching losses as compared to the methods wherein all the H-bridges are modulated. The acceptable DC-link voltages (including their variations) should be below blocking voltages of transistors or nominal voltages of passive circuit components.

The actual values of DC-link voltages are taken into account during construction of the inverter output voltage vector in SVM algorithm. The output voltage is generated properly independently of the DC-link voltage unbalance.

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