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A Comprehensive Survey on Antennas On-Chip Based on Metamaterial, Metasurface, and Substrate Integrated Waveguide Principles for Millimeter-Waves and Terahertz Integrated Circuits and Systems

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ABSTRACT Antennas on-chip are a particular type of radiating elements valued for their small footprint. They are most commonly integrated in circuit boards to electromagnetically interface free space, which is necessary for wireless communications. Antennas on-chip radiate and receive electromagnetic (EM) energy as any conventional antennas, but what distinguishes them is their miniaturized size. This means they can be integrated inside electronic devices. Although on-chip antennas have a limited range, they are suitable for cell phones, tablet computers, headsets, global positioning system (GPS) devices, and WiFi and WLAN routers. Typically, on-chip antennas are handicapped by narrow bandwidth (less than 10%) and low radiation efficiency. This survey provides an overview of recent techniques and technologies investigated in the literature, to implement high performance on-chip antennas for millimeter-waves (mmWave) and terahertz (THz) integrated-circuit (IC) applications. The technologies discussed here include metamaterial (MTM), metasurface (MTS), and substrate integrated waveguides (SIW). The antenna designs described here are implemented on various substrate layers such as Silicon, Graphene, Polyimide, and GaAs to facilitate integration on ICs. Some of the antennas described here employ innovative excitation mechanisms, for example comprising open-circuited microstrip-line that is electromagnetically coupled to radiating elements through narrow dielectric slots. This excitation mechanism is shown to suppress surface wave propagation and reduce substrate loss. Other techniques described like SIW are shown to significantly attenuate surface waves and minimise loss. Radiation elements based on the MTM and MTS inspired technologies are shown to extend the effective aperture of the antenna without compromising the antenna's form factor. Moreover, the on-chip antennas designed using the above technologies exhibit significantly improved impedance match, bandwidth, gain and radiation efficiency compared to previously used technologies. These features make such antennas a prime candidate for mmWave and THz on-chip integration. This review provides a thorough reference source for specialist antenna designers.

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INDEX TERMS Antenna on-chip (AoC), metamaterial (MTM), metasurface (MTS), substrate integrated waveguide (SIW), millimeter-waves (mmWave) and terahertz (THz) spectrum, intgrated RF transciver circuits, multilayer structures, electromagnetic (EM) coupled feed mechanism.

I. INTRODUCTION

Millimeter-wave (mmWave) and terahertz (THz) bands are the new frontiers of wireless communications technology that is expected to enable seamless interconnection between ultra high speed wired networks (fiber optic links) and personal wireless devices (laptops), achieving full transparency and rate convergence between wireless and wired links. This should facilitate the use of bandwidth intensive applications, mainly in indoor and local access scenarios. The push now is to develop systems-on-chip (SoC) since traditional off-chip antenna technology faces several severe constraints to meet the requirements of size, low-power, and low-loss. On-chip antennas are a promising solution, which are more favorable than off-chip antennas in this respect. Antennas are one of the key components to interface the communications system to free space. The limiting factor of antennas is their size, which is wavelength dependent. Hence, the design of mmWave and THz for on-chip integration is an extremely challenging task. Moreover, their design requires high-precision fabrication tools, accurate alignment as well as short bonding wire or flipped chip connections [1].

Active components of mmWave and THz circuits in current technology are usually highly integrated except for the antennas [2], [3]. The antennas are assembled using expensive ground-signal-ground (GSG) probes, bulky waveguides and horn antennas, which are not suitable in mass production. The integration of such antennas is therefore a highly complex and challenging endeavour for semiconductor system-on-chip (SoC) manufacturers [1], [4], [5]. To realise high efficiency and gain, the off-chip antenna in the package (AiP) design is usually fabricated on either printed circuit board (PCB) [5], low-temperature cofired ceramic (LTCC) [4], or other low-loss materials [1]. However, because of the incompatibility of the antennas and the active circuits, the interconnect loss of the packaging cannot be ignored, especially at mmWave and THz frequencies. Interconnect loss is experienced in both flip-chip [1] and the wire-bonding technologies [4].

With advancement in mobile communications and integration technology, the interest in radio frequency integrated circuits (RFICs) has increased, including the demonstration of antennas for SoC applications [6], [7]. An on-chip antenna has been used as a transformer in radio frequency identifiers (RFIDs) [8], [9]. A transceiver with on-chip antennas forms a true single-chip radio that can be used to wirelessly connect sensor network nodes [10]. For this application, the use of on-chip antennas eliminates the need for bondwire connections and sophisticated packaging, and hence makes the fabrication of cost-effective miniature systems feasible.

The first on-chip antenna integrated with a 95-GHz IMPATT diode oscillator on a high resistivity silicon substrate was reported in 1986 [11]. Two years later, a similar antenna on a GaAs substrate was reported [12]. During their first phase of evolution, integrated antennas were mainly designed for wireless interconnect applications and the measured transmission gain was limited to −50 to −70 dB, which was not adequate for practical applications. Since then, efforts have been made to optimize the substrate properties and antenna configurations to develop on-chip integrated antennas. Some of the important classes of on-chip silicon antennas investigated to date include printed circuit monopoles [13], dipoles [14]–[16], microstrip patch [17], inverted F, and quasi-Yagi [18] antennas. Although a few of these antennas [18] could boost the transmission gain up to −20 dB and the antenna gain up to −6 dBi, they were still unusable. It should be noted that for wireless interconnect, the performance is measured in transmission gain in dB [14] instead of dBi, and antenna directive gain [15], [16] is measured for wireless transmission applications.

Antennas have been implemented using high resistance silicon [19], [20] and using proton implantation techniques [13] to increase the substrate resistivity to improve the antenna performance. However, high resistivity silicon substrates are not compatible with cost effective silicon process technologies with high level of integration and proton implantation methods, which are very costly and challenging to implement. To reduce the losses, recent research on silicon integrated antennas has mainly focused on methods to isolate the substrate from the radiating element. Embedded structures and micromachined/multilayered antenna fabrication techniques [21]–[23] have also been investigated to improve the antenna performance. This was achieved by either coating low dielectric loss polymer/ceramic films on the conducting silicon or by employing multilayer process/micromachining techniques to isolate the lossy conducting silicon from the radiating element. This enables suspension of the radiating element above chip surface [24]–[27] and thereby enhance the antenna's bandwidth and radiation performance. Using these methods, antennas with a gain in the range of −5 dBi to 2 dBi have been reported. High precession micromachining is however a challenging process, especially for fabricating millimeter-wave and terahertz antennas. Printed planar integrated antennas on silicon have limitations of low power, low gain/efficiency and a large size. Poor antenna performance mainly results from conductor and substrate losses and surface wave effects [28].

Many technical solutions have been devised to design compact antennas, including high-permittivity dielectric substrates, shorting pins, shorting walls, applying the fractal geometry, etc. The drawbacks of these methods are complex design, narrow bandwidth, low gain and efficiency. Low gain is the main disadvantage of small planar antennas, which must be overcome to satisfy the overall link budget of transceivers.

More recently, metamaterials (MTM), metasurfaces (MTS), and substrate integrated waveguide (SIW) techniques have been used [29], [30] to realize high performance antennas for system-on-chip (SoC). This is because these technologies offer advantages of smaller size, wider bandwidth, and better radiation properties. Moreover, they suppress excitation of surface waves that can degrade the radiation characteristics of the antenna. They also ease the integration of the antenna with microwave integrated circuits (MIC). The proposed techniques facilitate the realization and integration of SoC antennas on the various high permittivity dielectric substrates like Silicon, graphene, polyimide, GaAs that can reduce the losses in the conducting layers and therefore help to improve the antenna performance [31]–[44].

Metamaterials and metasurfaces (a two-dimensional counterpart of metamaterials) are artificially engineered to manipulate EM-waves to exhibit negative refractive-index not found in nature [45]–[53]. These technologies have been used to reduce the physical size and improve the characteristics of microwave components such as couplers, filters, mixers, and antennas [45]. Their unique characteristics have allowed new applications, concepts, and devices to be developed [54]–[60].

The important characteristic of metamaterial transmission lines (TLs) compared with conventional TLs is their ability to control the phase constant and the characteristic impedance. Hence, MTM/MTS are now extensively applied in antenna design [29], [30], [61]–[67]. Moreover, the unusual characteristics of MTM/MTS enables us the create novel antenna structures, which cannot be obtained with traditional technologies. Research shows that antennas based on MTM/MTS have enhanced radiated power and extended operational bandwidth [68]–[70]. The main features that make MTM and MTS attractive for antenna designs compared with traditional technologies are (i) realization of smaller antennas, (ii) larger bandwidth, (iii) improved radiation characteristics, and (iv) realization of multiband functionality.

On-chip antennas are often constructed on multi-layered substrates. The design and fabrication of these antennas are highly complex. These devices are also lossy because of loss in the substrates and surface wave interactions between the radiating elements. To reduce these interactions and minimize substrate and surface wave loss, the use of substrate integrated waveguide technology in the design of on-chip antennas has been shown to be effective. SIW involves framing the antenna with via-pins or via-holes that penetrate the layers. This reduces loss and isolates individual radiators.

MTM, MTS and SIW technologies have been extensively used in the design of antennas at microwave frequencies. However, they are not so prevalent at mmWave and THz frequencies [29], [30], [71]–[76]. Nowadays, mmWave and THz technologies are recognized as one of the most promising and challenging areas of research, because they have the capacity to offer super high data rate communications and therefore high-resolution imaging [77], [78]. However, THz sources are complex to generate [79]. The various solutions proposed in the design of antennas at these frequency bands reveal the complexity and high fabrication costs [80]–[85].

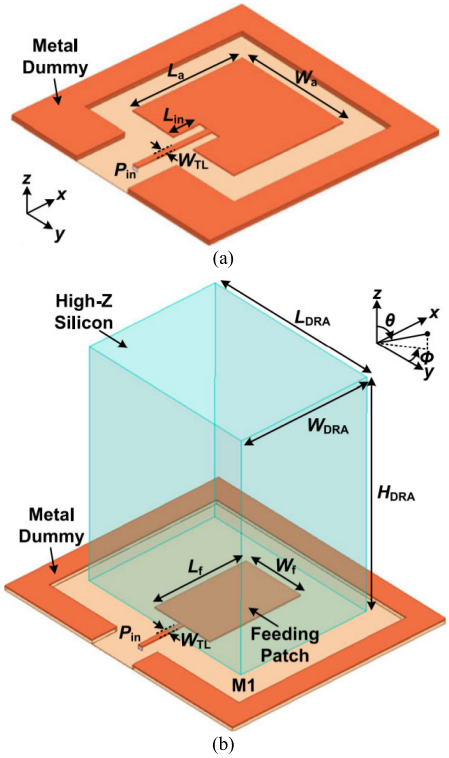

FIGURE 1. (a) Antenna on-chip implemented in the 0.18-μm CMOS technology, and (b) terahertz dielectric resonator on-chip antenna [88].

This survey presents the latest work related on-chip antennas using MTM, MTS and SIW technologies. It will look at the pros and cons of the various salient antenna parameters versus cost/complexity tradeoff for application in RF transciver circuits operating at mmWave and THz bands. The survey will examine on-chip antennas implemented on different substrates such as Silicon, graphene, polyimide, and GaAs to determine ease of on-chip integration and reduction in interconnect loss as well as challenges. This review should serve as a reference for researchers to advance the state-of-the-art.

II. HIGH PERFORMANCE ON-CHIP ANTENNAS FOR mmWAVE AND THz INTEGRATED RF CIRCUITS

On-chip antennas are essential for implementing fully integrated systems-on-chip. An on-chip antenna can significantly simplify the matching network required to interface the antenna to the RF circuitry. This simplification of the matching network can greatly improve the system's performance by reducing the front-end loss and noise figure. For the antenna to radiate optimally or extend the battery life of the systems, its efficiency must be as high as possible. It is also important to note that the on-chip antenna's dimension is the dominant factor in determining the chip area; hence, its size must be as small as possible to lower fabrication costs. Antenna miniaturization can be performed by using compact configurations and employing high permittivity materials.

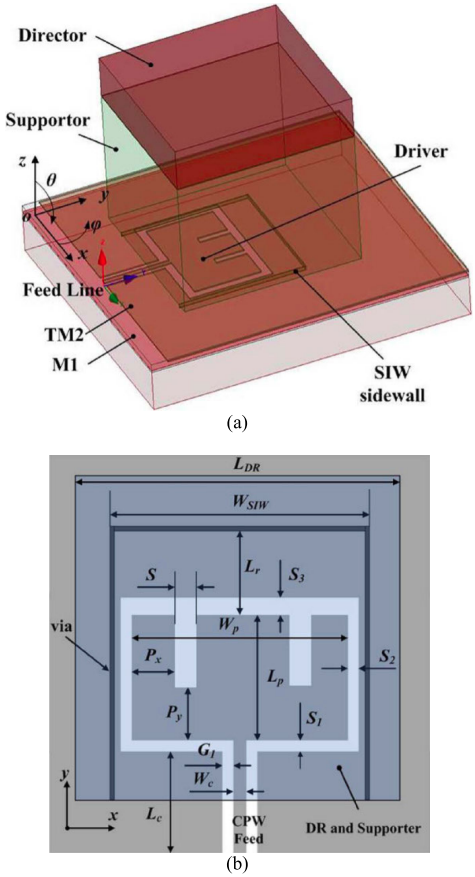

FIGURE 2. Configuration of the 3-D antenna on-chip constructed of an on-chip driver and a dielectric resonator director: (a) three dimensional view, and (b) top side [89].

In fact, miniaturizing an antenna while maintaining its gain and radiation efficiency is a challenging task [29], [30], [86], [87]. To overcome these issues, other technologies have been explored including MTM, MTS, and SIW [31]–[44]. It has been demonstrated that these technologies can significantly improve the gain and radiation efficiency of on-chip antennas.

A. STUDY ON MTM AND SIW-BASED ON-CHIP ANTENNA DESIGN FOR MILLIMETRE-WAVE AND THz INTEGRATED-CIRCUIT APPLICATIONS

A high-gain terahertz dielectric resonator on-chip antenna has been presented in [88] which is successfully tested applying a 0.18-μm CMOS technology by a dielectric resonator made of high-Z silicon material as shwon in Fig.1. The proposed on-chip antenna with thickness of 500 μm possesses a radiation gain and efficiency of 7.9 dBi and 74% at the operating frequency of 340 GHz, which enables it as a suitable candidate for transmissive THz circuits. The proposed dielectric resonator antenna has manufactured by using a wafer dicing.

A high-gain/efficiency 3-D antenna on-chip operating at 340 GHz is presented and investigated in [89]. The antenna based on a substrate integrated waveguide is realized and manufactured by the standard 0.13- m SiGe BiCMOS technology. The Yagi-like antenna has been established to achieve better radiation properties. The proposed structure, exhibited

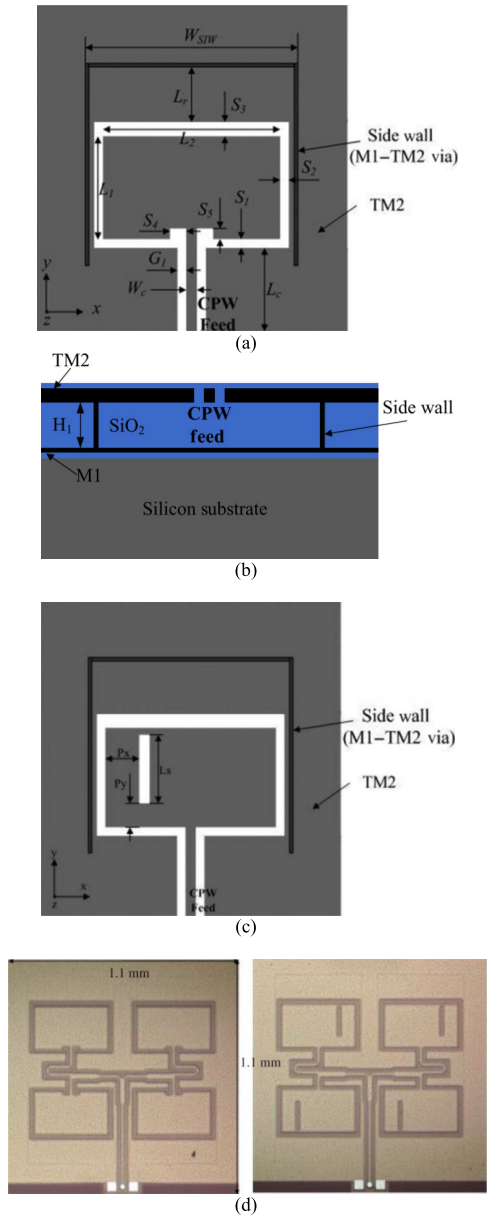

FIGURE 3. SIW cavity-backed magnetic rectangular slot loop antenna. (a) Top side of the structure without slot loading, (b) Side view of the structure without slot loading, (c) Top side of the antenna with slot loading, and (d) Array prototypes without (left-side) and with (right-side) slot-loading [90].

in Fig.2, with an overall size of 0.7 × 0.7 mm^2 provides a maximal gain and efficiency of 10 dBi and 80%, respectively.

In [90], a substrate integrtaed waveguide cavity-backed magnetic rectangular slot loop antenna on-chip in both single and array layouts have been realized and demonstrated, as displayed in Fig.3. A standard 0.13-μm SiGe BiCMOS technology has been applied for manufacturing without any post processes. In order to expand the frequency bandwidth, a slot is implemented in the upper wall of the structure. A maximum radiation efficeincy and gain of 48% and 7.9 dBi have ben attained at 340 GHz, respectively.

The paper [31] presents the results of a study on improving the performance parameters of on-chip antennas

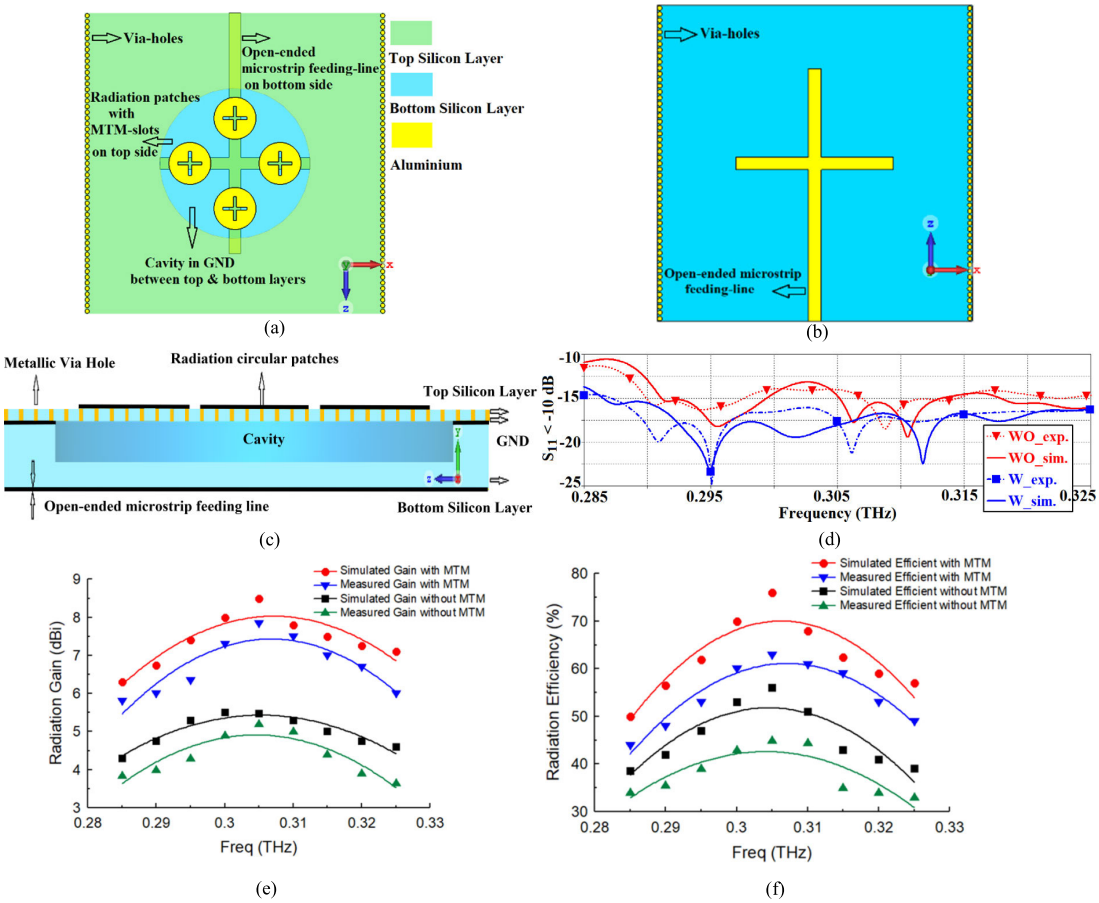

FIGURE 4. On-chip antenna with metamaterial-inspired crossed-shaped slot implemented on the radiation patches, (a) top-view, (b) back-view, (c) cross-section view showing the different layers of the on-chip antenna structure, (d) simulated (sim.) and experimental (exp.) reflection-coefficient responses of the antenna with no MTM (WO) and with MTM (W), (e) antenna gain response, and (f) radiation efficiency response [31].

for millimetre-wave and terahertz integrated-circuits. These parameters include the antenna's impedance bandwidth, gain and radiation efficiency. This was achieved by using the MTM and SIW technologies. The on-chip antenna structure, shown in Fig.4, comprises five alternating layers of metallization and Silicon. An array of circular radiation patches with MTM-inspired crossed-shaped slots are etched on the top metallization layer below which is a silicon layer whose bottom surface is metalized to create a ground-plane. Underneath the top silicon layer, a cavity is implemented which is not the ground-plane. Below the bottom silicon layer, an open-ended microstrip feedline is located which is used to excite the antenna. The feed mechanism is based on the coupling the EM-energy from the bottom silicon layer to the top circular patches through the cavity. To suppress surface-waves and reduce substrate loss, SIW concept is applied at the top silicon layer by implementing the metallic via-holes at the periphery of the structure that connect the top layer to the ground-plane. The on-chip antenna has an average measured gain and radiation efficiency of 6.9 dBi and 53%, respectively, across 0.285-0.325 THz, and dimensions of $1.35 \times 1 \times 0.06$ mm^3. The Silicon-based antenna structure provides low integration loss and is relatively simple to design and fabricate.

Table 1 compares the characteristics of the on-chip antenna investigated in [31] with other techniques. The novelty introduced includes: (i) the feed mechanism for effective coupling EM-energy from bottom layer to the top radiation patches; (ii) almalgamation of MTM-inspired and SIW technologies to improve the antenna's performance without comprosmising its physical dimensions; and (iii) stacking the substrate layers to create a highly compact structure. The results show that, compared to other types of antennas, the proposed technique in [31] yields an excellent fractional bandwidth. The gain and efficiency of this antenna is comparable to other techniques and in some cases better. In addition, compared to previously reported on-chip antenna designs the proposed design in [31] is of a simpler structure and easy to fabricate at low cost, which makes it viable for mass production and therefore a promising candidate in the millimeter-wave and terahertz integration applications.

B. STUDY ON SILICON-BASED HIGH-GAIN ON-CHIP ANTENNA DESIGN WITH APERTURE EXCITATION FOR TERAHERTZ APPLICATIONS

A miniaturized and feasible 60 GHz circular monopole antenna on-chip with an artificial magnetic conductor

TABLE 1. Performance parameters comparison of the recently published on-chip antennas.

Ref.	Antenna Type	Operation Mode	Freq. / BW (GHz / %)	Gain (dBi)	Eff. (%)	Fab. Process	DR Material εr	DR Type	Size (mm^2)	Height (mm)
[88]	Patch fed higher order mode DRA	$TE_{\delta 17}$	340 / 7	7.9	74	0.18-µm CMOS	11.9	Rectangular	0.2	0.5
[89]	On-chip 3D (Yagi like concept)	$TE_{11\delta}$	340 / 12	10	80	0.13-μm SiGe BiCMOS	10	Rectangular	0.49	0.43
[90]	Slot loaded magnetic loop on SIW	-	340 / 7	3.3	45	0.13-µm SiGe BiCMOS	NA	NA	0.49	-
[91]	Patch	-	280 / 2.5	–1.6	21	0.13-μm CMOS	NA	NA	0.2	-
[92]	Ring antenna	-	296 /-	4.2	-	65-nm CMOS	NA	NA	0.3	-
[93]	Slot ring antenna + superstrate	-	375 / 8	1.6	35	45-nm CMOS SOI	NA	NA	0.05	-
[94]	Ring antenna with silicon lens	-	288 / NA	18.3	65	65-nm CMOS	NA	NA	12.56	2.55
[95] - a	Half-mode cavity fed DRA	$TE_{\delta 11}$	135 / 13	3.7	62	0.18-μm CMOS	10	Rectangular	0.63	0.25
[95] - b	Half-mode cavity fed higher order mode DRA	$TE_{\delta 13}$ / $TE_{\delta 15}$	135 / 7	6.2 / 7.5	46 / 42	0.18-μm CMOS	10	Rectangular	0.72	1.3/2.2
[96]	Slot fed stacked DRA	$TE_{\delta 11}$	130 / 11	4.7	43	0.18-μm CMOS	10	Rectangular	0.72	1.5
[97]	DRA	$TE_{\delta 11}$	135 / 11	2.7	43	0.18-μm CMOS	10	Rectangular	0.72	0.6
[31]	MTM & SIW	$TE_{11\delta}$	305 / 13.11	8.05	62.95	0.13-μm CMOS	NA	NA	2.35	0.06

Note: DR represents Dielectric Resonator, and NR is not applicable.

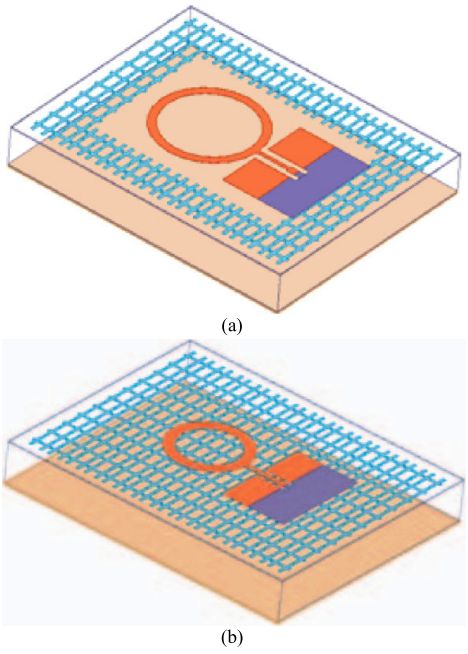

FIGURE 5. Antenna on-chip with (a) 7 × 9 artificial magnetic conductor units blank and (b) full artificial magnetic conductor plane [98].

structure has been designed and discussed in [98], as shown in Fig.5. The proposed structure has been implemented using the conventional 0.18-μm CMOS silicon technology. It was exhibited that the circular monopole antenna on-chip loaded with the artificial magnetic conductor can exhibit higher radiation properties across the entire working frequency band between 57 GHz to 66 GHz, compared to antennas without an artificial magnetic conductor load.

A antenna on-chip with circular polarization utilizing a modified artificial magnetic conductor structure to enhance the performance parameters has been modelled and realized in [99], which employs the standard 0.18-μm CMOS process. Its prototype consisting of a modified artificial magnetic conductor structure, as displayed in Fig.6, occupies $1.8 \times 1.8 \times 0.3$ mm^3 footprint area. The highest radiation gain at 60 GHz spot frequency is -4.4 dBi. The operating band with circular polarization can cover the frequency range between 57 GHz to 67 GHz. The proposed antenna on-chip can be integrated to CMOS circuits for further applications at 60 GHz wireless communications.

The work in [32] investigates the feasibility of designing a high-gain on-chip antenna on silicon technology for sub-THz applications. Fig. 7 shows the antenna structure which is implemented on Silicon substrate. High gain is achieved by exciting the antenna using an aperture fed mechanism to couple EM-energy from a metal slot-line, which is sandwiched between the silicon and polycarbonate substrates, to a periodic array of 15-element comprising circular and rectangular radiation patches fabricated on the top surface of the polycarbonate layer. An open-ended microstrip line, which is orthogonal to the metal slot-line, is implemented on the underside of the silicon substrate. When the open-ended microstrip line is excited, it couples the RF energy to the metal slot-line, and this energy in turn is coupled to the patch array. The measurement results in Fig.7 show the proposed on-chip antenna exhibits a reflection-coefficient of better than -10 dB across 0.290 THz to 0.316 THz. A maximum gain and radiation efficiency achieved by this structure are 11.71 dBi and 70.8%, respectively, at 0.3THz. The physical size of the sub-THz antenna is $20 \times 3.5 \times 0.126$ mm^3.

The performance parameters of the silicon-based on-chip antenna proposed in [32] is compared to recently published mmWave antennas in Table 2. It is evident that previous

TABLE 2. State-of-the-art comparison of the on-chip antennas.

Ref.	Antenna Type	Meas. Freq. Band (GHz)	Meas. Gain (dBi)	Meas. Eff. (%)	Size (mm^3) or (mm^2)	Process
[98]	Ring-shaped Monopole	50-70	≤0.02	≤ 35	-	0.18-μm CMOS silicon
[99]	Circular Open-loop	57-67	≤ -4.4	-	1.8×1.8 ×0.3	CMOS 0.18-µm
[100]	Bowtie-slot	90-105	≤-1.78	-	0.71×0.31× 0.65	IHP 0.13-µm Bi-CMOS
[101]	Differential-fed Circularly Polarized	50-70	≤-3.2	-	1.5×1.5 ×0.3	CMOS 0.18-µm
[102]	AMC embedded squared slot antenna	15-66	≤ 2	-	1.44×1.1	CMOS 0.09-µm
[103]	Monopole	45-70	≤4.96	-	1.9×1.9×0.25	silicon CMOS
[104]	Dipole-Antenna	95-102	≤4.8	-	-	Bi-CMOS
[32]	Coupled Feeding Mechanism	290-316	≥9.6	≥55	20×3.5×0.126	Standard 120-µm silicon

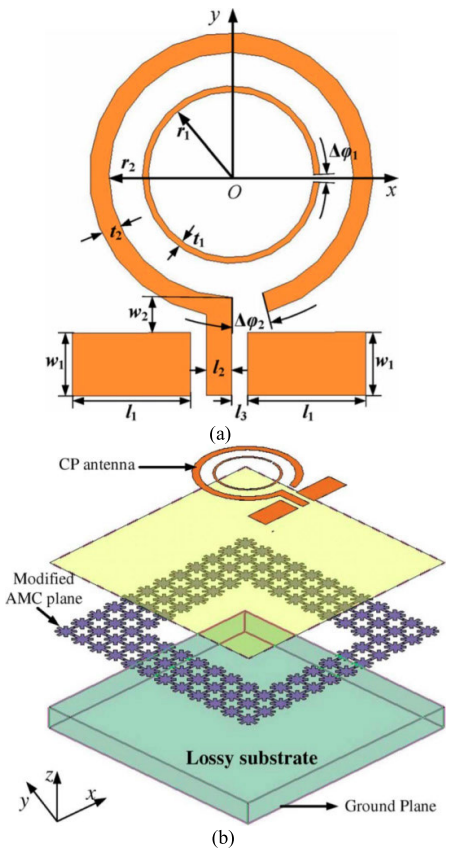

FIGURE 6. (a) Configuration of the antenna on-chip with circular polarization, (b) proposed antenna with modified artificial magnetic conductor plane [99].

works are based on newer fabrication processes of 0.09-μm, 0.13-μm, and 0.18-μm technologies however in [32] the on-chip antenna was fabricated on a standard 120-μm process as the smallest dimension in the design is limited to 200-μm. The purpose of this investigation was to determine how much the operating frequency could be extended using the standard silicon technology. Compared to the publications cited in the table, the antenna in [32] has a higher gain and radiation efficiency. Additionally, it works at a significantly higher frequency band of 290-316 GHz.

C. STUDY ON IMPROVING THE PERFORMANCE PARAMETERS OF MTS-BASED ON-CHIP ANTENNA

A CMOS 0.18-μm process-based antenna on-chip with high radiation properties operating across V-band has been designed and demostrated in [105]. As shown in Fig. 8, a silicon layer, dielectric resonator, and an off-chip ground layer have been applied in this model to increase the gain and reduce the physical dimensions. The proposed structure provides a highest radiation efficiency and gain of 96.7% and 8 dBi, respectively, over the operating frequency band of 65 GHz to 69 GHz. The good performance is achieved with a chip area of 0.875 mm^2.

A GaN-on-low resistivity silicon layer-based viable microstrip antenna array operating over frequency band of 259 GHz to 291 GHz has been realized and discussed in [106]. To reduce the losses created by the substrate layer and to increase the performance of the integrated antenna array at terahertz spectrum, the microstrip patch has shielded with silicon nitride and gold layer in addition to a layer of benzocyclobutene. The proposed 4 × 1 linear array antennas depicted in Fig.9 resonates at 273 GHz with an impedance matching of −40 dB. The array shows a directivity, radiation gain and efficiency of 11.2 dB, 5.2 dB, and 20% respectively, for a 5 μm BCB inset. The presented antenna array on benzocyclobutene proposes a promising technology for the integration of high RF performance active devices and passive elements for the realization of terahertz monolithic integrated circuits.

The feasibilityy of a two-element broadband octagonal shorted annular ring on-chip antenna array with high radiation specifications has been studied in [107]. The octagonal shorted annular ring approach has been utilized to increase the gain and suppress the surface-waves based on 130-nm SiGe BiCMOS. The footprint area of the antenna exhibited in Fig.10 is 550 × 1100 μm^2. It operates over a frequency band of 303 GHz to 320 GHz with −10-dB impedance bandwidth of 17 GHz. The antenna possesses 4.1 dBi gain at 320 GHz. The results show that the proposed on-chip antenna structure can be a promising candidate for THz communication systems.

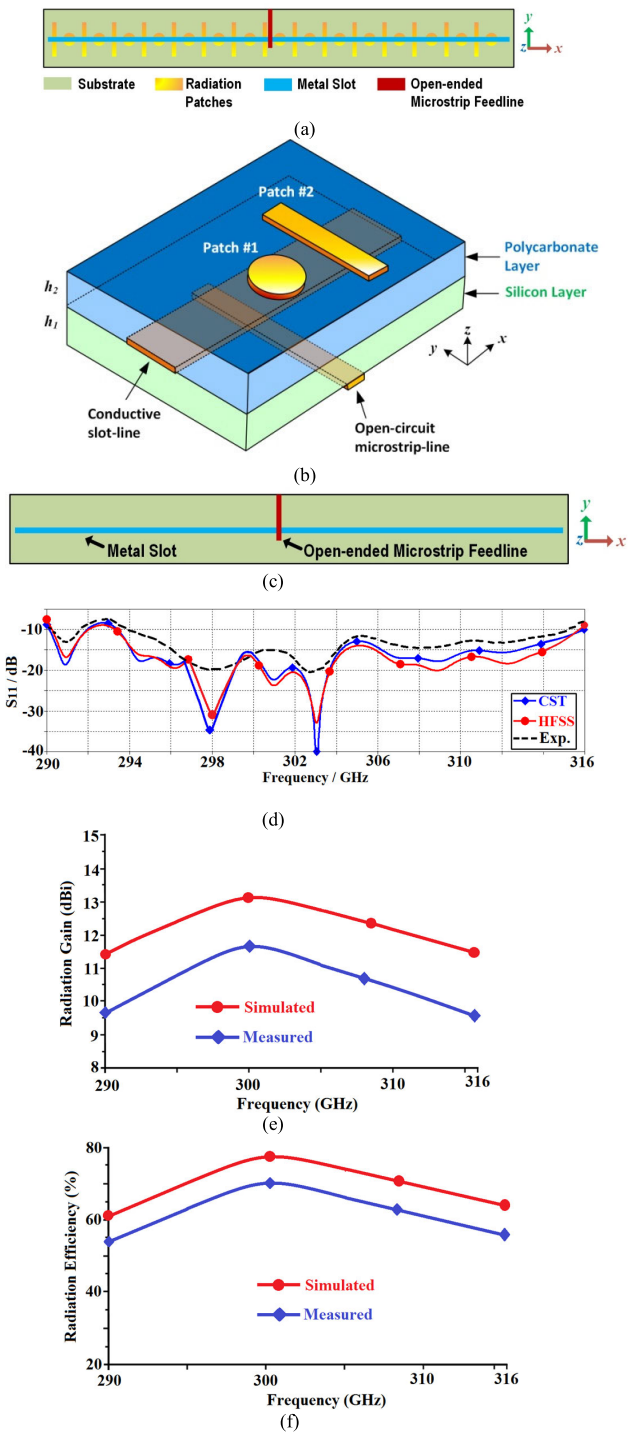

FIGURE 7. Silicon-based integrated on-chip antenna, (a) top-side, (b) side-vision, (c) back view, (d) reflection-coefficient responce, (e) gain response, and (f) radiation effienicy response [32].

In [33], a feasibility study was carried out on a novel on-chip antenna based on MTM technology at THz band. The proposed MTM on-chip antenna is constructed on an electrically thin high-permittivity gallium arsenide (GaAs) substrate layer, as illustrated in Fig.11. The MTM is implemented by engraving slot-lines on an array of 11 × 11 circular patches, which are fabricated on the top layer of the

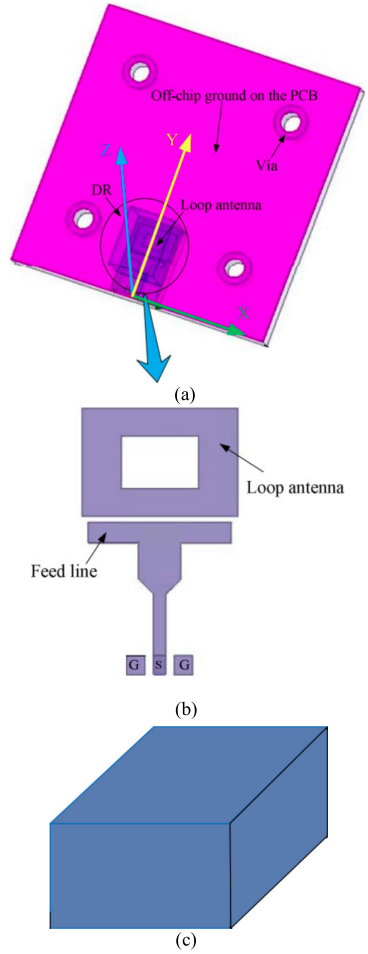

FIGURE 8. (a) Configuration of the V-band on-chip dielectric resonator antenna contsructed of three parts (i) a loop antenna, (ii) a dielectric resonator antenna, and (iii) a layer of off-chip ground. (b) loop antenna, (c) dielectric resonator antenna [105].

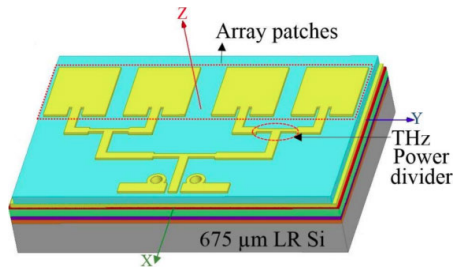

FIGURE 9. 3-D schematic of the proposed THz monolithic integrated circuit 4 × 1 array antennas [106].

GaAs substrate. Metallic via-holes are implemented in the central patch of each row constituting the array to connect the patch to the leaky-wave open-ended slot-line feed running underneath the patches. The slot-lines are connected to each other with a slit. A waveguide port is used to excite the array via slot-lines that couples the EM-energy to the patches. The on-chip antenna is shown to exhibit an average measured gain that is more than 10 dBi and radiation efficiency above 60% over a wide frequency range from 0.41 THz to 0.47 THz. This is a significant development over other on-chip antenna techniques reported to date. Dimensions of the antenna are $8.6 \times 8.6 \times 0.0503$ mm^3. The results show that the proposed

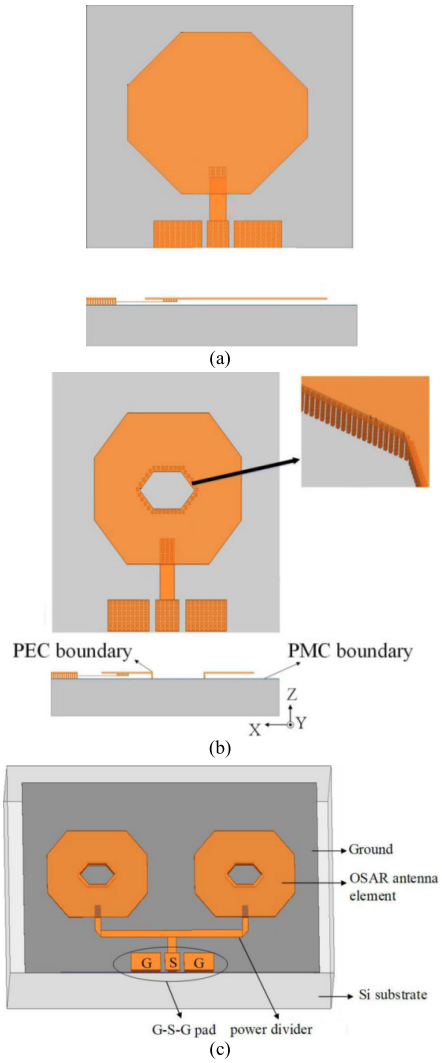

FIGURE 10. **(a) Single element octagonal microstrip antenna, (b) single element octagonal shorted annular ring on-chip antenna, and (c) 320 GHz two-element octagonal shorted annular ring on-chip antenna array [107].**

GaAs-based MTM on-chip antenna is viable for applications in THz integrated circuits.

Performance parameters of the GaAs-based on-chip antenna with MTS slot-lines reported in [33] are compared to other recently published mmWave antennas in Table 3. The comparison shows that the proposed MTS on-chip antenna in [33] operates at a much higher frequency from 410 GHz - 470 GHz, which to the authors' knowledge is demonstrated for the first time. In addition, this antenna has comparable gain and radiation efficiency to the cited references in Table 3. Compared to other antennas cited in Table 3, the on-chip antenna in [33] is less complex and cost effective to implement in practice, which makes it a viable candidate for applications in THz integrated circuits.

D. STUDY ON HIGH-GAIN CRLH-TL-BASED ON-CHIP ANTENNA FOR SUB-THz INTEGRATED CIRCUITS

An efficient antenna on-chip realized by the back-end-of-line process of the conventional CMOS silicon technology is designed and studied in [109]. The proposed antenna resonates at 60 GHz, has the dimensions of 1.5 mm by 1.0 mm and consists of a feed line and pads which are the integral parts of the antenna as exhibited in Fig.12. The results demostrate that the on-chip antenna attains a highest radiation gain and efficiency around of 0.11dBi and 39% at 60 GHz, respectively, along with a VSWR < 1.5 over the frequency band of 51.5 - 70.6 GHz and a impedance matching of 36 dB at 60 GHz. The results explain that the proposed on-chip antenna can be a promising candidate for integration in millimeter-waves and sub-terahertz circuits.

Deployment of the advanced 130nm SiGe HBT silicon technology for high data-rate communication at 240 GHz has been proposed and discussed in [110]. This work investigates the realization of an integrated antenna on-chip transmitter and receiver modules, which is implemented by two single-chip TX and RX front-end circuits as depicted in Fig.13. 7.5dBm output power with a 3-dB RF bandwidth of 40GHz has been delivered by the transmitter chip, while a noise figure and maximum conversion gain and of 15 dB and 11dB, respectively, have been exhibited by the receiver chip. In combination with a silicon lens with a 9 mm diameter, both TX and RX modules provides an average directivity of 26.4 dBi, which allows for high-speed communication at a distance of 1 m or higher.

A simple design of small orthogonally polarized antenna on-chip to implement 300 GHz full-duplex communication system with low interfaces has been proposed in [111]. As shown in Fig.14, it was constructed of a disk-loaded monopole antenna and a dipole antenna for vertical and horizontal polarizations, respectively. The disk-loaded monopole antenna and dipole antenna have proper cross-polarization states with > 90 dB of self-isolation value. Consequently, they can be applied to obtain low interactions between transmitting and receiving antennas. The two antennas with dual polarization have been adopted in two separated transceivers to study their interface behaviour. The overall size of the antenna is $390 \times 300 \times 78\ \mu m^3$, so it can be a potential candidate for applications in integrated circuits and multiple-input multiple-output systems across the THz spectrum.

Reference [34] presents a novel on-chip antenna using standard CMOS-technology based on 2D composite right/left-hand (CRLH) metasurface implemented on two-layers polyimide substrates with a thickness of $500\mu m$ and using artificial magnetic conductor (AMC) structure. The proposed sub-THz on-chip antenna is is shown in Fig.15. The aluminium ground-plane of thickness of $3\mu m$ is sandwiched between the two-layers. The AMC comprises concentric dielectric-rings which are etched in the ground-plane sandwiched between the two-polyimide substrates and under the radiation patches implemented on the top-layer. This approach suppresses the surface waves and reduce substrate losses. The radiation patches comprise concentric metal-rings that are arranged in a 3×3 matrix. The antennas are excited by coupling EM-energy through the gaps of concentric dielectric-rings in the ground-plane using a

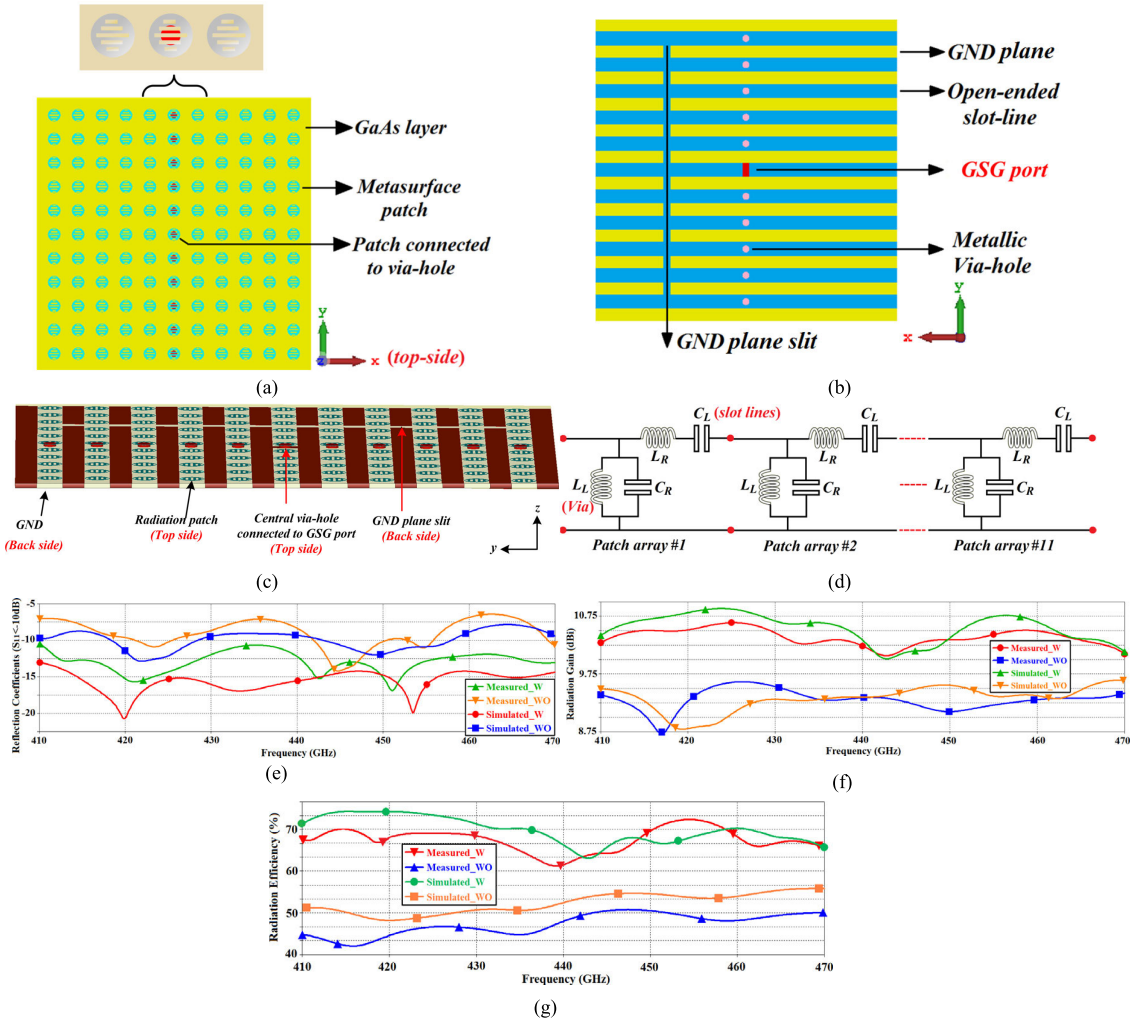

FIGURE 11. On-chip antenna design comprising an array of 11 × 11 circular patches with metasurface, (a) top-view, (b) back-side, (c) 3D isometric-view, (d) equivalent circuit model, (e) reflection-coefficient response without (WO) and with (W) metasurface slot-lines, (f) gain response, and (g) radiation efficiency response [33].

TABLE 3. Salient features comparison of the on-chip antennas publicationed in literature.

Ref.	Type	BW / [Freq. range] (GHz)	Gain (dBi)	Eff. (%)	Size	Process
[105]	Loop antenna	4 / [65-69]	Max. 8	Max. 96.7	0.7×1.25 mm^2	CMOS 0.18-µm
[106]	4×1 Patch antenna array	32 / [259-291]	Max. 5.2	-	2.47×1.53×0.675 mm^3	0.675-μm GaN
[107]	2×1 Octagonal shorted annular ring on-chip antenna array	17 / [303-320]	Max. 4.1	Max. 38	0.55×0.5×0.3 mm^3	0.13-μm SiGe BiCMOS
[108]	8×8 Magneto-electric dipole antenna array	14.7 / [130.3-145]	Max. 20.5	Max. 59.2	32×20×0.818 mm^3	LTCC
[33]	Metasurface on-chip antenna	60 / [410-470]	Min. 10	Min. 60	8.6×8.6×0.0503 mm^3	Standard 50μm GaAs layer

microstrip feedline created on the bottom polyimide-layer. The open-ended feedline is split in three-branches that are aligned under the radiation elements to couple the maximum energy. In this structure, the concentric metal-rings essentially act as series of left-handed capacitances that extend the effective aperture area of the antenna without affecting its dimensions, and the concentric dielectric rings etched in the ground-plane act as shunt left-handed inductors. This structure suppresses the surface-waves and reduces the substrate losses that leads to improved bandwidth and radiation properties. The overall structure behaves like a metasurface that is shown to exhibit a very large bandwidth

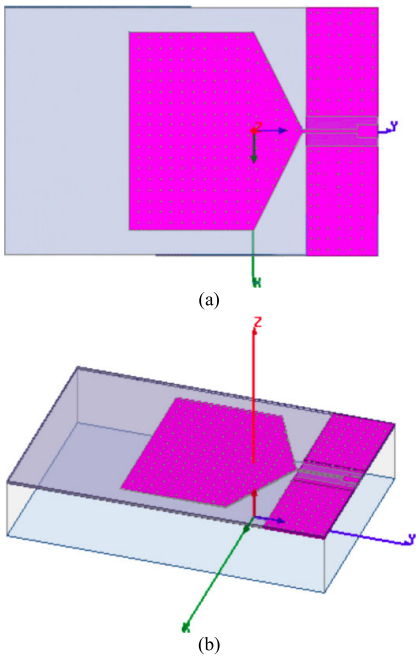

FIGURE 12. On-chip antenna structure, (a) top-side, and (b) isometric view [109].

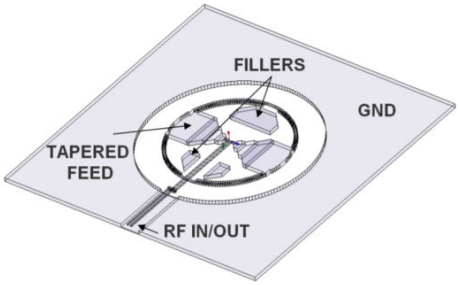

FIGURE 13. On-chip antenna integrated in the transmitter and receiver modules [110].

from 0.350-0.385 THz with an average gain and radiation efficiency of 8.15 dBi and 65.71%, respectively, as shown in Fig.15. The antenna has dimensions of $6 \times 6 \times 1\text{mm}^3$.

In Table 4, the performance of the on-chip antenna demosntrated in [34] is compared with other types of mmWaves and THz antennas. The comparison shows the antenna in [34] operates at a much higher frequency and has comparable gain to [110] but its efficiency is not reported. Although its dimensions are larger than other cited antennas, however the proposed antenna is less complex to implement.

E. ANTENNA ON CHIP DESIGN USING MTS AND SIW TECHNOLOGIES FOR THz WIRELESS APPLICATIONS

In [108], various antennas in array configurations working at 37, 45, and 140-GHz over the millimeter-wave and terahertz spectrum have been designed and investigated. The layout of the 8×8 magneto-electric array antennas based on the 37-GHz substrate integrated waveguide-fed is shown in Figs.16 (a) and (b). The radiating elements are constructed of cavities and metallic posts. To improve the impedance bandwidth and achive high radiation properties, the metallic cross slots have been loaded overhead of the substrate

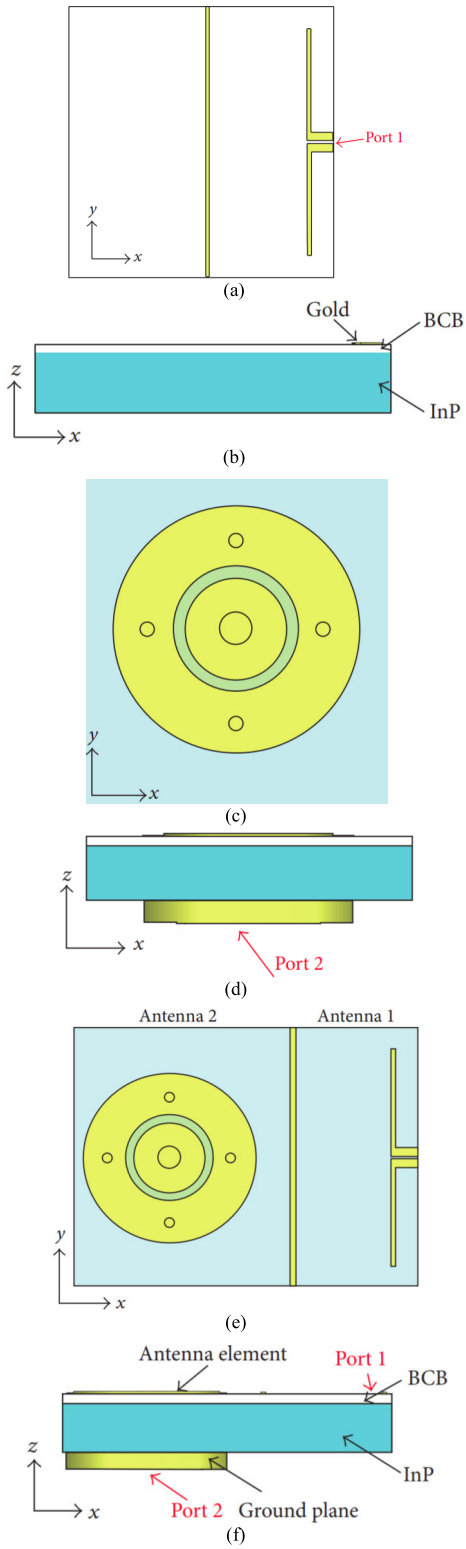

FIGURE 14. (a) Top-side of the dipole antenna horizontally polarized, (b) side view of the dipole antenna with different layers, (c) top-view of the vertically polarized monopole antenna, (d) side-view of the vertically polarized monopole antenna, (e) top-view of the dual-polarized antenna topology, and (f) side-view of the dual-polarized antenna topology [111].

integrated waveguide slots. So, the second 4×4 array antenna is loaded with metallic cross slots and its feeding mechanism is based on the 45-GHz substrate integrated waveguide-fed as

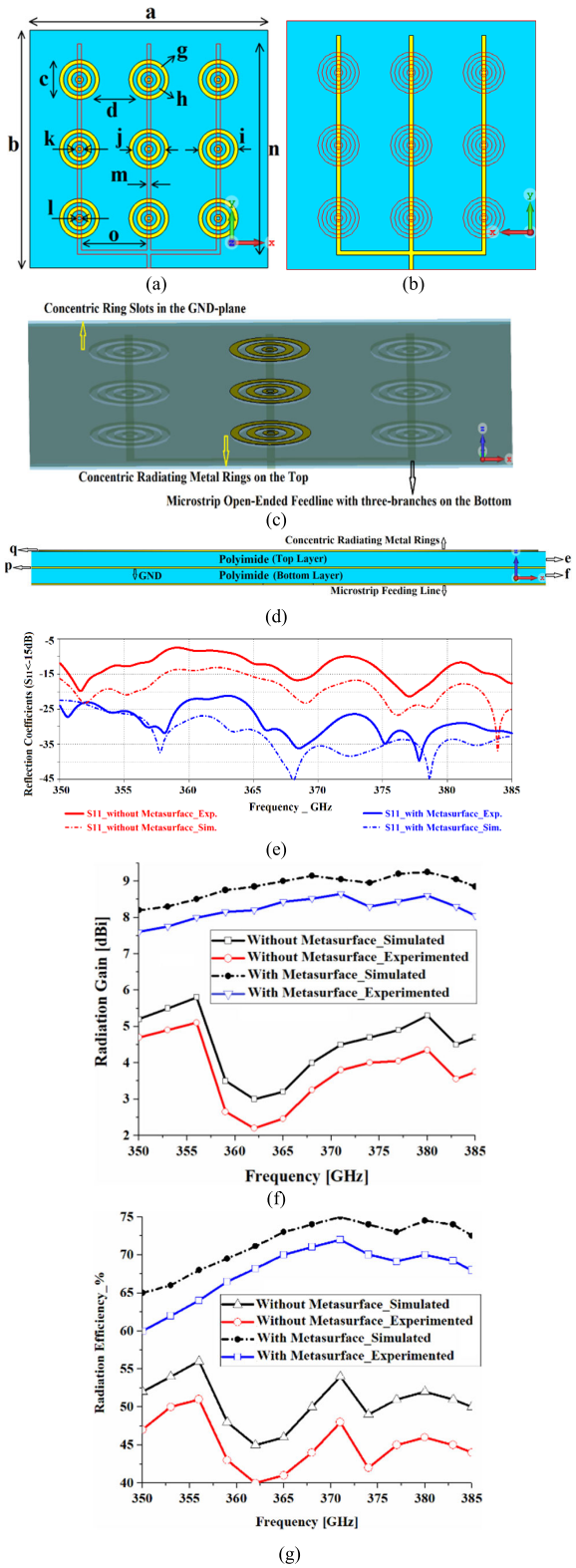

FIGURE 15. On-chip antenna with AMC metasurface structure, (a) top view, (b) back view, (c) concentric dielectric rings antennas (shown in yellow) in the middle layer, (d) cross-section view, (e) reflection-coefficient responses, (f) gain response, and (g) radiation efficiency response [34].

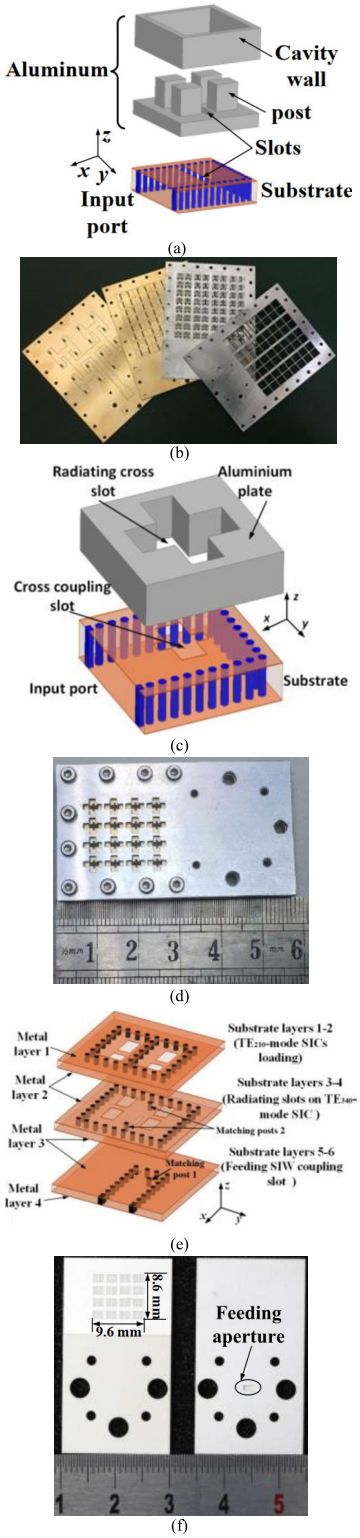

FIGURE 16. (a) 37-GHz SIW-fed magneto-electric dipole antenna element, (b) 37-GHz SIW-fed magneto-electric 8 × 8 dipole antenna arrays, (c) 45-GHz SIW-fed cross slot antenna element, (d) 45-GHz SIW-fed cross slot antenna arrays, (e) 140-GHz high order mode substrate integrated cavities 2 × 2 slot subarray antennas, and (f) 140-GHz high order mode SIC 8 × 8 slot antenna arrays (left side: front view, right side: top view) [108].

exhibited in Figs.16 (c) and (d). To attain more compact structure along with lower loss feeding network a TE340-mode substrate integrated cavities stimulated 8 × 8 slot array antennas has been implemented as third design which operates at

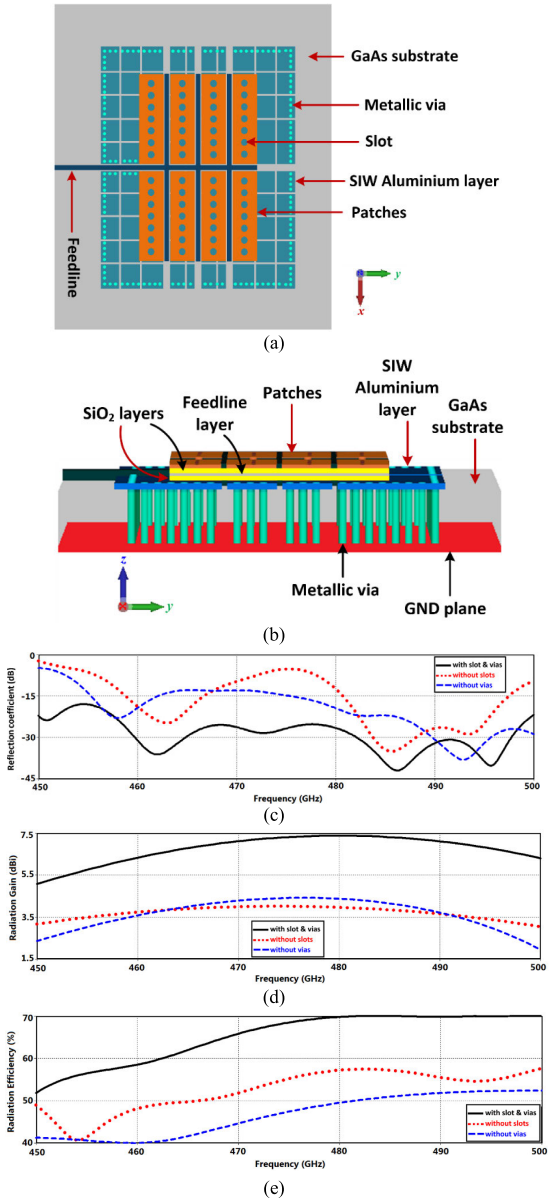

FIGURE 17. **AoC incorporating metamaterial and SIW technologies, (a) top view, (b) side view, (c) reflection-coefficient response, (d) gain response, and (e) radiation efficiency response [35].**

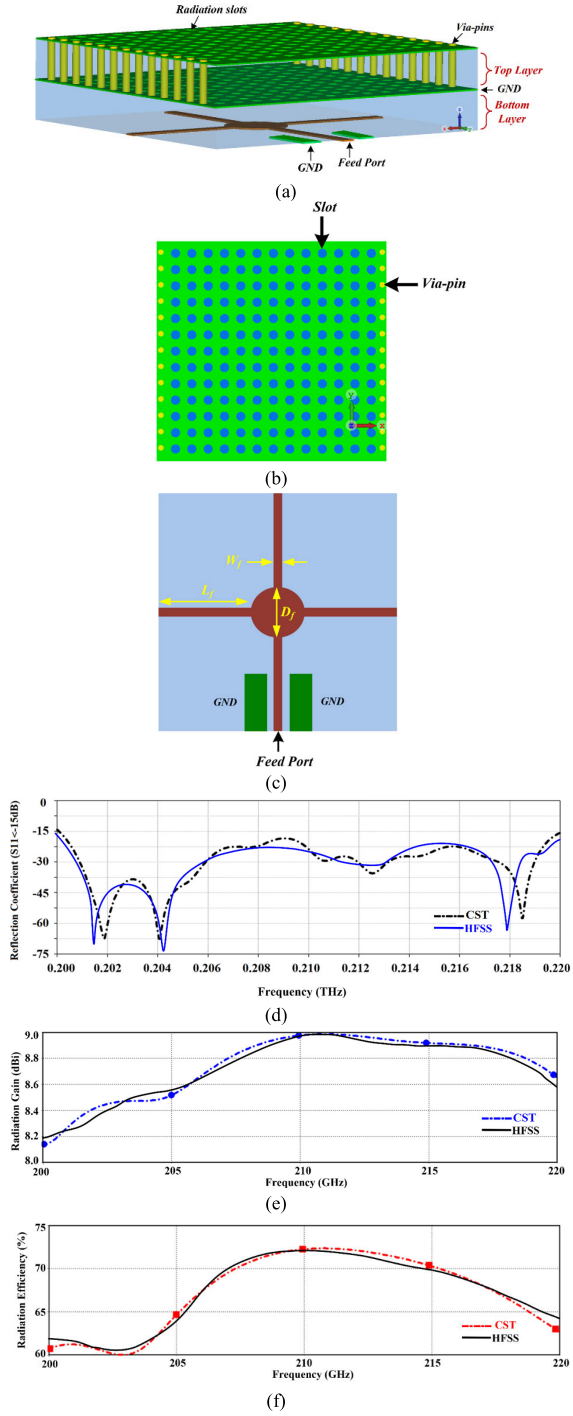

FIGURE 18. **AoC implemented using MTS and SIW technologies, (a) isometric view, (b) top view, (c) bottom side, (d) reflection-coefficient responses, (e) gain response, and (f) radiation efficiency response [36].**

140 GHz in LTCC process as displayed in Figs.16 (e) and (f). As result, wideband operation and high radiation performance has been obtained in the three various designs of millimeter-wave and terahertz antenna arrays based on PCB or LTCC process. These antenna arrays can be potential candidates for millimeter-wave and terahertz wireless communication systems.

Reference [35] presents an innovative design of a high-performance 0.45–0.50 THz antenna on-chip (AoC) for fabrication on a 100-micron GaAs substrate. The antenna is based on MTS and SIW technologies, which is shown in Fig.17. It consists of seven stacked layers of copper patch–silicon oxide–feedline–silicon oxide–aluminium–GaAs–copper ground. The top layer consists of a 2 × 4 array of rectangular metallic patches with a row of subwavelength circular slots to transform the array into a metasurface. The MTS essentially enlarges the effective aperture area of the antenna. The antenna is excited using a coplanar waveguide feedline that is sandwiched between the two silicon oxide layers below the patch layer. The proposed antenna structure reduces substrate loss and surface waves. The AoC has dimensions of 0.8 × 0.8 × 0.13 mm^3. The results in Fig.17 show that the proposed structure greatly enhances the

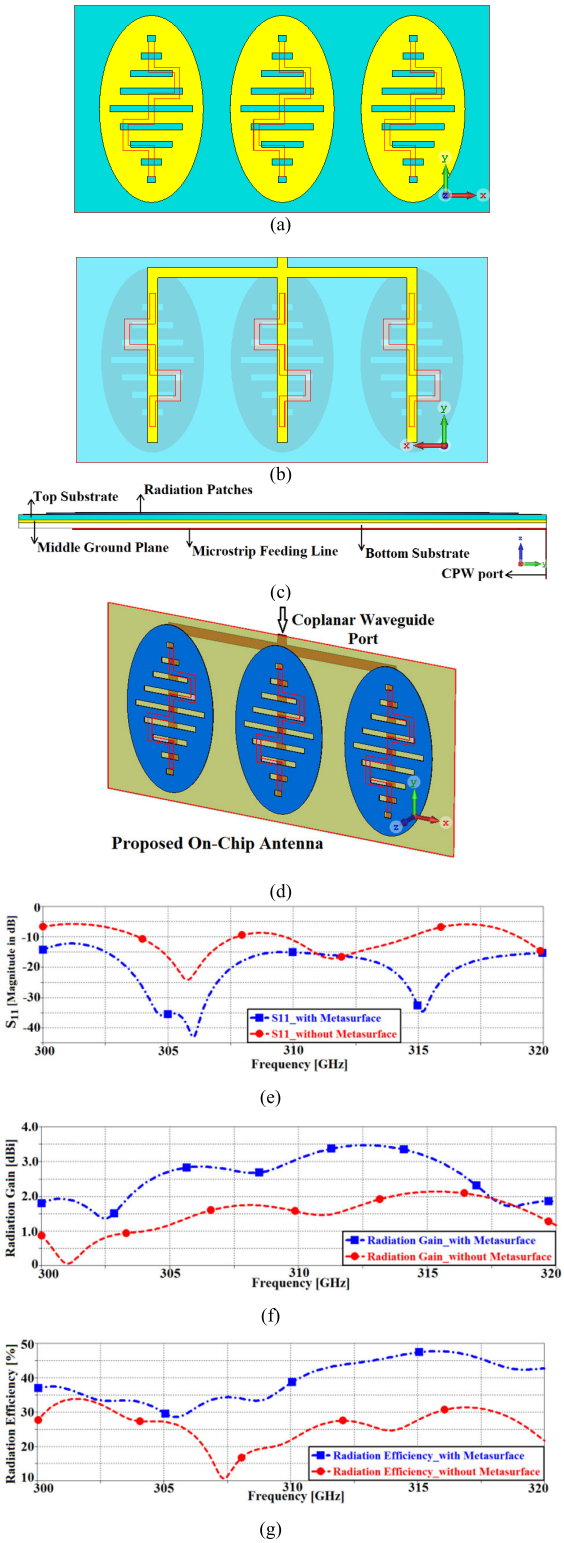

FIGURE 19. On-chip antenna with metasurface concept, (a) top-view, (b) bottom view, (c) side-view, (d) isometric view, (e) reflection-coefficients, (f) gain esponse, and (g) radiation efficency esponse [37].

antenna's gain and radiation efficiency, without compromising its physical size. The antenna exhibits an average gain and efficiency of 6.5 dBi and 65%, respectively. Compared to most AoCs reported in the literature, the proposed antenna has a larger frequency bandwidth and operates at a much higher frequency with comparable gain and radiation efficiency, which makes it a promising candidate for emerging terahertz applications.

Table 5 compares the salient features of the on-chip antenna realized in [35] with AoC reported in the literature. The maximum gain of the antenna in [35] of 7.4 dBi is lower than [108], but it is higher than in other reported works. Additionally, it has a maximum efficiency of 70%, which is higher than all previously reported works. Compared to the cited works in Table 5, the antenna in [35] operates over a much higher frequency (between 450 and 500 GHz). It is much less thick with respect to the operating wavelength than other on-chip antennas reported to date. This is attributed to combining MTS and SIW technologies in the implementation of the on-chip antenna. The thinner antenna structure is important to prevent the generation of surface or substrate modes that can adversely affect the antenna's performance, especially at THz frequencies [112].

F. COMPACT ON-CHIP ANTENNA USING UNDERSIDE EM COUPLING MECHANISM FOR THz FRONT-END TRANSCEIVERS

The results presented in [36] are obtained by a combination of MTM and SIW technologies to create a compact and low-profile antenna that overcomes the drawbacks of narrow-bandwidth and low radiation properties encountered by other THz AoCs. The proposed antenna in Fig.18 uses an RF cross-shaped feed structure to excite the antenna from its underside, by coupling EM-energy through the multi-layered structure. The feed mechanism facilitates integration with integrated circuits. The proposed antenna is constructed from five stacked layers comprising of metal–Silicon–metal–Silicon–metal. Dimensions of the AoC are $1\times1\times0.265$ mm^3. The AoC has an impedance match, radiation gain and efficiency of ≤-15 dB, 8.5 dBi and 67.5%, respectively, over a frequency range of 0.20–0.22 THz. The antenna's radiation pattern is stable over its operating frequency band. This is achieved by coupling EM-energy through the silicon layers to the circular slots implemented on the metallised silicon layers. These results confirm that the proposed AoC design is compatible for full integration in THz transceivers and THz on-chip front-end wireless systems.

G. HIGH PERFORMANCE MTS BASED ON-CHIP ANTENNA FOR THz INTEGRATED CIRCUITS

Reference [37] presents a relatively simple prototype of a MTS based on-chip antenna operating in 0.3-0.32 THz. The proposed structure, illustrated in Fig.19, is constructed from two layers of polyimide-substrates with thickness of 0.1 mm that sandwich the middle 50-micron thickness metallic ground-plane layer. Implemented on the top polyimide layer are three elliptical radiators with embedded dielectric and linear slots of different length to create a MTS that is established by the interaction of the EM-fields between

TABLE 4. Comparison of the on-chip antennas specifications available in the literature.

Refs.	Antenna Type	Frequency Band (GHz)	Gain (dBi)	Efficiency (%)	Dimensions (λ_0 @ 350 GHz)	Process
[109]	Tab monopole	45-75	Max. 0.1	Max. 42	1.75×1.16	Standard CMOS Silicon
[110]	Transmitter and receiver modules	218-246	Average 8.5	-	3.19×0.68	130-nm SiGe HBT silicon Technology
[111]	Monopole antenna	~300	Max. 1.72	-	0.35×0.35×0.09	InP 50- µm Substrates
[34]	Metasurface & EM coupled feed mechanism	>350	Min. 7.58	Min. 60.85	7.0×7.0×1.16	Standard 500-µm Polyimide

TABLE 5. AoC's specification comparison reported in the literature.

Ref.	Antenna Design	Fractional Bandwidth (%) (Freq. Range (GHz))	Gain (dBi)	Eff. (%)	Dimensions (Physical and Electrical)
[106]	Patch array antenna	11.6 [259–291]	Max. 5.2	-	$2.47 \times 1.53 \times 0.675$ mm^3 $2.14\lambda_0 \times 1.33 \times 0.586\lambda_0$ @259 GHz
[107]	Octagonal shorted annular ring array antenna	5.4 [303–320]	Max. 4.1	Max. 38	$0.55 \times 0.5 \times 0.3$ mm^3 $0.555\lambda_0 \times 0.505 \times 0.303\lambda_0$ @303 GHz
[108]	Dipole array antenna	10.7 [130.3–145]	Max. 20.5	Max. 59.2	$32 \times 20 \times 0.818$ mm^3 $13.91\lambda_0 \times 8.69 \times 0.355\lambda_0$ @130.3 GHz
[35]	Metasurface and SIW	10.5 [450–500]	Max. 7.4	Max. 70	$0.8 \times 0.8 \times 0.13$ mm^3 $1.21\lambda_0 \times 1.21\lambda_0 \times 0.196\lambda_0$ @450 GHz

the slots. This is shown to enhance the antenna's effective aperture area and improve its radiation performance without affecting the overall footprint of the antenna. To reduce the surface-waves and substrate-losses, a meander-line slit is realized inside the ground-plane. The antenna is fed by an open-ended microstrip feedline located on the bottom-layer. The feedline consists of three-branches that are aligned under each radiation patch to maximise EM-energy transfer from bottom-side of the bottom layer to the upper side of the top-layer. Coupling of the EM-energy from the bottom-layer to the top-layer occurs via meander-line slits introduced between the two layers. The results confirm that the proposed on-chip antenna shows superior performance in terms of impedance bandwidth, gain and radiation efficiency compared to the antenna without MTS. Fig.19 shows that the proposed on-chip antenna operates over 0.30 THz to 0.32 THz. It is shown that after creating the metasurface, an average improvement of 11dB is achieved in the impedance match. The average gain and radiation efficiency of the proposed on-chip antenna are 2.5 dBi and 40%, respectively.

H. GaAs-BASED TRANSCEIVER WITH ON-CHIP SLOTTED MTM ANTENNA USING SIW TECHNOLOGY

A novel on-chip antenna that is fully integrated in a 0.3-0.31 THz transceiver is reported in [38]. The antenna is implemented on a 0.5μm GaAs substrate. The transceiver, shown in Fig.20, comprises a voltage-controlled oscillator (VCO), a buffer amplifier, a modulator stage, a power-amplifier, a frequency-tripler, and an on-chip antenna. The on-chip antenna is constructed using SIW technology and comprises 4 × 4 longitudinal and transverse array slots that are realized using MTM technology. The SIW antenna also exhibits high-pass filter functionality to suppress unwanted harmonics and radiate the desired signal. Dimensions of the on-chip antenna are 2 × 1 × 0.0006 mm^3. The proposed on-chip antenna has a minimum and average gain and efficiency of 0.25 dBi & >1.0 dBi, and 46.12% & ~55%, respectively. The transceiver provides an average output power of −15 dBm over 0.3-0.31 THz, which is suitable for near-field imaging applications.

I. OVERCOMING THE LIMITATIONS OF PERFORMANCE PARAMETERS OF ON-CHIP ANTENNAS EMPLYOING THE MTS CONCEPT AND EM COUPLED FEED MECHANISM

A 130-nm logic CMOS-based 2 × 2 array of 280-GHz Schottky-barrier diode detectors with an antenna on-chip has realized in [91]. By employing poly-gate separation, the series resistance of the diode has been minimized, and a 2 THz cut-off frequency has achieved. An incident carrier with 100-Hz ~ 2-MHz amplitude modulation has been detected by each detector unit. The proposed antenna on-chip with a size of 255 × 250 μm^2 has picked up the radiated signals. As exhibited in Fig.21, the antenna is realized of the top aluminum layer. To stabilize the ground plane with dimensions of 450 × 450 μm^2 the metal layers 1 and 2 are shunted with each other. As a result, the electromagnetic-wave is reflected back to free space instead of propagating across the lossy silicon layer. The slots in Metal 1 cover the utilized Metal 2. The the antenna on-chip shows a simulated peak directivity and gain of 5.1 dBi and 1.6 dBi for efficiency

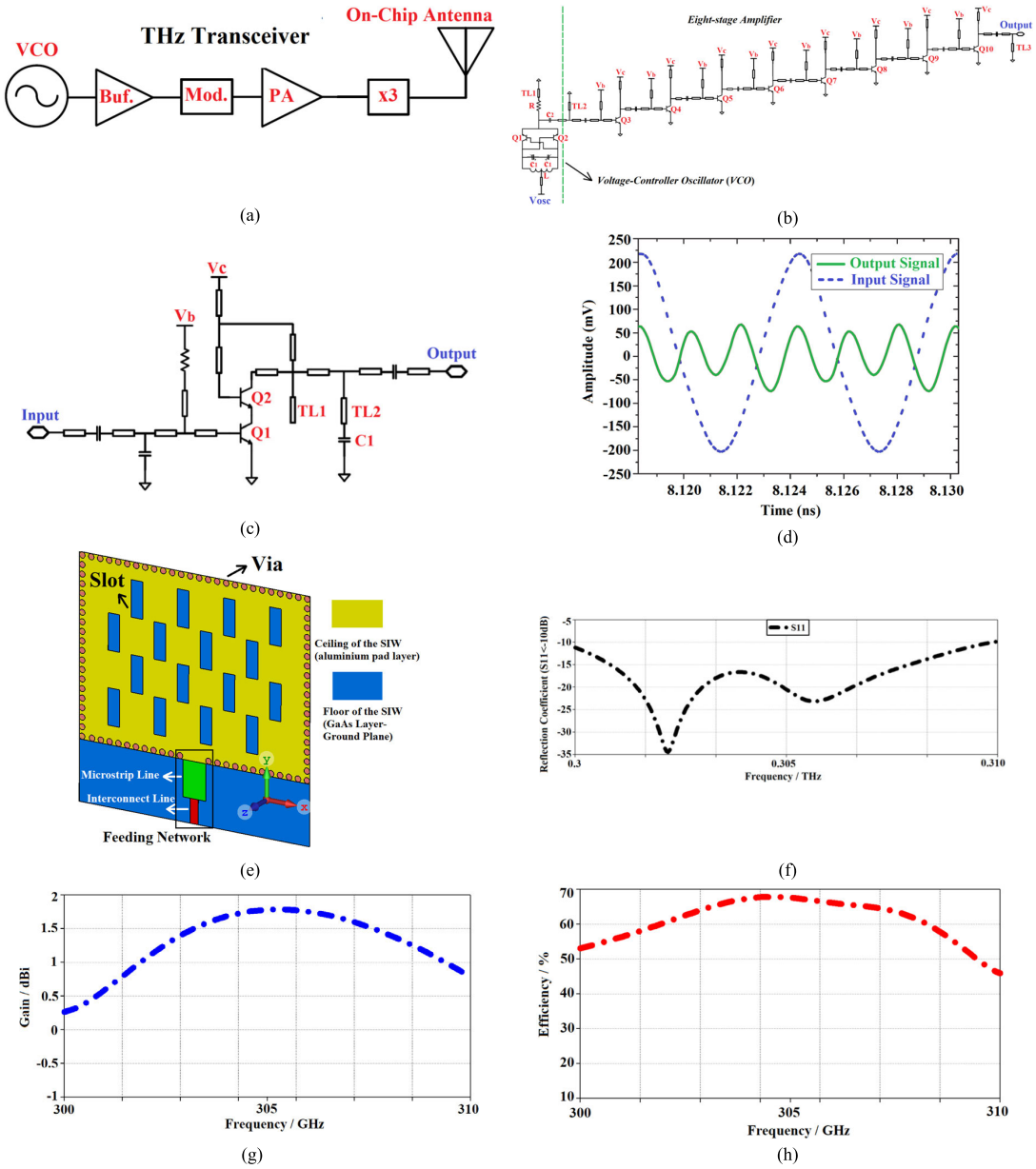

FIGURE 20. **(a) Schematic block diagram of the THz transceiver integrated with an on-chip antenna, (b) circuit diagram of the voltage-controller oscillator and the eight-stage amplifier, (c) circuit schematic of the frequency tripler, (d) simulated time-domain waveform of the frequency-tripler, (e) on-chip antenna based on SIW and MTM technologies, (f) reflection coefficient response, (g) gain response, and (h) radiation efficiency response [38].**

of 21%. The aperture size calculated from the directivity is 0.29 mm^2.

The results provided in [92] propose a wirelessly-locked 65nm CMOS-based 300 GHz 2 × 3 radiating source array as shown in Fig.22. To obtain a total radiated power (TRP) of +5.4dBm and effective isotropic radiated power (EIRP) of +22dBm with 5.1% radiated DC-to-THz efficiency the post-processing plated and partly diced trenches at the die backside have been applied. The attained radiated efficiency and power in the locked source, outperforms any previously reported work for integrated circuits (ICs) of any technology above 0.2 THz. The developed concept permits implementation of a two dimensional scalable terahertz source array at a low cost.

An 0.38–0.44 THz amplifier-multiplier-antenna array based on CMOS technology, capable of producing an EIRP of 3–4 dBm at 420 GHz has been proposed and demosntrated in [93]. The chip has contsructed appliying a 45-nm CMOS SOI process. To extract the power out of the chip, efficient non-chip antennas on-chip, shown in Fig.23, have been employed. The array combines efficient signal amplification and low-loss signal distribution at the W-band spectrum, along with a balanced quadrupler at each antenna. The amplifier–multiplier principle has proven by a 2 × 4 array. However, it can be scaled to any array size for additional EIRPs. It can also be scaled to 600–700 GHz by employing a 150–175 GHz amplifier–distribution network. Besides that,

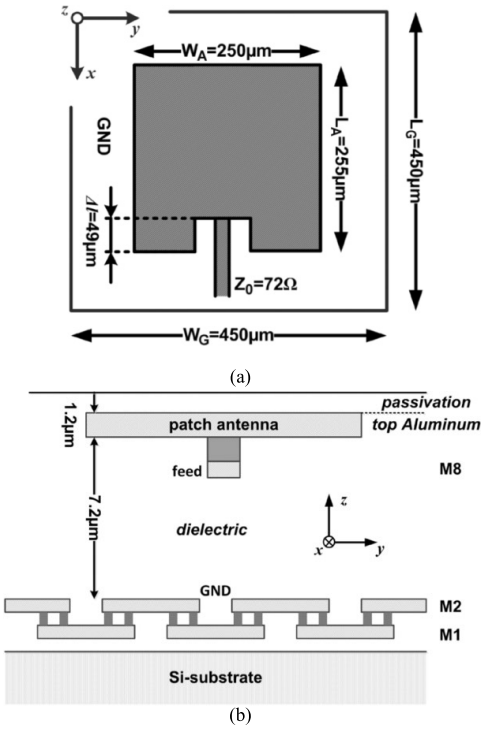

FIGURE 21. Antenna on-chip, (a) top-side and (b) cross section view [91].

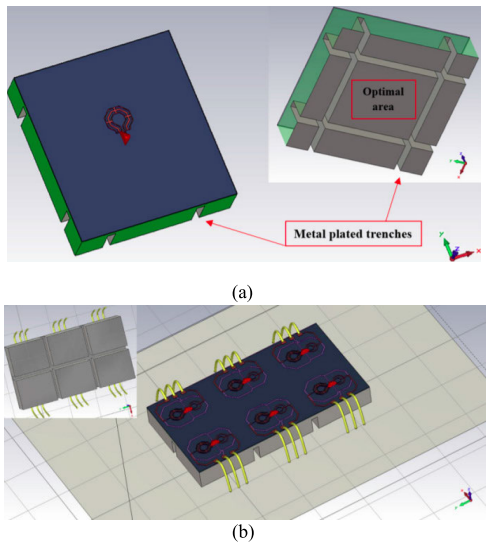

FIGURE 22. (a) 2 × 3 loop-antenna array layout, and (b) silicon area and metal plated trenches [92].

it is anticipated that this configuration can be utilized to create 1 THz radiation by applying the recent design on 250 GHz amplifiers in advanced SiGe processes.

A new solution to improve the performance parameters of the on-chip antenna fabricated on standard CMOS silicon (Si) technology is proposed in [39]. The antenna employs MTSs and excites the radiating elements through an EM coupled feed mechanism. The on-chip antenna, shown in Fig.24, is constructed using Si-GND-Si layers. The ground (GND) plane is sandwiched between two Si layers. The silicon and ground-plane layers have thicknesses of 20μm and 5μm, respectively. The 3 × 3 array consists of asterisk-shaped

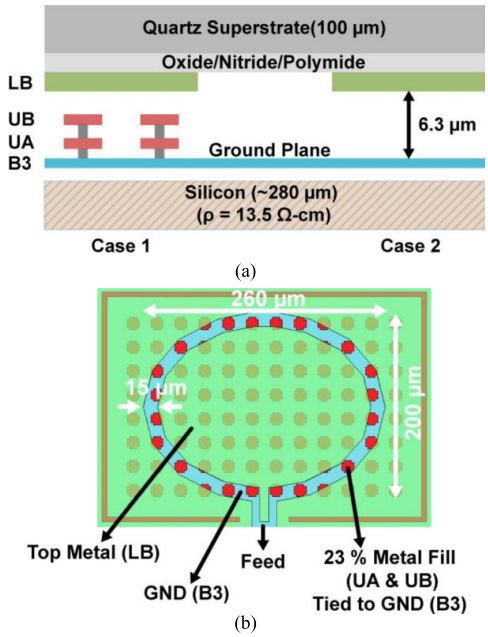

FIGURE 23. (a) Metal fill cases, and (b) antenna on-chip with metal-fill underneath the antenna [93].

radiating elements implemented on the top silicon layer. The resonator is transformed to a metasurface by embedding dielectric slots in it. By doing this, the effective aperture of the antenna is increased without affecting the dimensions of the antenna. The three slot lines in the ground-plane are located directly under the radiating elements. The radiating elements are excited through the slot-lines using an open-circuited microstrip-line constructed on the bottom silicon layer. The proposed feeding mechanism suppresses substrate losses and surface-waves, which improve the antenna's impedance matching and its impedance bandwidth. Moreover, the proposed technique overcomes the common drawbacks of narrow bandwidth and poor radiation specifications of on-chip antennas. The antenna exhibits a large impedance bandwidth of 60 GHz from 0.5THz to 0.56THz with an average gain and radiation efficiency of 4.58 dBi and 25.37%, respectively. The proposed structure has dimensions of 200 × 200 × 45μm^3. These results shows that the proposed technique is a potential candidate for THz system-on-chip.

In Table 6, the proposed work in [39] is compared to Refs. [91]–[93]. It is obsereved that using MTSs, the design process of the proposed on-chip antenna in [39] is simpler and more feasible than other reposted works in the table. Besides that, the on-chip antenna presented in [39] has more compact dimensions in a lower profile, compared to the reported works in Table 6. Furthermore, it also works over a much more higher frequency band above 500 GHz ans presents higher radiation gain than all the other antennas, except [92], which has a larger structure.

J. HIGH-PERFORMANCE 50μm SILICON-BASED ON-CHIP ANTENNA USING MTM AND SIW PRINCIPLES

A novel 50μm Silicon-based on-chip antenna in [40] combines MTM and SIW technologies. By combining the two

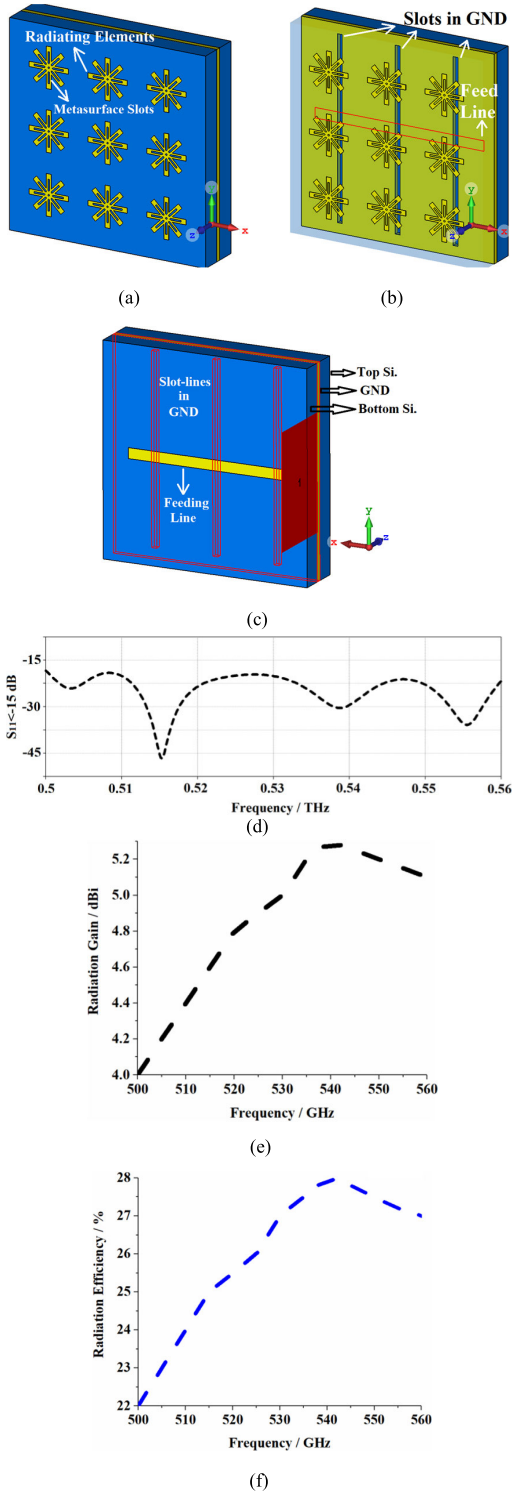

FIGURE 24. On-chip antenna configuration, (a) top view, (b) ground plane view as middle layer, (c) back view, (d) frequency bandwidth, (e) gain response, and (f) radiation efficeincy response [39].

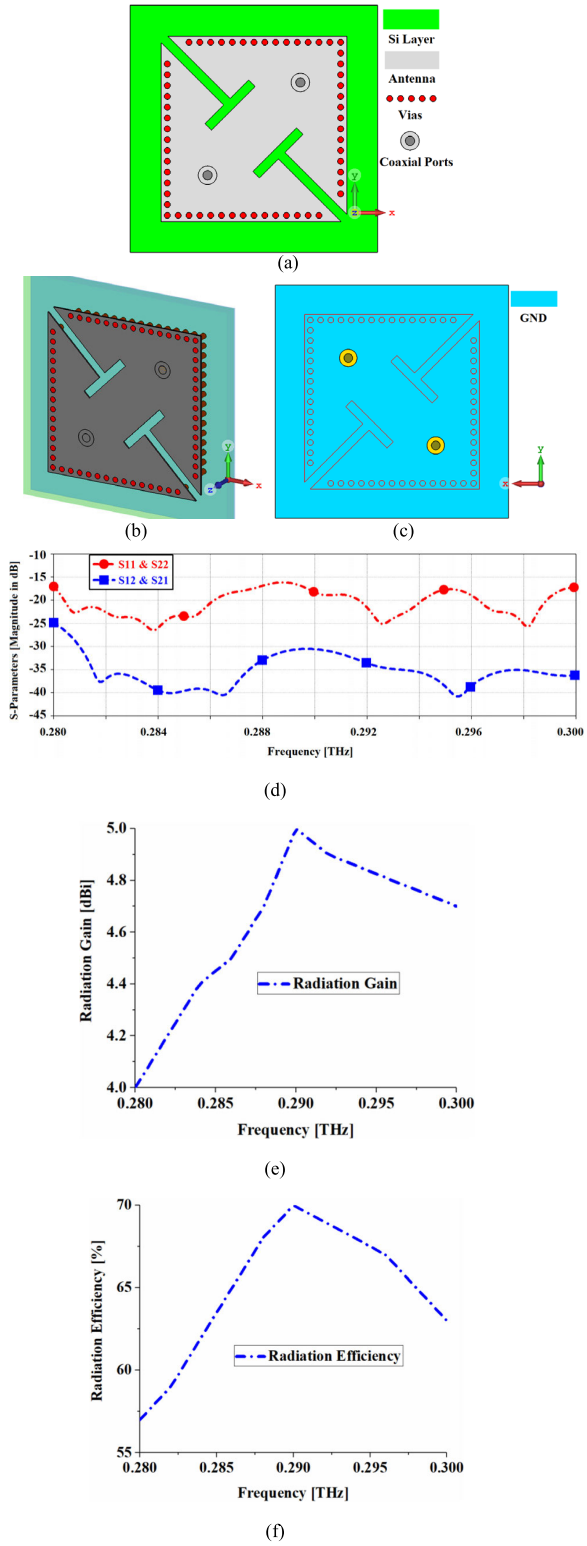

FIGURE 25. On-chip antenna layout based on MTM and SIW technologies, (a) top view, (b) isometric view, (c) back-side, (d) reflection and transmission coefficient responses, (e) gain response, and (f) radiation efficiency response [40].

technologies, its effective aperture area is increased and the losses due to surface waves and substrate are reduced. It is shown that this leads to an improved impedance matching, impedance bandwidth, port-to-port isolation, gain and radiation efficiency. The antenna structure, shown in Fig.25, comprises a square patch antenna implemented on a silicon substrate with a ground-plane. Embedded diagonally in the patch are two T-shaped slots and the edges of the patch is short-circuited to the ground-plane with metal vias, which

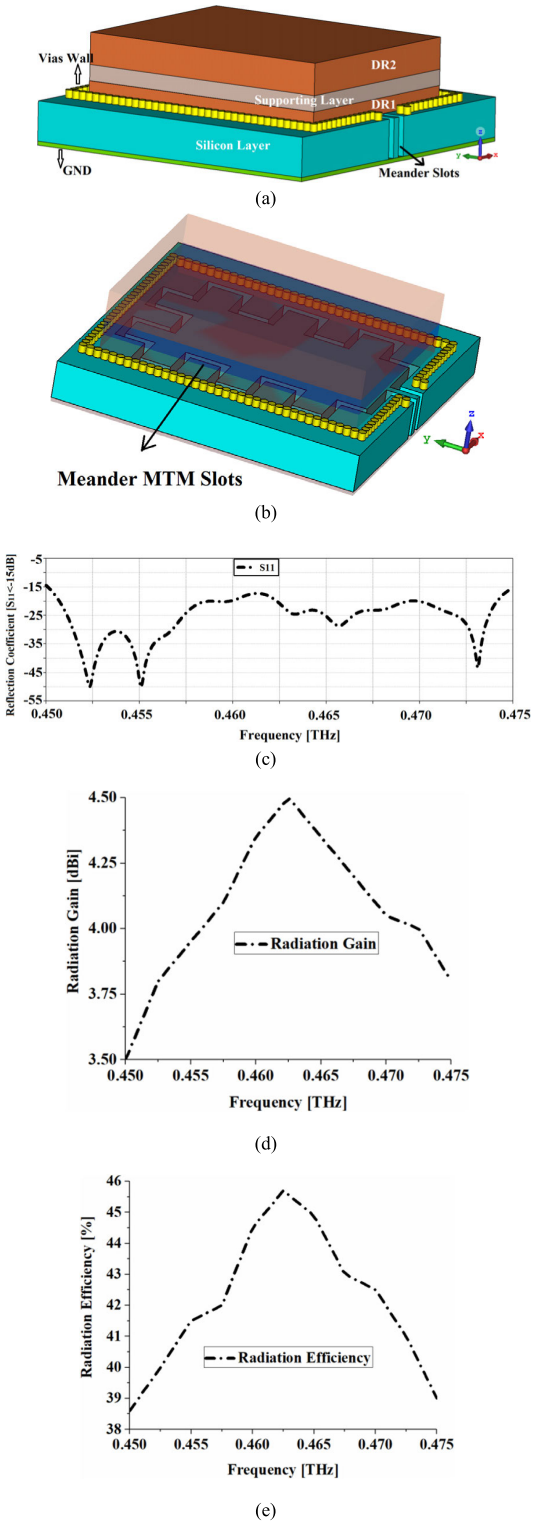

FIGURE 26. Series fed double DR on-chip antenna array based on MTM, (a) side view, (b) isometric view, (c) reflection coefficient response, (d) gain rrsponse, and (e) radiation efficiency response [41].

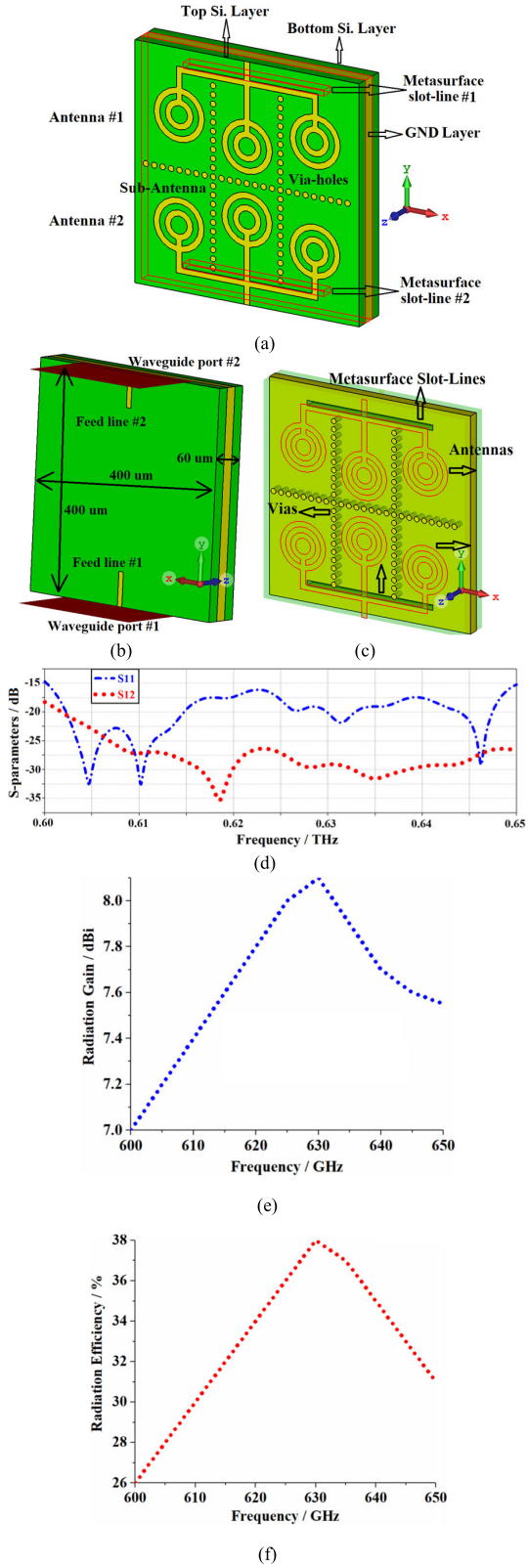

FIGURE 27. On-chip array antenna based on metasurface, (a) top layer, (b) bottom layer, (c) midle layer, (d) reflection and transmission coefficients, (e) gain response, and (f) radiation efficiency [42].

convert the structure into a substrate integrated waveguide. This structure reduces losses resulting from surface waves and silicon dielectric substrate. The modes in the structure can be excited through two coaxial ports connected to the patch from the underside of the silicon substrate. The proposed antenna structure is essentially transformed to exhibit MTM properties by realizing two T-shaped slots. This enlarges the

TABLE 6. State-of-the-art comparison of the the on-chip antennas.

Ref.	Antenna Type	Freq. (GHz)/ BW (%)	Gain (dBi)	Eff.%	Process	Size (mm^2)	Height (mm)
[91]	Patch	280/2.5	–1.6	21	0.13-μm CMOS	0.29	-
[92]	Loop Antenna Array	296/28	11.2	40	65-nm CMOS	2.22	0.23
[93]	Slot Ring with quartz Superstrate	420/10	1.6	35	45-nm SOI CMOS	0.05	-
[39]	Metasurface and EM coupled feed mechanism	540/11.3	5.3	28.15	CMOS	0.04	0.045

effective aperture area and significantly enhances its impedance bandwidth and radiation characteristics between 0.28 THz to 0.3 THz. It has an average gain and efficiency of 4.5dBi and 65%, respectively. In addition, it is a self-isolated structure with high isolation of better than 30 dB between the two ports. The on-chip antenna has dimensions of $800 \times 800 \times 60\ \mu m^3$.

K. MTM SILICON-BASED SERIES-FED DOUBLE DIELECTRIC RESONATOR ON-CHIP ANTENNA ARRAY

The antenna array in [41] is designed to operate over 0.450-0.475 THz. As shown in Fig.26, it comprises two dielectric resonators (DRs) that are stacked vertically on top of each other and placed on the surface of the slot antenna fabricated on a silicon substrate using standard CMOS technology. A meandering slot is created in the silicon substrate and the periphery of the silicon substrate is surrounded by a metallic via-wall to prevent energy dissipation, by suppressing the substrate loss and surface wave effects. The combination of slot and vias transform the antenna to a MTM structure that provides a relatively small antenna footprint. The antenna has dimensions of $400 \times 400 \times 135\ \mu m^3$. It has a maximum gain of 4.5 dBi and radiation efficiency of 45.7% at 0.4625 THz. The proposed series-fed double DRs on-chip antenna array is another candidate for application in THz integrated circuits.

L. HIGH PERFORMANCE MTS-BASED ON-CHIP ARRAY ANTENNA

CMOS 20μm silicon technology is used in [42] for fabrication of an innovative on-chip antenna array for 0.6-0.65 THz operation. The proposed array structure, shown in Fig.27, is constructed on three stacked layers composed of Silicon-metal-Silicon. The middle metal layer is a ground plane, which is sandwiched between two silicon layers. Implemented on the top layer are two antennas, which consist of three interconnected radiation elements. The radiation elements consist of interconnected dual rings that act like a MTS. This arrangement is shown to increase the effective aperture area of the array. Metallic via-holes have been inserted through the three layers and implemented between the radiation elements to mitigate surface waves and reduce substrate losses. The antenna is excited using open-circuited microstrip lines located on the back side of the structure. The EM-energy is coupled from the bottom layer to the radiating elements on the top-layer through the slots created in the ground-plane layer. The antenna array has dimensions of $0.4 \times 0.4 \times 0.06\ mm^3$. The results in Fig.27 show that the proposed on-chip antenna array has an average radiation gain, efficiency, and isolation of 7.62 dBi, 32.67%, and −30 dB, respectively. These results support the viability of the antenna array for THz integrated circuits.

III. CONCLUSION

This paper presented thorough survey on antennas for on-chip integration for operation at mmWave and THz bands. These bands are envisioned to provide unprecedented performance improvement in terms of data rates in the Terabit-per-second regime, and inherently supporting applications that combine extreme data rates with agility, reliability, zero response time and artificial intelligence. Antennas are one of the key components to enable wireless communications. Wireless systems operating at such bands will have stringent requirements that cannot be fulfilled by traditional off-chip antenna technology. The only viable solution is instead to use on-chip antennas. Typically, on-chip antennas are handicapped by narrow bandwidth (less than 10%) and low radiation efficiency. Hence, innovative on-chip antennas have been described in this survey, which employ technologies such as metamaterials, metasurfaces and substrate integrated waveguides to improve the frequency bandwidth and radiation properties with keeping constant the physical dimensions. It is shown that all three technologies can enhance the effective aperture of on-chip antennas, suppress surface waves and reduce substrate losses, that degrade the performance of such antennas. Therefore, the proposed antennas on-chip realized employing the above methodologies show substantially improved impedance match, operating frequency band, and radiation specifications compared to previously used technologies. These aspects make such antennas a prime nominate for mmWave and THz on-chip integration. This survey presents a perfect reference source for specialist antenna designers.

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