IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received December 10, 2019, accepted December 22, 2019, date of publication January 3, 2020, date of current version January 15, 2020.

Digital Object Identifier 10.1109/ACCESS.2019.2963743

A New Concept of PWM Duty Cycle Computation Using the Barycentric Coordinates in a Three–Dimensional Voltage Vectors Arrangement

PAWEŁ SZCZEPANKOWSKI[1], (Member, IEEE), NIKOLAI POLIAKOV[2], DENIS VERTEGEL[2], KRZYSZTOF JAKUB SZWARC[1], AND RYSZARD STRZELECKI[1], (Senior Member, IEEE)

[1]Faculty of Electrical and Control Engineering, Gdańsk University of Technology, 80-233 Gdańsk, Poland
[2]Faculty of Control Engineering and Robotics, ITMO University, 191002 Saint Petersburg, Russia

Corresponding author: Pawel Szczepankowski (pawel.szczepankowski@pg.edu.pl)

This work was supported in part by the LINTE^2 Laboratory, Gdansk University of Technology, Grant DS 033784, and in part by the Government of the Russian Federation under Grant 08-08.

ABSTRACT The paper presents a novel approach to the Pulse Width Modulation (PWM) duty cycle computing for complex or irregular voltage vector arrangements in the two (2D) and three–dimensional (3D) Cartesian coordinate systems. The given vectors arrangement can be built using at least three vectors or collections with variable number of involved vectors (i.e. virtual vectors). Graphically, these vectors form a convex figure, in particular, a triangle or a tetrahedron. The reference voltage vector position inside that figure can be expressed by the *barycentric coordinates*, which are calculated using the second (2D case) or the third–degree determinant (3D case) – without trigonometry and angles. Thus, the speed of the PWM duty cycle computation rises significantly. The use of the triangle area or the tetrahedron volume, instead of the standard vector projection also permits for a well–defined and universal approach to identifying the reference vector position, especially for converters with complex and/or deformed space–vector diagrams (i.e. floating DC–link, multisource DC–link). The proposed computation scheme is based on simple instructions without trigonometry thereby, the DSP processor, or digital solution for field–programmable gate array, can fast–perform this operation using atomic operations. The aim of the presented considerations is not a novel PWM modulation, but a computable idea of a general calculation scheme for cases in which the distribution of vectors is non-trivial. A detailed algebraic and geometric analysis, as well as mathematical proofs on the total consistency of the results with the standard projection method, are also included. Subsequently, the Three–Dimensional Space Vector Modulation (3D–SVM), is considered as a special background to present a novel approach.

INDEX TERMS 3D–SVM, duty cycle calculation, nonlinear loads, space vector, pulse width modulation, 3–level 4–leg inverter.

I. INTRODUCTION

The development of industrial power electronic applications is currently associated with multilevel inverters [1]–[5]. It results from the need for quality of formed voltages, currents and EMI, as well as the necessity to work with multiple sources and higher voltages. To meet these requirements Voltage Source Inverters (VSI) topologies, become more complex with the increasing number of voltage levels and inverter legs. Growing complexity of VSI topologies entails a significant increase in the complexity of Pulse Width Modulation (PWM) methods suitable for these inverters. This paper addresses the above problem by proposing an effective 3D–SVM computing algorithm based on *barycentric coordinates* [6] for 3–level 4–leg diode-clamped VSI. The proposed algorithm can be applied for 4–wire 3–phase applications such as DSTATCOM, multi-source Hybrid Energy Storage Systems, Active Power Filter [4], [7]–[13], local small power PV generation plant, uninterruptible power supply of various factories, offices, residential houses, etc.

The associate editor coordinating the review of this manuscript and approving it for publication was Zhilei Yao.

According to the simple modulation algorithms, several references propose transformations of the space–vector diagrams from the Cartesian (or $\alpha\beta$) coordinates to other frames. The *gh* [14], the 60° [15], *mn* coordinates [16] or $\alpha'\beta'$ coordinate system proposed in [17] are attempts to simplifying the modulation algorithm. However, all of them relies on balanced DC–link voltages. Moreover, none of the mentioned space–vector diagram transformations are applicable to 4–wire, 4–legs inverters. Analysis and comparison of the mentioned transformation methods with *barycentric coordinates* for 3–wire system can be found in [6]. One of the few attempts (applicable for 4–wire systems) to compute the duty cycles of the actual (i.e. non–ideal) component vectors for the three-level NPC inverter was presented in [18]. The authors proposed an extension of the *gh* frame method of [14] to include accurate duty cycle calculations under the DC–link imbalance. The idea, called the *method of projections*, is quite complex and is derived after a complex analysis of geometric relationships between the basic vectors displaced by the DC–link voltage imbalance. The approach is hardly extendable to other cases, for instance, a different type of component vectors (e.g. virtual vectors) or different inverter topologies (e.g. 4–leg inverters or inverters with more than 3 levels).

A more universal method was proposed in [19]. The calculations of duty cycles are performed in a frame called *abc* coordinates. This frame is made of three axes – *a*, *b* and *c* – corresponding to the respective three phases of the inverter, but forming a three–dimensional orthogonal system rather than the standard planar system with the *abc* axes rotated by multiples of $2\pi/3$. It permits for quite simple representation of DC–link voltage imbalance and computation of duty cycles under imbalance. The method can be used for multilevel 3–leg and 4–leg inverters however, considering DC–link voltages imbalance requires an additional transformation of coordinates and allows to synthesize voltage only in a three–phase system according to its orthogonal nature.

This paper also proposes a computational approach supporting explicit space–vector PWM computations for multilevel inverters with possible DC–link voltage imbalance. The key idea in the proposed arithmetic is the use of *barycentric coordinates* for the duty cycle computations and the selection of the modulation triangle/tetrahedron (2D/3D). Unlike the method of [19], which uses a special coordinate frame, the proposed method is applied directly to space–vector diagrams in the natural Cartesian coordinates ($\alpha\beta$) and can be implemented to multiphase systems. The method can be applied to all types of multilevel inverters.

To achieve a better understanding of the proposed concept, the discussion was divided into smaller sections. The new general computation formula for two–dimensional space is presented in detail in Section I. The next section contains analogous considerations for the three–dimensional coordinates system. Section III contains a brief introduction the used 3D–SVM modulation and *barycentric coordinates* in the modulation algorithm. Proposed modulation algorithm is based on [20] but developed by balancing DC–link voltages [21]–[24], accurate generation of output voltages regardless of unbalanced capacitor voltages [18], [19], fast duty cycles calculations algorithm based on *barycentric coordinates* [6] and optimal switching state sequence. Experimental results are introduced in Section IV to validate the effectiveness of the proposed duty cycle computation. The article closes with a summary and a brief discussion on the experimental results.

II. PWM DUTY CYCLES COMPUTATION IN A TWO–DIMENSIONAL COORDINATE SPACE

Let $[\vec{w}_1, \vec{w}_2, \vec{w}_3]$ denote a three–element vector collection in the two–dimensional Cartesian *xy* coordinate system shown in Fig. 1(a). Coordinates of these independent vectors meet the following equation

$$\alpha_1 \cdot \vec{w}_1 + \alpha_2 \cdot \vec{w}_2 + \alpha_3 \cdot \vec{w}_3 = \vec{e} \tag{1}$$

where α_1, α_2 and α_3 are real numbers for scaling the length of the corresponding vector. The value of scaling coefficients from (1) can be obtained by constructing a graphic solution. However, it is not a suitable form for implementation in the Digital Control System (DCS). In order to formulate a more practical solution, the vectors arrangement in Fig. 1(a), can be transformed into a new equivalent collection represented by $\vec{v}_1$, $\vec{v}_2$, $\vec{u}$ vectors in a local *pq* reference frame, as shown in Fig. 1(b). Thus, updated coordinates can be calculated using the following formula

$$\begin{aligned} \vec{w}_2 - \vec{w}_3 &= \vec{v}_2 \\ \vec{w}_1 - \vec{w}_3 &= \vec{v}_1 \\ \vec{e} - \vec{w}_3 &= \vec{u} \end{aligned} \tag{2}$$

Note that, all vectors in (2) are obtained by subtracting $\vec{w}_3$ from the other vectors and the reference vector $\vec{u}$ can be represented in a similar way to (1) by

$$\vec{u} = d_1 \cdot \vec{v}_1 + d_2 \cdot \vec{v}_2 \tag{3}$$

where $d_1 = |\vec{u}_1| / |\vec{v}_1|$ and $d_2 = |\vec{u}_2| / |\vec{v}_2|$ are non-negative scaling coefficients referred as PWM duty cycles (PWMDC). The d_1 and d_2 can be obtained using the vector projection

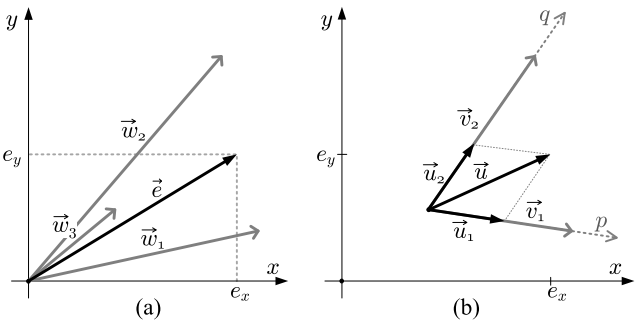


FIGURE 1. Replacement of the Cartesian *xy* coordinate reference frame (a) into local *pq* frame (b).

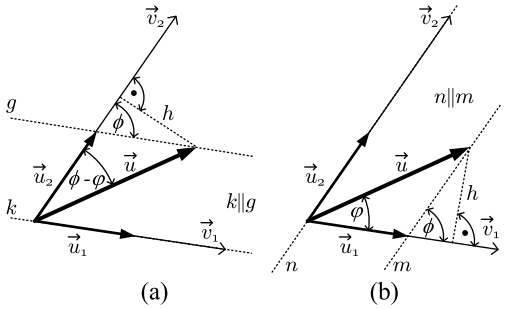


FIGURE 2. Reference vector $\vec{u}$ projection: (a) on the base vactor $\vec{v}_2$ (b) on the base vactor $\vec{v}_1$.

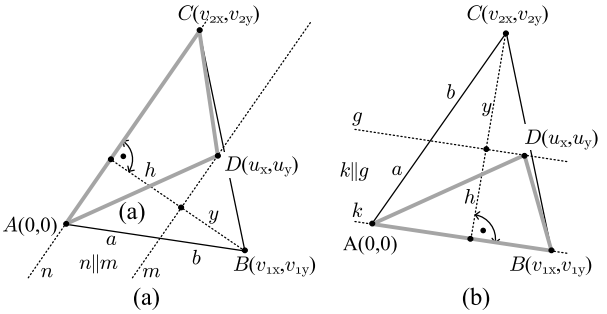


FIGURE 3. Collections of points in *xy* coordinate reference frame correspond to: (a) triangle $\Delta(A, D, C)$, (b) triangle $\Delta(A, D, B)$.

principle, which is ilustrated in Fig. 2. Using expressions on the sine of angles ϕ and φ and based on the h segment

$$\frac{h}{|\vec{u}_1|} = \sin(\phi), \quad \frac{h}{|\vec{u}|} = \sin(\phi - \varphi) \tag{4}$$

formally obtain

$$|\vec{u}_1| = |\vec{u}| \cdot \frac{\sin(\phi - \varphi)}{\sin(\phi)}, \quad |\vec{u}_2| = |\vec{u}| \cdot \frac{\sin(\varphi)}{\sin(\phi)} \tag{5}$$

To eliminate trigonometric expressions sin containing angles ϕ and φ,the formula of vectors cosine is applied

$$\begin{aligned} \cos(\phi) &= \frac{\vec{v}_1 \circ \vec{v}_2}{|\vec{v}_1| \cdot |\vec{v}_2|} \\ \cos(\varphi) &= \frac{\vec{v}_1 \circ \vec{u}}{|\vec{v}_1| \cdot |\vec{u}|} \\ \cos(\phi - \varphi) &= \frac{\vec{v}_2 \circ \vec{u}}{|\vec{v}_2| \cdot |\vec{u}|} \end{aligned} \tag{6}$$

and also Pythagorean identity formula, which leads to the following equations

$$d_1 = \frac{|\vec{u}|}{|\vec{v}_1|}\sqrt{\frac{1-\cos^2(\phi-\varphi)}{1-\cos^2(\phi)}} = \frac{|\vec{u}|}{|\vec{v}_1|}\sqrt{\frac{1-\left(\frac{\vec{v}_2 \circ \vec{u}}{|\vec{v}_2|\cdot|\vec{u}|}\right)^2}{1-\left(\frac{\vec{v}_1 \circ \vec{v}_2}{|\vec{v}_1|\cdot|\vec{v}_2|}\right)^2}} \tag{7}$$

$$d_2 = \frac{|\vec{u}|}{|\vec{v}_2|}\sqrt{\frac{1-\cos^2(\varphi)}{1-\cos^2(\phi)}} = \frac{|\vec{u}|}{|\vec{v}_2|}\sqrt{\frac{1-\left(\frac{\vec{v}_1 \circ \vec{u}}{|\vec{v}_1|\cdot|\vec{u}|}\right)^2}{1-\left(\frac{\vec{v}_1 \circ \vec{v}_2}{|\vec{v}_1|\cdot|\vec{v}_2|}\right)^2}} \tag{8}$$

where the mark ($\circ$) designates the scalar product of two vectors. Both equations (7) and (8) are not satisfying and further optimization can be perform. Despite the elimination of trigonometric functions, they contain the square root operation. In order to obtain a simpler expression for d_1 and d_2, vectors shown in Fig. 2, can be represented as a collection of points A, B, C, and D as illustrated in Fig. 3. Based on the Thales' theorem, d_1 as the ratio of the length of the segment a to the sum of segments a and b in Fig. 3(a),

$$d_1 = \frac{|\vec{u}_1|}{|\vec{v}_1|} = \frac{a}{a+b} = \frac{h}{h+y} \tag{9}$$

and analogically for the case ilustrated in Fig. 3(b).

$$d_2 = \frac{|\vec{u}_2|}{|\vec{v}_2|} = \frac{a}{a+b} = \frac{h}{h+y} \tag{10}$$

As can be seen in Fig. 3(a), triangles $\Delta(A, D, C)$ and $\Delta(A, B, C)$ have the same base length. Thus, d_1 and d_2 can be expressed as ratio of triangle areas

$$d_1 = \frac{\Delta_{ADC}}{\Delta_{ABC}}, \quad d_2 = \frac{\Delta_{ADB}}{\Delta_{ABC}} \tag{11}$$

If vertex A is located at the origin $(0, 0)$ of a Cartesian coordinate system and the remaining vertices are represented by point $B(v_{1x}, v_{1y})$, $C(v_{2x}, v_{2y})$ and $D(u_x, u_y)$, the area of each required triangle can be computed as the absolute value of the determinant. Thus, the PWM duty cycle for vector $\vec{v}_1$ can be written as

$$d_1 = \left|\frac{\det\begin{bmatrix} D_x & D_y \\ C_x & C_y \end{bmatrix}}{\det\begin{bmatrix} B_x & B_y \\ C_x & C_y \end{bmatrix}}\right| = \left|\frac{\det\begin{bmatrix} u_x & u_y \\ v_{2x} & v_{2y} \end{bmatrix}}{\det\begin{bmatrix} v_{1x} & v_{1y} \\ v_{2x} & v_{2y} \end{bmatrix}}\right| \tag{12}$$

and identically for vector $\vec{v}_2$

$$d_2 = \left|\frac{\det\begin{bmatrix} D_x & D_y \\ B_x & B_y \end{bmatrix}}{\det\begin{bmatrix} B_x & B_y \\ C_x & C_y \end{bmatrix}}\right| = \left|\frac{\det\begin{bmatrix} u_x & u_y \\ v_{1x} & v_{1y} \end{bmatrix}}{\det\begin{bmatrix} v_{1x} & v_{1y} \\ v_{2x} & v_{2y} \end{bmatrix}}\right| \tag{13}$$

The PWMDC for zero vector, which corresponds with point $A(0, 0)$ in Fig. 3, is equal to

$$d_0 = \frac{\Delta_{BCD}}{\Delta_{ABC}} \tag{14}$$

The sum of all PWMDC, computed for each triangle $\Delta(A, B, C)$ vertex, is equal to unity

$$d_1 + d_2 + d_0 = 1 \tag{15}$$

As pointed out, vectors' geometric arrangement depicted in Fig.2, has been transformed into the local triangular area, in which the reference vector $\vec{u}$ resides. Secondly, the PWMDC have been calculated using a simple rational function based on the triangle area, which can be fast computed using the absolute value of determinants. As is evident

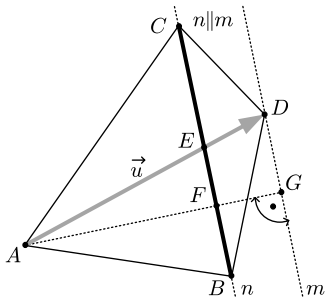


FIGURE 4. Rescaling the length of vector $\vec{u}$.

from the presented elaboration, only vectors coordinates are only needed. The proposed calculation scheme is widely used in mechanics problem solving and has been successfully adopted in the following paper for the unification of the PWMDC computation [25]. Graphically, all three selected vectors form a convex figure – the triangle – and the reference voltage vector position inside that figure can be expressed by *barycentric coordinates*, which are just calculated using (12)–(14).

If the sum (15) is greater then unity, as it is shown in Fig. 4, it means that point D lies outside the triangle $\Delta(A, B, C)$ and the length of the reference vector $\vec{u}$ must be rescaled by factor ζ which can be expressed as follows

$$\zeta = \frac{|AE|}{|AD|} = \frac{|AE|}{|AE| + |ED|} \tag{16}$$

Note, that lines m and n in Fig. 4 are parallel, and therefore, by the theorem of Tales and previous consideration, the ζ factor can be calculated based on the following equation,

$$\zeta = \frac{|AF|}{|AF| + |FG|} = \frac{\Delta_{\mathrm{ABC}}}{\Delta_{\mathrm{ABC}} + \Delta_{\mathrm{BCD}}} \tag{17}$$

which can be easily implemented in PWM overmodulation algorithms. The proposed approach has a very useful additional property that their sum equals unity if it is computed for a point inside a triangle (as in Fig. 3), but it is greater than unity if the point lies outside the element (as illustrated in Fig. 4). This is a uniform and effective method to find the traingle in which the reference vector resides. In practice, due to floating-point numbers limited accuracy, the smallest sum (15), ideally equal to unity, is selected as a minimal element using optimized and fast DSP function.

The proposed approach based on geometrical relations, represented by (12) and (13), can be proved algebraically using the formula interpretation of the absolute value of a vector product as follows

$$d_1 = \frac{|\vec{u}|\,|\vec{v}_2| \cdot \sin(\phi - \varphi)}{|\vec{v}_1|\,|\vec{v}_2| \cdot \sin(\phi)} = \frac{|\vec{u} \times \vec{v}_2|}{|\vec{v}_1 \times \vec{v}_2|} = \frac{\Delta_{ADC}}{\Delta_{ABC}} \tag{18}$$

$$d_2 = \frac{|\vec{u}|\,|\vec{v}_1| \cdot \sin(\varphi)}{|\vec{v}_1|\,|\vec{v}_2| \cdot \sin(\phi)} = \frac{|\vec{u} \times \vec{v}_1|}{|\vec{v}_1 \times \vec{v}_2|} = \frac{\Delta_{ADB}}{\Delta_{ABC}} \tag{19}$$

The proposed computing time of a routine based on the *barycentric coordinates* was compared with the time used by a routine based on the trigonometric functions and classified

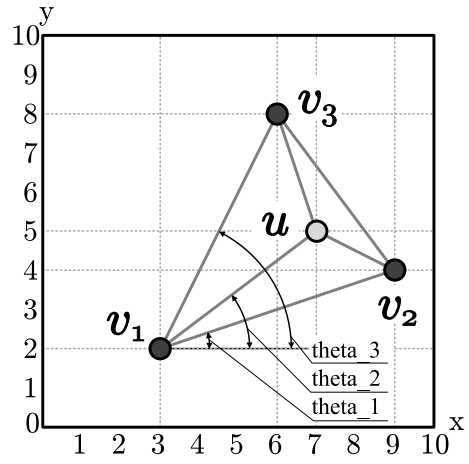


FIGURE 5. Illustration of the case considered in the benchmark code.

TABLE 1. Comparison conditions.

parameter	description
processor type	DSP Texas Instruments
model	TMS320C6672
clock	1GHz
format of numbers	single precision IEEE 754
library of trigonometric functions	dedicated DSP Math Library for Floating Point Devices
compiler optimization level (Code Composer Studio 8.0)	O–2
DSP core usage	computations performed by CORE1 only

TABLE 2. Comparison results.

parameter	description
duty cycle d1_trig	0.5
duty cycle d2_trig	0.333
duty cycle d1_new	0.5
duty cycle d2_new	0.333
total DSP cycles for the method of projections	859 (program code line 57–71)
total DSP cycles for the proposed method	61 (program code line 84–89)

as the *method of projections* described in [18]. The DSP processor code used in the comparison, which correspondes to illustration in Fig. 5, is shown in Listing 1. The comparison conditions are specified in Table 1, while the comparison results are presented in Table 2.

As might be seen, the proposed arithmetic is more than tentimes faster than the conventional approach. The rationality behind applying *barycentric coordinates* to calculate PWMDC is that it quickly performs the forward analysis of the effects associated with the given set of selected base vectors in the reference voltage synthesis with small computing

```
int i;
/* code execution measurement */
unsigned int t3_barycentric;
unsigned int t3_projection;
unsigned int t1,t2; //start,stop
/* vertices shown in Fig.17 */
const float v1[2]={3.0f,2.0f};
const float v2[2]={9.0f,4.0f};
const float v3[2]={6.0f,8.0f};
/* reference vector shown in Fig.17 */
const float vref[2]={7.0f,5.0f};
/* local vectors shown in Fig.17 */
float u[2];  //reference vector
float u1[2]; //first base vector
float u2[2]; //second base vector
/* required angles shown in Fig.17 */
float theta_2;
float theta_1;
float theta_3;
/* angles between vectors u, u1, u2 */
float theta;
float phi;
/* required vector lengths */
float mod_u; //vector u length
float mod_u1; //vector u1 length
float mod_u2; //vector u2 length
/* temporary variable = 1.0f/sin() */
float invsin;
/* PWM duty cycle for active vectors u1
    and u2 in projection method*/
float d1_trig,d2_trig;
/* PWM duty cycle for active vectors u1
    and u2 for proposed method */
float d1_new,d2_new;
/* value of trinagle area*/
float area;  //points: v1--v2--v3
float area1; //points: v1--vref--v3
float area2; //points: v1--v2--vref
/* temporary variable = 1.0f/area */
float inv_area;

//====================================
// collection of linearly independent
// vectors - this is common part
// of both method
//====================================
u[0]=vref[0]-v1[0];  u[1]=vref[1]-v1[1];
u1[0]=v2[0]-v1[0];  u1[1]=v2[1]-v1[1];
u2[0]=v3[0]-v1[0];  u2[1]=v3[1]-v1[1];

//====================================
// standard projection approach
// for non-equilateral triangle case
//====================================

/* time measurement: start */
t1=Timestamp_get32();
//calc angles (see Fig.17)
theta_2=atan2sp(u[1],u[0]);
theta_1=atan2sp(u1[1],u1[0]);
theta_3=atan2sp(u2[1],u2[0]);
theta=theta_3-theta_1;
```

Listing 1. DSP processor code used for comparision.

```
phi=theta_2-theta_1;
//calc modules (see Fig.17)
mod_u=sqrtsp(u[0]*u[0]+u[1]*u[1]);
mod_u1=sqrtsp(u1[0]*u1[0]+u1[1]*u1[1]);
mod_u2=sqrtsp(u2[0]*u2[0]+u2[1]*u2[1]);
//calc PWM duty cycles for u1 and u2
    vector
invsin=recipsp(sinsp(theta));
d1_trig=(mod_u*recipsp(mod_u1));
d1_trig*=(sinsp(theta-phi)*invsin);
d2_trig=(mod_u*recipsp(mod_u2));
d2_trig*=(sinsp(phi)*invsin);
/* time measurement: stop */
t2=Timestamp_get32();
t3_projection=t2-t1;

//====================================
// proposed barycentric approach
// for non-equilateral triangle case
//====================================

/* time measurement: start */
t1=Timestamp_get32();
//equation (2)
area=u1[0]*u2[1] - u1[1]*u2[0];
inv_area=recipsp(area);
area1=u2[1]*u[0] - u2[0]*u[1];
area2=u1[0]*u[1] - u1[1]*u[0];
d1_new=fabsf(area1*inv_area);
d2_new=fabsf(area2*inv_area);
/* time measurement: stop */
t2=Timestamp_get32();
t3_barycentric=t2-t1;
```

Listing 1. *(Continued.)* DSP processor code used for comparision.

overhead. The presented approach can be extended to the three–dimensional space divided into irregular tetrahedrons. The word 'irregular' has been used to emphasize the impact of DC voltage asymmetry in multi–level inverters on the actual output voltage of the NPC converter.

III. PWM DUTY CYCLES COMPUTATION IN A THREE–DIMENSIONAL COORDINATE SPACE

It is assumed that the vector $\vec{p}$ in Fig. 6, is located inside the tetrahedron V with vertices A, B, C, and D. The reference vector $\vec{p}$ can be expressed as the following sum

$$\vec{p} = \vec{u} + \vec{v} + \vec{w} \tag{20}$$

where the vectors $\vec{u}$, $\vec{v}$, and $\vec{w}$ are the effect of a reference vector $\vec{p}$ projection on the base vectors $\overrightarrow{AB}$, $\overrightarrow{AC}$, and $\overrightarrow{AD}$ respectively

$$\vec{p} = d_B \cdot \overrightarrow{AB} + d_C \cdot \overrightarrow{AC} + d_D \cdot \overrightarrow{AD} \tag{21}$$

The PWMDC from (21) can be written as ratio of appropriate lengths

$$d_B = \frac{|\vec{u}|}{\left|\overrightarrow{AB}\right|}, \quad d_C = \frac{|\vec{v}|}{\left|\overrightarrow{AC}\right|}, \; d_D = \frac{|\vec{w}|}{\left|\overrightarrow{AD}\right|}. \tag{22}$$

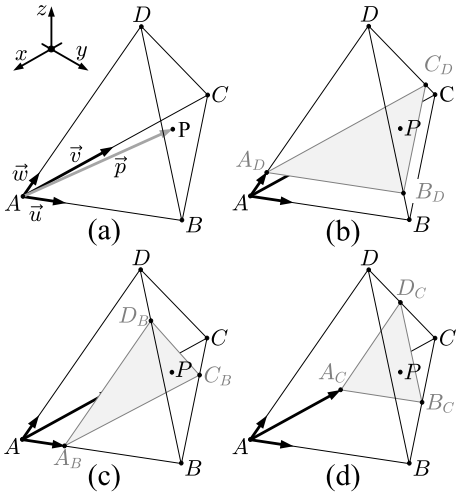


FIGURE 6. The three-dimensional case: (a) reference vector $\vec{p}$ and base vectors $\vec{u}$, $\vec{v}$, $\vec{w}$, (b), (c), and (d) triangular surfice parallel to the corresponding sides of the tetrahedron $V(A, B, C, D)$.

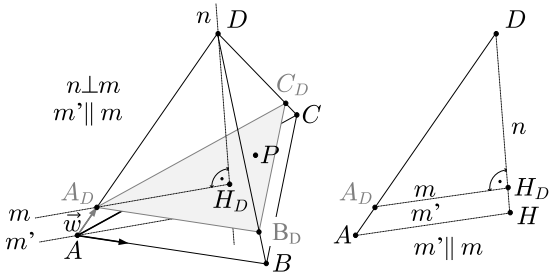


FIGURE 7. Geometric layout for the Thales Theorem application for the case illustrated by Fig. 6(b).

To find a more practical form of (22), the case illustrated in Fig. 6(b) and more detailed in Fig. 7 is considered. The triangle $\Delta(A_D, B_D, C_D)$, which contains a point P (the end of reference vector $\vec{p}$), is parallel to the base of tetrahedron $V(A, B, C, D)$, which is the triangle $\Delta(A, B, C)$. Moreover, the line n is passing through the vertex D and is normal to the surfaces represented by triangles $\Delta(A, B, C)$ and $\Delta(A_D, B_D, C_D)$. Based on the geometric layout in Fig. 7, the PWMDC for vector $\vec{w}$ can be finally described by the following formula

$$d_D = \frac{|\vec{w}|}{\left|\overrightarrow{AD}\right|} = \frac{|AA_D|}{|AD|} = \frac{|HH_D|}{|HD|} \tag{23}$$

Considering that both tetrahedrons $V(A, B, C, D)$ and $V(A, B, C, P)$ have the same base triangle $\Delta(A, B, C)$, the duty cycle d_D can be expressed in *barycentric coordinates* as the ratio of the volume of these figures

$$d_D = \frac{V_{ABCP}}{V_{ABCD}} \tag{24}$$

Analogous results can be obtained with respect to the other verticles

$$d_A = \frac{V_{ABCP}}{V_{ABCD}}, \quad d_B = \frac{V_{ADCP}}{V_{ABCD}}, \; d_C = \frac{V_{ABDP}}{V_{ABCD}} \tag{25}$$

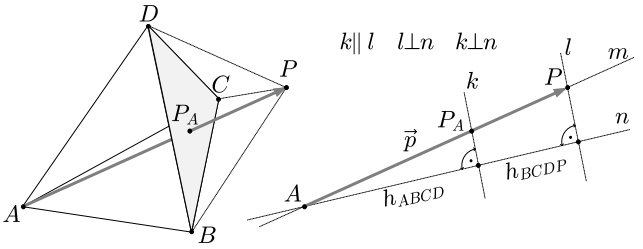


FIGURE 8. Point P is located outside the tetrahedron $V(A, B, C, D)$.

Tetrahedron volume can be represented in *barycentric coordinates* as a ratio of absolute values of determinants. Thus, finally the PWMDC can be expressed as follows

$$d_A = \left| \det \begin{bmatrix} P_x - B_x & P_y - B_y & P_z - B_z \\ P_x - C_x & P_y - C_y & P_z - C_z \\ P_x - D_x & P_y - D_y & P_z - D_z \end{bmatrix} \cdot g \right| \tag{26}$$

$$d_B = \left| \det \begin{bmatrix} P_x - C_x & P_y - C_y & P_z - C_z \\ P_x - D_x & P_y - D_y & P_z - D_z \\ P_x - A_x & P_y - A_y & P_z - A_z \end{bmatrix} \cdot g \right| \tag{27}$$

$$d_C = \left| \det \begin{bmatrix} P_x - D_x & P_y - D_y & P_z - D_z \\ P_x - A_x & P_y - A_y & P_z - A_z \\ P_x - B_x & P_y - B_y & P_z - B_z \end{bmatrix} \cdot g \right| \tag{28}$$

$$d_D = \left| \det \begin{bmatrix} P_x - A_x & P_y - A_y & P_z - A_z \\ P_x - B_x & P_y - B_y & P_z - B_z \\ P_x - C_x & P_y - C_y & P_z - C_z \end{bmatrix} \cdot g \right| \tag{29}$$

where

$$g = \left(\det \begin{bmatrix} D_x - A_x & D_y - A_y & D_z - A_z \\ D_x - B_x & D_y - B_y & D_z - B_z \\ D_x - C_x & D_y - C_y & D_z - C_z \end{bmatrix} \right)^{-1} \tag{30}$$

If the given reference vector $\vec{p}$ resides inside the tetrahedron $V(A, B, C, D)$, the sum of all duty cycles is equal to one,

$$d_A + d_B + d_C + d_D = 1 \tag{31}$$

but if point P lies outside the tetrahedron, as it is shown in Fig. 8, the length of $\vec{p}$ has to be rescaled by factor ζ

$$\zeta = \frac{|AP_A|}{|AP|} = \frac{|AP_A|}{|AP_A| + |P_AP|} \tag{32}$$

The following tetrahedrons $V(A, B, C, D)$ and $V(B, C, D, P)$ have a common base triangle $\Delta(B, C, D)$. In addition, straight line n is perpendicular to the triangle $\Delta(B, C, D)$ surface. Therefore the scaling factor ζ can be also calculated based on Thales theorem

$$\zeta = \frac{h_{ABCD}}{h_{ABCD} + h_{BCDP}} \cdot \frac{\frac{\Delta_{BCD}}{3}}{\frac{\Delta_{BCD}}{3}} = \frac{V_{ABCD}}{V_{ABCD} + V_{BCDP}} \tag{33}$$

There are two tetrahedrons shown in Fig. 9. Selection of the appropriate tetrahedron strongly depends on checking the result of duty cycle summation. Only if point P is inside the tetrahedron, the sum (31), by definition, is equal to unity.

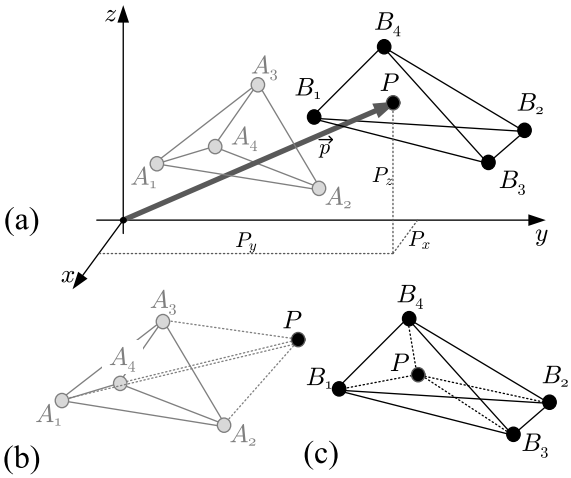


FIGURE 9. Two tetrahedrons in three dimensional system: (a) vector $\vec{p}$ resides in tetrahedron $V(B_1, B_2, B_3, B_4)$, (b) the sum of PWMDC is greater than one, (c) the sum of PWMDC is equal one.

IV. THREE-DIMENSIONAL SPACE VECTOR MODULATION FOR THREE-LEVEL FOUR-LEG DIODE CLAMPED INVERTER

A three–dimensional fast algorithm in *abc* coordinates has been proposed in [4], [19], [26] but that representation limits the potential of space vector modulation. The DC–link voltage balancing [18], [21]–[24], [27], [28] is omitted though it is a critical task, especially in the Active Power Filter application [10], [13], [29], [30]. In addition, the overmodulation aspect of converter control is also not considered [31]. By using the proposed method of PWMDC calculation, balanced and unbalanced systems can be realized with balanced or unbalanced DC–link voltages. Moreover, during the DC–link voltage balancing process, the output average voltages are precisely synthesized and no output current distortion is observed [18]. The main advantage of accurate control of the DC–link voltages, is that it allows to use smaller capacitors in the DC–link. Note that the main purpose of this section is to demonstrate the abilities of the proposed approach of duty cycle computing. In order to achieve a better understanding, the discussion is divided into smaller subsections.

NOMENCLATURE

For the clarity in further consideration, the following nomenclature is proposed:

u_{DC}	DC-link total voltage.
u_{C1}	lower capacitor voltage.
u_{C2}	upper capacitor voltage.
u_Δ	neutral-point voltage.
i_{NP}	neutral-point (NP) average current.
l	number of converter leg $l = 1..4$.
s_{il}	i-switch, l-leg, $s_{il} = \{0, 1\}$ switch is $\{off, on\}$.
i_l	l-leg output current.
u_{lk}	l-leg output voltage, k-switching state.
h_{lk}	l-leg switches state, k-switching state.

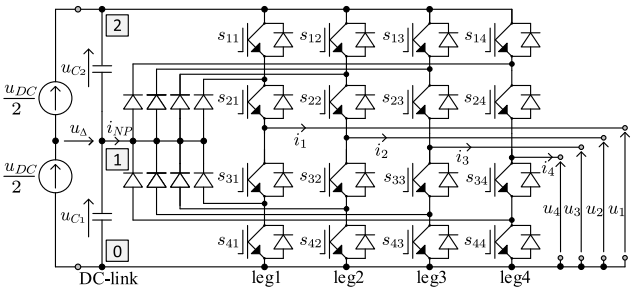


FIGURE 10. Three-level four-leg neutral-point clamped converter.

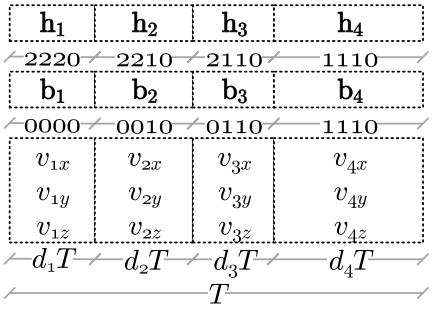


FIGURE 11. Example switching states sequence.

b_{lk}	l-leg neutral-point flag, k-switching state.
$\mathbf{h_k}$	$[h_{1k}, h_{2k}, h_{3k}, h_{4k}]$ leg k-switch state vector.
$\mathbf{b_k}$	$[b_{1k}, b_{2k}, b_{3k}, b_{4k}]$ leg neutral-point k-flag vector.
$\mathbf{d_k}$	$[d_1, d_2, d_3, d_4]$ PWM duty cycle vector.
$\mathbf{B}$	$[\mathbf{b_1}, \mathbf{b_2}, \mathbf{b_3}, \mathbf{b_4}]^{\mathrm{T}}$ neutral-point flags matrix.

PRINCIPLE OF OPERATION

The 3–level 4–leg Diode–Clamped inverter is presented in Fig. 10. A general k-switching state of each converter leg can be characterized using three following quantities u_{lk}, h_{lk}, b_{lk}

$$\{u_{lk}, h_{lk}, b_{lk}\} = \begin{cases} \{u_{DC}, 2, 0\} & \Leftrightarrow [s_{1l}, s_{2l}, s_{3l}, s_{4l}] = [1, 1, 0, 0] \\ \{u_{C1}, 1, 1\} & \Leftrightarrow [s_{1l}, s_{2l}, s_{3l}, s_{4l}] = [0, 1, 1, 0] \\ \{0, 0, 0\} & \Leftrightarrow [s_{1l}, s_{2l}, s_{3l}, s_{4l}] = [0, 0, 1, 1] \end{cases} \quad (34)$$

The first u_l is the l-leg output voltage value, the second one h_l describes the combination of gate signals of power switches s_{il}, and the b_l informs whether the load is connected to the neutral-point (NP), marked as a square "1" in Fig. 10. The total number of possible switch state vectors is equal 3^4. An appropriate description can be found in the Table 5 and Table 6 located in the Appendix section. The grey color of the table row indicates that u_Δ is not affected by a DC–link voltage asymmetry. Thus, coordinates of this vector in xyz reference frame are independent of u_Δ. The 3D–SVM implementation is performed by the generating proper sequence of four switch state vectors $\mathbf{h_1}$, $\mathbf{h_2}$, $\mathbf{h_3}$, $\mathbf{h_4}$ within a period T as it is shown in Fig. 11. In reference to the publications [20], [32] the three-dimensional space contains 24 base tetrahedrons.

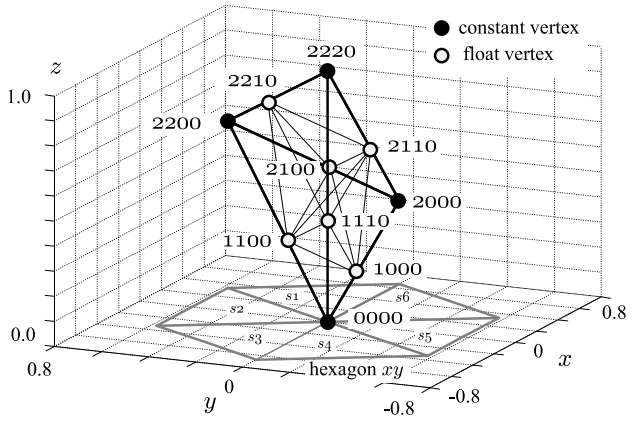


FIGURE 12. The *n*-type base tetrahedron $\triangle_1$, in sector *s*1 for $u_\Delta = 0.1$ p.u.

TABLE 3. The switch states matrix **H** for the base tetrahedrons in sector 1.

$\triangle_1$ case	*n*-type	*p*-type
1	[2220;2210;2110;1110]	[2221;2220;2210;2110]
2	[1101;1100;1000;0000]	[2222;2212;2211;2111]
3	[1101;1001;1000;0000]	[2222;2212;2112;2111]
4	[1101;1001;0001;0000]	[2222;2212;2112;1112]
5	[2210;2110;1110;1100]	[2221;2211;2210;2110]
6	[2101;2100;2000;1000]	[2111;2101;2100;2000]
7	[2101;2001;2000;1000]	[2111;2101;2001;2000]
8	[1102;1101;1001;0001]	[2212;2112;1112;1102]
$\triangle_2$ case	*n*-type	*p*-type
1	[2110;1110;1100;1000]	[2221;2211;2111;2110]
2	[2101;2100;1100;1000]	[2211;2111;2101;2100]
3	[2101;2001;1001;1000]	[2112;2111;2101;2001]
4	[1102;1002;1001;0001]	[2112;1112;1102;1002]
5	[1110;1100;1000;0000]	[2222;2221;2211;2111]
6	[2101;1101;1100;1000]	[2212;2211;2111;2101]
7	[2102;2101;2001;1001]	[2112;2102;2101;2001]
8	[1102;1002;0002;0001]	[1112;1102;1002;0002]
$\triangle_3$ case	*n*-type	*p*-type
1	[2110;2100;2000;1000]	[2111;2110;2100;2000]
2	[2201;2200;2100;1100]	[2211;2201;2200;2100]
3	[2102;2002;2001;1001]	[2112;2102;2002;2001]
4	[2102;2002;1002;1001]	[2112;2102;2002;1002]
5	[2210;2110;2100;1100]	[2211;2210;2110;2100]
6	[2201;2101;2100;1100]	[2211;2201;2101;2100]
7	[2101;1101;1001;1000]	[2212;2112;2111;2101]
8	[2102;1102;1101;1001]	[2212;2112;2102;1102]
$\triangle_4$ case	*n*-type	*p*-type
1	[2110;2100;1100;1000]	[2211;2111;2110;2100]
2	[2201;2101;1101;1100]	[2212;2211;2201;2101]
3	[2102;2101;1101;1001]	[2212;2112;2102;2101]
4	[2102;1102;1002;1001]	[2112;2102;1102;1002]
5	[2210;2200;2100;1100]	[2211;2210;2200;2100]
6	[2202;2201;2101;1101]	[2212;2202;2201;2101]
7	[2202;2102;2101;1101]	[2212;2202;2102;2101]
8	[2202;2102;1102;1101]	[2212;2202;2102;1102]

There are four base tetrahedrons $\triangle_1$, $\triangle_2$, $\triangle_3$, and $\triangle_4$ per one sector. An example of a base tetrahedron $\triangle_1$ resides in sector *s*1 as is illustrated in Fig. 12. Each base tetrahedron can be divided into 8 smaller tetrahedrons, which correspond to an appropriate switch states matrix **H** in Table 3. Due to the DC–link voltage unbalance phenomena, the *n*-type and *p*-type switch state matrix can be used for capacitor voltage balancing. The flowchart of the proposed algorithm is presented in Fig. 13 and described in next subsection.

THE ALGORITHM FLOWCHART

The *position* of the reference vector $\vec{p}$ is defined by one *sector* {*s*1, *s*2, *s*3, *s*4, *s*5, *s*6} and one base *tetrahedron* {$\triangle_1$, $\triangle_2$, $\triangle_3$, $\triangle_4$}. At step 1 the *position* of $\vec{p}$ is calculated according to the solution given in [20] and is based on a few conditional operations. Next, the six *float vertex* coordinates for *n*-type

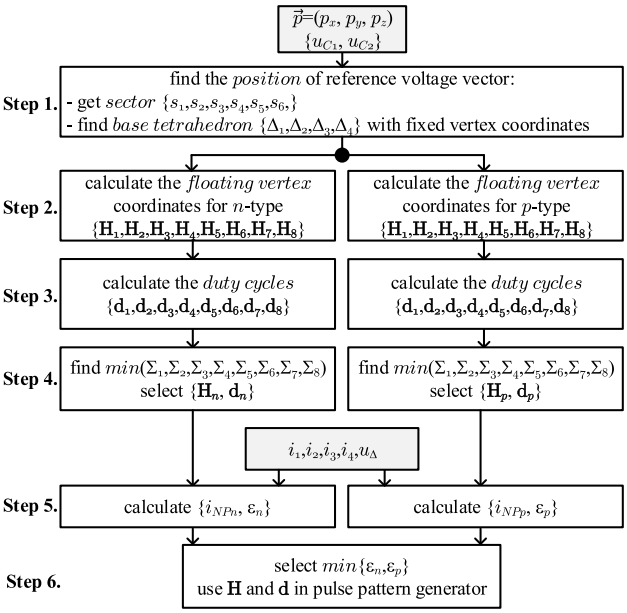


FIGURE 13. The 3D-SVM modulation flowchart.

and *p*-type **H**, from Table 3, are calculated at step 2 using Clarke transform as follows

$$\begin{bmatrix} v_{1x} & v_{2x} & v_{3x} & v_{4x} \\ v_{1y} & v_{2y} & v_{3y} & v_{4y} \\ v_{1z} & v_{2z} & v_{3z} & v_{4z} \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} \end{bmatrix} \cdot \mathbf{U} \tag{35}$$

where

$$\mathbf{U} = \begin{bmatrix} u_{11} - u_{41} & u_{21} - u_{41} & u_{31} - u_{41} \\ u_{12} - u_{42} & u_{22} - u_{42} & u_{32} - u_{42} \\ u_{13} - u_{43} & u_{23} - u_{43} & u_{33} - u_{43} \\ u_{14} - u_{44} & u_{24} - u_{44} & u_{34} - u_{44} \end{bmatrix}^{\mathrm{T}} \tag{36}$$

At step 3 all needed duty cycles are computed based on *barycentric coordinates* (26)-(30). Calculation of the following sum at step 4 for each switch state matrix **H**

$$\Sigma_k = sum(\mathbf{d}_k) \tag{37}$$

can be used for the selection of the one right candidate from 8-element set. If the sum (37) is a minimal element, ideally equal unity, the right switch state matrix **H** will be selected. The fifth step is the selection of the most appropriate switch state matrix $\mathbf{H_p}$ or $\mathbf{H_n}$ respectively. The decision can be based on the comparison of the predicted influence of the choice on the NP imbalance voltage

$$u_\Delta = \frac{u_{C2} - u_{C1}}{2u_{DC}} \tag{38}$$

A simple analysis of the four possible combinations of the signs of the imbalance voltage and the average neutral point

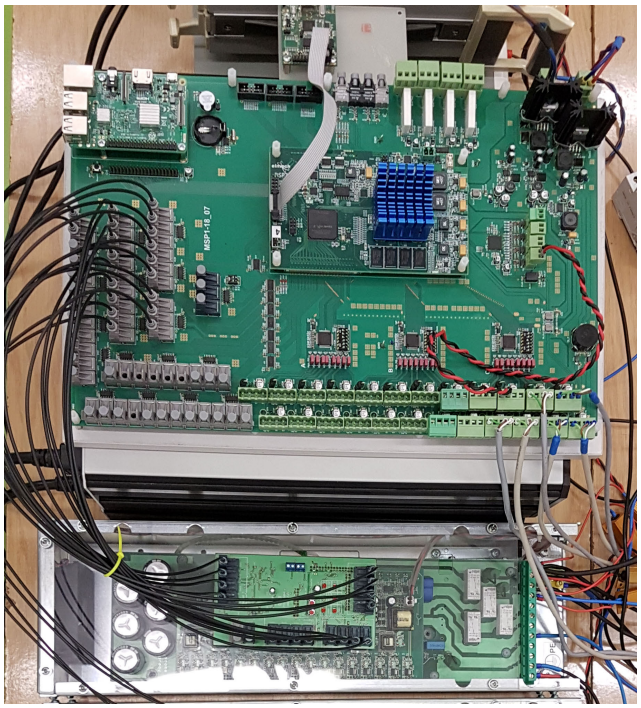


FIGURE 14. An experimental prototype with DCS.

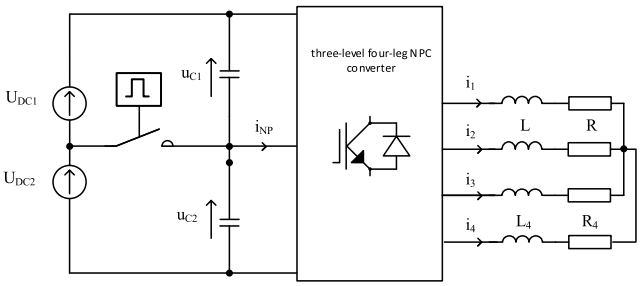


FIGURE 15. Schematic of experiment.

current leads to the conclusion that it is sufficient to compare the following quantities

$$\varepsilon_n = i_{NPn} \cdot u_\Delta, \varepsilon_p = i_{NPp} \cdot u_\Delta \tag{39}$$

where i_{NPn} and i_{NPp} are estimates of the expected average neutral point currents corresponding to their respective types of bias

$$\begin{cases} i_{NPn} = [\, i_1 \quad i_2 \quad i_3 \quad i_4 \,] \cdot \mathbf{B}_n^{\mathrm{T}} \cdot \mathbf{d}_n^{\mathrm{T}} \\ i_{NPp} = [\, i_1 \quad i_2 \quad i_3 \quad i_4 \,] \cdot \mathbf{B}_p^{\mathrm{T}} \cdot \mathbf{d}_p^{\mathrm{T}} \end{cases} \tag{40}$$

If ε_n is greater than ε_p then $\mathbf{H}_p$ should be selected; otherwise, the better choice is negative bias represented by $\mathbf{H}_n$. Finally, at step 6, the selected pair $\{\mathbf{H}, \mathbf{d}\}$ is sent to the pulse pattern generator implemented in a programmable logic device.

V. EXPERIMENTAL RESULT

An experimental prototype of an inverter is presented in Fig. 14, while the parameters are presented in Table 4. The digital control system (DCS) contains a DSP (Texas Instruments TMS320C6672) and a field–programmable gate array FPGA (Cyclone V). The DC–link is supplied by two adjustable dc-voltage sources U_{DC1} and U_{DC2} with additional switch S for voltage balancing experiments. Schematic of the experimental setup is illustrated in Fig. 15. The experimental research plan included the following issues:

- DC–link capacitors active voltage balancing ability using redundant switch states (Fig. 16),
- Preserving the sinusoidal output currents during the DC–link voltages asymmetry (Fig. 17),
- Proper generation of constant gamma component in output currents by adding the common signal (Fig. 18),

TABLE 4. Experiment circuit diagram and modulation parameters.

symbol	value	description
E_1	75V, 45V	DC source voltages
E_2	75V, 45V	DC source voltages
C_1	300μF	upper capacity
C_2	300μF	lower capacity
R	15Ω	load resistor
L	3mH	load inductor
R_4	2.2Ω	4–th leg resistor
L_4	6mH	4–th leg inductor
f_c	5kHz	PWM frequency
f_n	50Hz	output frequency
S	ON/OFF	neutral point additional switch

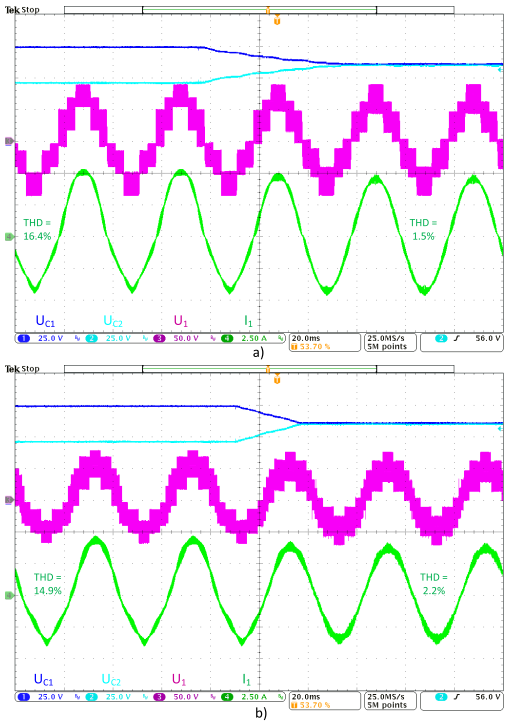


FIGURE 16. DC–link capacitors voltage active balancing for referenced vectors without capacitors voltage asymmetry compensation a) $\bar{p} = [0.57 \cdot \cos(\omega t), 0.57 \cdot \sin(\omega t), 0]$, b) $\bar{p} = [0.46 \cdot \cos(\omega t), 0.46 \cdot \sin(\omega t), 0]$.

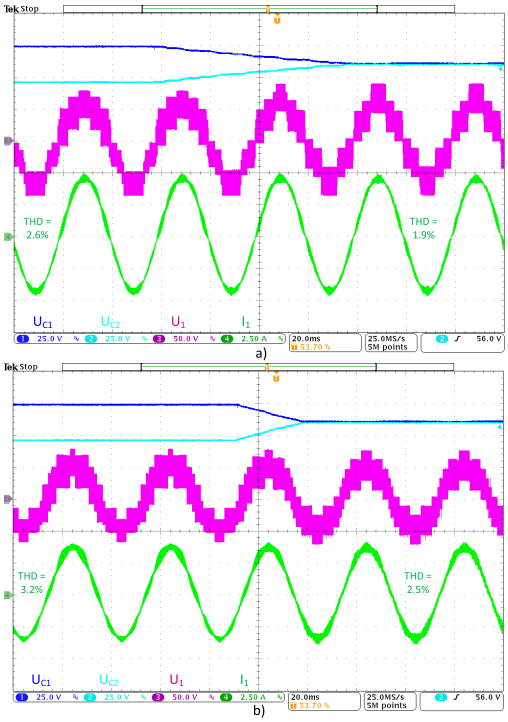


FIGURE 17. Preserving the sinusoidal output currents during the DC–link voltages asymmetry and active balancing for referenced vectors a) $\bar{p} = [0.57 \cdot \cos(\omega t), 0.57 \cdot \sin(\omega t), 0]$, b) $\bar{p} = [0.46 \cdot \cos(\omega t), 0.46 \cdot \sin(\omega t), 0]$.

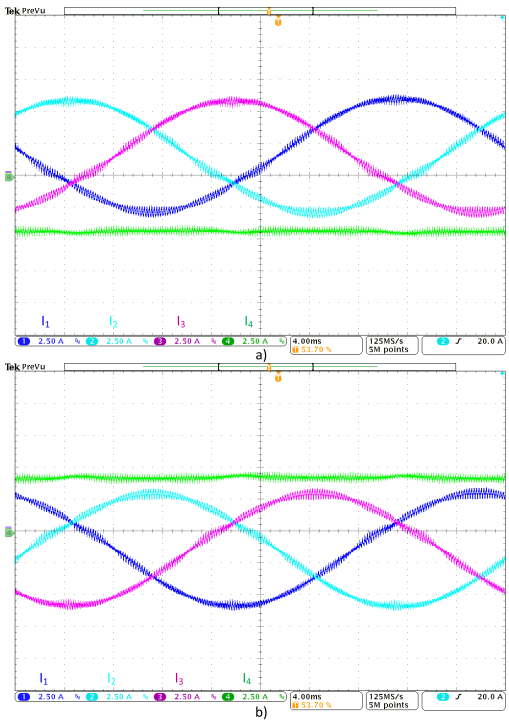


FIGURE 18. Generation of constant gamma component in output currents for referenced vectors a) $\bar{p} = [0.57 \cdot \cos(\omega t), 0.57 \cdot \sin(\omega t), 0.5]$, b) $\bar{p} = [0.57 \cdot \cos(\omega t), 0.57 \cdot \sin(\omega t), -0.5]$.

- Selected higher-order current harmonic injection (Fig. 19),
- The phase current asymmetry generation (Fig. 20).

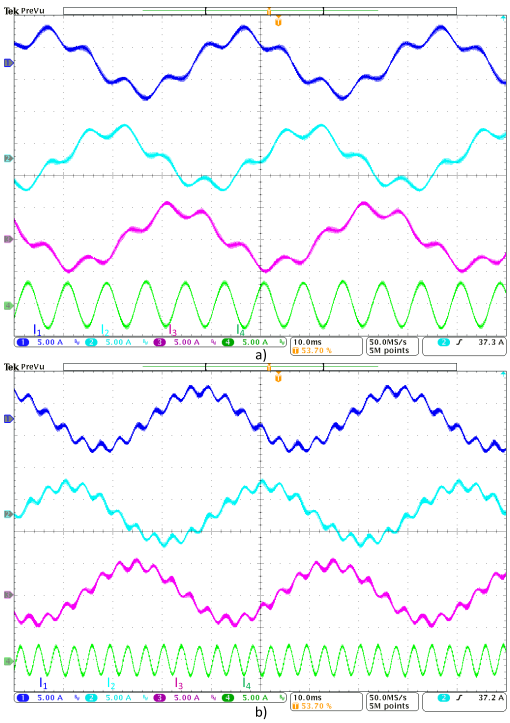


FIGURE 19. Selected harmonic injection in output currents for referenced vectors a) 5–th harmonic $\bar{p} = [0.57 \cdot \cos(\omega t), 0.57 \cdot \sin(\omega t), 0.3 \cdot \cos(5\omega t)]$, b) 11–th harmonic $\bar{p} = [0.57 \cdot \cos(\omega t), 0.57 \cdot \sin(\omega t), 0.3 \cdot \cos(11\omega t)]$.

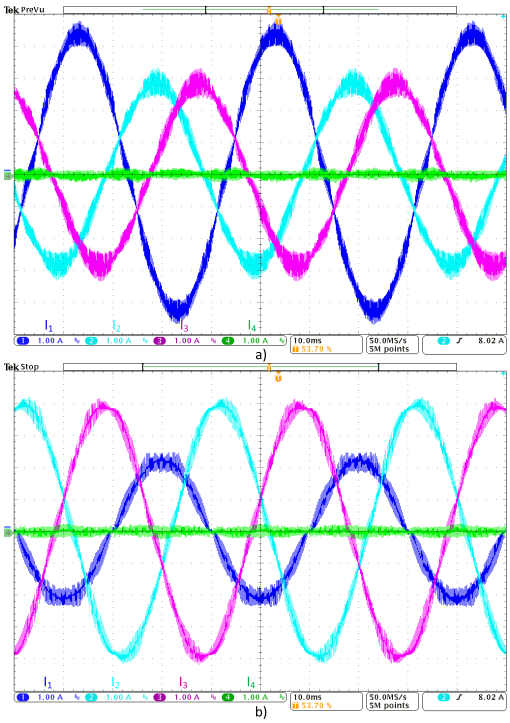


FIGURE 20. The output current asymmetry generation for referenced vectors a) $\bar{p} = [0.57 \cdot \cos(\omega t), 0.285 \cdot \sin(\omega t), 0]$, b) $\bar{p} = [0.285 \cdot \cos(\omega t), 0.57 \cdot \sin(\omega t), 0]$.

VI. CONCLUSION

The proposed algorithms using *barycentric coordinates* based on *area* – 2D case, solved by (12), (13) – or

TABLE 5. The leg voltages, states and neutral–point flags for Three–Level Four–Leg Neutral–Point Clamped Converter (part I).

	u_1	u_2	u_3	u_4	h	b
1	0	0	0	0	0000	0000
2	0	0	0	u_{C1}	0001	0001
3	0	0	0	u_{DC}	0002	0000
4	0	0	u_{C1}	0	0010	0010
5	0	0	u_{C1}	u_{C1}	0011	0011
6	0	0	u_{C1}	u_{DC}	0012	0010
7	0	0	u_{DC}	0	0020	0000
8	0	0	u_{DC}	u_{C1}	0021	0001
9	0	0	u_{DC}	u_{DC}	0022	0000
10	0	u_{C1}	0	0	0100	0100
11	0	u_{C1}	0	u_{C1}	0101	0101
12	0	u_{C1}	0	u_{DC}	0102	0100
13	0	u_{C1}	u_{C1}	0	0110	0110
14	0	u_{C1}	u_{C1}	u_{C1}	0111	0111
15	0	u_{C1}	u_{C1}	u_{DC}	0112	0110
16	0	u_{C1}	u_{DC}	0	0120	0100
17	0	u_{C1}	u_{DC}	u_{C1}	0121	0101
18	0	u_{C1}	u_{DC}	u_{DC}	0122	0100
19	0	u_{DC}	0	0	0200	0000
20	0	u_{DC}	0	u_{C1}	0201	0001
21	0	u_{DC}	0	u_{DC}	0202	0000
22	0	u_{DC}	u_{C1}	0	0210	0010
23	0	u_{DC}	u_{C1}	u_{C1}	0211	0011
24	0	u_{DC}	u_{C1}	u_{DC}	0212	0010
25	0	u_{DC}	u_{DC}	0	0220	0000
26	0	u_{DC}	u_{DC}	u_{C1}	0221	0001
27	0	u_{DC}	u_{DC}	u_{DC}	0222	0000
28	u_{C1}	0	0	0	1000	1000
29	u_{C1}	0	0	u_{C1}	1001	1001
30	u_{C1}	0	0	u_{DC}	1002	1000
31	u_{C1}	0	u_{C1}	0	1010	1010
32	u_{C1}	0	u_{C1}	u_{C1}	1011	1011
33	u_{C1}	0	u_{C1}	u_{DC}	1012	1010
34	u_{C1}	0	u_{DC}	0	1020	1000
35	u_{C1}	0	u_{DC}	u_{C1}	1021	1001
36	u_{C1}	0	u_{DC}	u_{DC}	1022	1000
37	u_{C1}	u_{C1}	0	0	1100	1100
38	u_{C1}	u_{C1}	0	u_{C1}	1101	1101
39	u_{C1}	u_{C1}	0	u_{DC}	1102	1100
40	u_{C1}	u_{C1}	u_{C1}	0	1110	1110

TABLE 6. The leg voltages, states and neutral–point flags for Three–Level Four–Leg Neutral–Point Clamped Converter (part II).

	u_1	u_2	u_3	u_4	h	b
41	u_{C1}	u_{C1}	u_{C1}	u_{C1}	1111	1111
42	u_{C1}	u_{C1}	u_{C1}	u_{DC}	1112	1110
43	u_{C1}	u_{C1}	u_{DC}	0	1120	1100
44	u_{C1}	u_{C1}	u_{DC}	u_{C1}	1121	1101
45	u_{C1}	u_{C1}	u_{DC}	u_{DC}	1122	1100
46	u_{C1}	u_{DC}	0	0	1200	1000
47	u_{C1}	u_{DC}	0	u_{C1}	1201	1001
48	u_{C1}	u_{DC}	0	u_{DC}	1202	1000
49	u_{C1}	u_{DC}	u_{C1}	0	1210	1010
50	u_{C1}	u_{DC}	u_{C1}	u_{C1}	1211	1011
51	u_{C1}	u_{DC}	u_{C1}	u_{DC}	1212	1010
52	u_{C1}	u_{DC}	u_{DC}	0	1220	1000
53	u_{C1}	u_{DC}	u_{DC}	u_{C1}	1221	1001
54	u_{C1}	u_{DC}	u_{DC}	u_{DC}	1222	1000
55	u_{DC}	0	0	0	2000	0000
56	u_{DC}	0	0	u_{C1}	2001	0001
57	u_{DC}	0	0	u_{DC}	2002	0000
58	u_{DC}	0	u_{C1}	0	2010	0010
59	u_{DC}	0	u_{C1}	u_{C1}	2011	0011
60	u_{DC}	0	u_{C1}	u_{DC}	2012	0010
61	u_{DC}	0	u_{DC}	0	2020	0000
62	u_{DC}	0	u_{DC}	u_{C1}	2021	0001
63	u_{DC}	0	u_{DC}	u_{DC}	2022	0000
64	u_{DC}	u_{C1}	0	0	2100	0100
65	u_{DC}	u_{C1}	0	u_{C1}	2101	0101
66	u_{DC}	u_{C1}	0	u_{DC}	2102	0100
67	u_{DC}	u_{C1}	u_{C1}	0	2110	0110
68	u_{DC}	u_{C1}	u_{C1}	u_{C1}	2111	0111
69	u_{DC}	u_{C1}	u_{C1}	u_{DC}	2112	0110
70	u_{DC}	u_{C1}	u_{DC}	0	2120	0100
71	u_{DC}	u_{C1}	u_{DC}	u_{C1}	2121	0101
72	u_{DC}	u_{C1}	u_{DC}	u_{DC}	2122	0100
73	u_{DC}	u_{DC}	0	0	2200	0000
74	u_{DC}	u_{DC}	0	u_{C1}	2201	0001
75	u_{DC}	u_{DC}	0	u_{DC}	2202	0000
76	u_{DC}	u_{DC}	u_{C1}	0	2210	0010
77	u_{DC}	u_{DC}	u_{C1}	u_{C1}	2211	0011
78	u_{DC}	u_{DC}	u_{C1}	u_{DC}	2212	0010
79	u_{DC}	u_{DC}	u_{DC}	0	2220	0000
80	u_{DC}	u_{DC}	u_{DC}	u_{C1}	2221	0001
81	u_{DC}	u_{DC}	u_{DC}	u_{DC}	2222	0000

volume – 3D case, solved by (26)–(30) – are proposed as a tool for PWMDC computations, especially for complex and unbalanced lattices of inverter vectors. Results of benchmark presented in Table 2 show the main advantage of the proposed computation idea – a short time of code execution, what leads to the conclusion, that this method is particularly useful for complex systems (multilevel, multiphase inverters, high–frequency systems, virtual vector methods). The concept permits building the modulation algorithms by referring straight to the converter switch state vectors. Thus, the presented computation idea is suitable for multilevel inverters of different types (diode clamped, flying capacitors or matrix converters). The proposed algorithm enables precise voltages and currents forming during unbalanced capacitor voltages (Fig. 17), as well as it allows to balance DC–link voltages (Fig. 16) using redundant vectors. Comparing currents in Fig. 16 and Fig. 17 it is notable, that considering DC–link unbalanced voltages leads to a better quality of output currents. Possibility of injecting chosen harmonics (Fig. 19) and generation of asymmetry (Fig. 20) or constant gamma component (Fig. 18) in currents show that the proposed algorithm can be a suitable tool for Active Power Filters. The use of barycentric coordinates helps in the development of computation schemes. Note that the method does not influence the results of the PWM duty cycle computations at all, so further analysis of formed voltages and currents in this paper seems pointless, because this kind of research is widely reported in the literature.

The presented article shows that trigonometric functions can be eliminated from the modulation algorithm. The presented elaborations lead to the conclusion, that the PWM duty cycle computation can be realized using the simple rational functions and voltages coordinates (in most cases calculated using the Clarke transform). In general, this approach does not give the new spectacular PWM features observed in the frequency spectrum of voltages and currents. The obtained simplification permits for using the low costs FPGA devices because the core of calculation can be based on the parallel add/subtract and multiply operation. If we take into account a very high operating frequency of the GaN or SiC power switches and the limitations of the one-core processors, the undertaken research is purposeful and justified [33]–[36]. The proposed solution is particularly useful when considering the irregular space of voltage vectors. Presented solutions also add uniformity and transparency to the description of PWM–related problems.

The paper authors demonstrated that the proposed PWM duty cycle computation can be successfully applied to the three-dimensional space vector modulation for a three–level four–leg NPC inverter where the volume–based rational functions have been used.

APPENDIX

See Tables 5 and 6.

REFERENCES

[1] J. W. Kolar, T. Friedli, J. Rodriguez, and P. W. Wheeler, "Review of three–phase PWM AC–AC converter topologies," *IEEE Trans. Ind. Electron.*, vol. 58, no. 11, pp. 4988–5006, Nov. 2011.

[2] B. Bose, "Power electronics and motor drives recent progress and perspective," *IEEE Trans. Ind. Electron.*, vol. 56, no. 2, pp. 581–588, Feb. 2009.

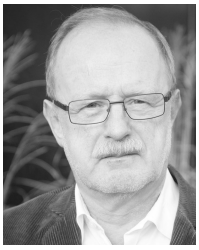
[3] J. Carrasco, L. Franquelo, J. Bialasiewicz, E. Galvan, R. P. Guisado, M. Pratsa, and J. Leon, "Power-electronic systems for the grid integration of renewable energy sources: A survey," *IEEE Trans. Ind. Electron.*, vol. 53, no. 4, pp. 1002–1016, Jun. 2006.
[4] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. Franquelo, B. Wu, J. Rodriguez, M. Perez, and J. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.
[5] K. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu, and S. Jain, "Multilevel inverter topologies with reduced device count: A review," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 135–151, Jan. 2016.
[6] P. Szczepankowski and J. Nieznanski, "Application of barycentric coordinates in space vector PWM computations," *IEEE Access*, vol. 7, pp. 91499–91508, 2019.
[7] F. Zhang and Y. Yan, "Selective harmonic elimination PWM control scheme on a three–phase four–leg voltage source inverter," *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1682–1689, Jul. 2009.
[8] B. Saber, B. Abdelkader, B. Said, and B. Mansour, "Reactive power compensation in three-phase four-wire distribution system using four-leg DSATATCOM based on symmetrical components," in *Proc. 4th Int. Conf. Electr. Eng. (ICEE)*, Dec. 2015, pp. 1–4.
[9] Q. Tabart, I. Vechiu, A. Etxeberria, and S. Bacha, "Hybrid energy storage system microgrids integration for power quality improvement using four–leg three–level NPC inverter and second–order sliding mode control," *IEEE Trans. Ind. Electron.*, vol. 65, no. 1, pp. 424–435, Jan. 2018.
[10] B.-F. Chen, L. Yang, D.-K. Hu, J.-J. Sun, and X.-M. Zha, "A novel and small-capacity neutral line active power filter in three-phase four-wire system," in *Proc. Int. Conf. Power Electron. Drive Syst. (PEDS)*, Nov. 2009, pp. 371–375.
[11] B. Saber, B. Abdelkader, B. Said, and B. Mansour, "Neutral current compensation of three–phase four-wire distribution system using three–level four–leg DSTATCOM based on simplified 3DSVM algorithm," in *Proc. 6th Int. Conf. Control Eng. Inf. Technol.(CEIT)*, Oct. 2018, pp. 1–6.
[12] S. Sajjad Seyedalipour, S. Bayhan, and H. Komurcugil, "Lyapunov-function-based control approach for three–level four–leg shunt active power filters with nonlinear and unbalanced loads," in *Proc. IEEE 27th Int. Symp. Ind. Electron. (ISIE)*, Jun. 2018, pp. 427–432.
[13] M. Bouzidi and S. Barkat, "Backstepping–direct power control of three-level four–leg shunt active power filter," in *Proc. Int. Conf. Commun. Electr. Eng. (ICCEE)*, Dec. 2018, pp. 1–6.
[14] N. Celanovic and D. Boroyevich, "A fast space-vector modulation algorithm for multilevel three-phase converters," *IEEE Trans. Ind Appl.*, vol. 37, no. 2, pp. 637–641, Mar./Apr. 2001.
[15] L. Hu, H. Wang, V. Deng, and X. He, "A simple SVPWM algorithm for multilevel inverters," in *Proc. IEEE 35th Annu. Power Electron. Specialists Conf.*, vol. 5, Nov. 2004, pp. 3476–3480.
[16] B. Jacob and M. R. Baiju, "A new space vector modulation scheme for multilevel inverters which directly vector quantize the reference space vector," *IEEE Trans. Ind. Electron.*, vol. 62, no. 1, pp. 88–95, Jan. 2015.
[17] Z. Shu, N. Ding, J. Chen, H. Zhu, and X. He, "Multilevel SVPWM with DC–link capacitor voltage balancing control for diode–clamped multilevel converter based STATCOM," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1884–1896, May 2013.
[18] J. Pou, D. Boroyevich, and R. Pindado, "New feedforward space-vector PWM method to obtain balanced AC output voltages in a three-level neutral-point-clamped converter," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 1026–1034, Oct. 2002.
[19] J. I. Leon, S. Vazquez, R. Portillo, L. G. Franquelo, J. M. Carrasco, P. W. Wheeler, and A. J. Watson, "Three-dimensional feedforward space vector modulation applied to multilevel diode-clamped converters," *IEEE Trans. Ind. Electron.*, vol. 56, no. 1, pp. 101–109, Jan. 2009.
[20] R. Zhang, V. Prasad, D. Boroyevich, and F. Lee, "Three-dimensional space vector modulation for four-leg voltage-source converters," *IEEE Trans. Power Electron.*, vol. 17, no. 3, pp. 314–326, May 2002.
[21] N. Celanovic and D. Boroyevich, "A comprehensive study of neutral point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters," *IEEE Trans. Power Electron.*, vol. 15, no. 2, pp. 242–249, Mar. 2000.
[22] H. Zhang, S. Jon Finney, A. Massoud, and B. Williams, "An SVM algorithm to balance the capacitor voltages of the three–level NPC active power filter," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2694–2702, Nov. 2008.
[23] A. Lewicki, Z. Krzeminski, and H. Abu-Rub, "Space–vector pulsewidth modulation for three–level NPC converter with the neutral point voltage control," *IEEE Trans. Ind. Electron.*, vol. 58, no. 11, pp. 5076–5086, Nov. 2011.
[24] R. Maheshwari, S. Munk-Nielsen, and S. Busquets-Monge, "Design of neutral–point voltage controller of a three–level NPC inverter with small DC–link capacitors," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1861–1871, May 2013.
[25] M. S. Floater, K. Hormann, and G. Kós, "A general construction of barycentric coordinates over convex polygons," *Adv. Comput. Math.*, vol. 24, nos. 1–4, pp. 311–331, Jan. 2006.
[26] L. Franquelo, M. Prats, R. Portillo, J. Galvan, M. Perales, J. Carrasco, E. Diez, and J. Jimenez, "Three-dimensional space-vector modulation algorithm for four-leg multilevel converters using abc coordinates," *IEEE Trans. Ind. Electron.*, vol. 53, no. 2, pp. 458–466, Apr. 2006.
[27] S. Busquets-Monge, J. Bordonau, D. Boroyevich, and S. Somavilla, "The nearest three virtual space vector PWM—a modulation for the comprehensive neutral-point balancing in the three-level NPC inverter," *IEEE Power Electron. Lett.*, vol. 2, no. 1, pp. 11–15, Mar. 2004.
[28] J. Yao and T. Green, "DC-link capacitors sizing for three-level neutral-point-clamped inverters in four-wire distributed generation systems," in *Proc. Int. Conf. Future Power Syst.*, Nov. 2005, p. 5.
[29] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of three-phase improved power quality AC-DC converters," *IEEE Trans. Ind. Electron.*, vol. 51, no. 3, pp. 641–660, Jun. 2004.
[30] F. Rojas, R. Kennel, R. Cardenas, R. Repenning, J. C. Clare, and M. Diaz, "A new space-vector-modulation algorithm for a three–level four–leg NPC inverter," *IEEE Trans. Energy Convers.*, vol. 32, no. 1, pp. 23–35, Mar. 2017.
[31] S. Busquets-Monge, R. Maheshwari, and S. Munk-Nielsen, "Overmodulation of *n*-level three–leg DC–AC diode–clamped converters with comprehensive capacitor voltage balance," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1872–1883, May 2013.
[32] X. Li, Z. Deng, Z. Chen, and Q. Fei, "Analysis and simplification of three–dimensional space vector PWM for three–phase four–leg inverters," *IEEE Trans. Ind. Electron.*, vol. 58, no. 2, pp. 450–464, Feb. 2011.
[33] A. Hassan, Y. Savaria, and M. Sawan, "GaN integration technology, an ideal candidate for high–temperature applications: A review," *IEEE Access*, vol. 6, pp. 78790–78802, 2018.
[34] A. Choudhury, "Present status of sic based power converters and gate drivers—A review," in *Proc. Int. Power Electron. Conf. (IPEC-Niigata-ECCE Asia)*, May 2018, pp. 3401–3405.
[35] P. Ning, T. Yuan, Y. Kang, C. Han, and L. Li, "Review of Si IGBT and SiC MOSFET based on hybrid switch," *Chin. J. Electr. Eng.*, vol. 5, no. 3, pp. 20–29, Sep. 2019.
[36] J. O. Gonzalez, R. Wu, S. Jahdi, and O. Alatise, "Performance and reliability review of 650V and 900V silicon and SiC devices: MOSFETs, Cascode JFETs and IGBTs," *IEEE Trans. Ind. Electron.*, to be published.

PAWEŁ SZCZEPANKOWSKI (Member, IEEE) received the Ph.D. degree in electrical engineering from the Gdańsk University of Technology, Poland, in 2009. He has authored or coauthored more than 30 scientific and technical articles. His research interests include design, control, diagnostics, modeling, and simulation of power electronic converters, including multilevel and matrix topologies, and signal processing with the use of advanced DSP nad FPGA devices. He is a member of the LINTE^2 Laboratory.

NIKOLAI POLIAKOV received the B.S. and M.S. degrees in electrical engineering from ITMO University, Saint Petersburg, Russia, in 2009 and 2011, respectively. He defended the Ph.D. thesis at ITMO University, Russia, in 2016. He is currently an Associate Professor with the Faculty of Control Engineering and Robotics, ITMO University. His current research interests include power converters design, power electronics, power efficiency, wireless power transfer systems, and control theory and its applications.

DENIS VERTEGEL received the B.S. and M.S. degrees in electrical engineering from ITMO University, Saint Petersburg, Russia, in 2016 and 2018, respectively, where he is currently pursuing the Ph.D. degree with the Faculty of Control Engineering and Robotics. His research interests include power converters, power electronics, multilevel topologies, and multiphase electric drives.

KRZYSZTOF JAKUB SZWARC received the M.S. degree in electrical engineering from the Gdańsk University of Technology, Poland, in 2008. His current research interests include power converters controls, power electronics, coupled reactors theory and applications. He is a member of the LINTE^2 Laboratory.



RYSZARD STRZELECKI received the degree in industrial electronics from the Kyiv University of Technology, in 1981, the Ph.D. degree, in 1984, and the Habilitation (D.Sc.) degree from the Institute of Electrodynamics, Academy of Sciences of the Ukrainian Soviet Socialist Republic, Kiev, in 1991. His D.Sc. thesis was on Prediction Control of the Self Commutation Power Electronics Converters. In 1999, he received the title of Professor of technical sciences. He is currently a Full Professor with the Gdańsk University of Technology, Poland, the Co-Head of the Laboratory of Power Electronics and Automated Electric Drive, ITMO University, Saint Petersburg, Russia, and a Professor of the Łukasiewicz Research Network-Electrical Engineering Institute, Warsaw/Gdańsk, Poland. He is the author of more scientific articles as well as monographs and patents. His interests focus on topologies and control methods as well as industrial application of power electronic systems. He is a member of the LINTE^2 Laboratory.