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ASIC Design Example of Complex SoC with FPGA Prototyping

Abstract. *The paper presents an example of the System on a Chip design, where the FPGA prototyping has been used. Two FPGA prototypes have been realized. The first FPGA prototype uses AVNET board containing Xilinx Virtex4 device accompanied by custom board with required devices. The second FPGA prototype has been built using the custom PCB with Xilinx Virtex-4 XC4VLX60 FPGA accompanied by all needed external components. The final system contains the custom UMC CMOS 130nm ASIC, designed from the FPGA prototypes.*

Streszczenie*. W artykule przedstawiono przykład projektu złożonego cyfrowego układu scalonego z wykorzystaniem prototypowania z użyciem układów FPGA. Wykonano dwa prototypy FPGA. Pierwszy z nich bazuje na gotowej płytce ewaluacyjnej zawierającej układ Xilinx Virtex-4, do której zaprojektowano dodatkową płytkę drukowaną. Drugi prototyp zawiera układ FPGA Xilinx XC4VLX60 wraz ze wszystkimi niezbędnymi komponentami. Końcowy projekt systemu zawiera układ ASIC wykonany w technologii CMOS 130nm firmy UMC (****Przykład projektu układu ASIC zawierającego złożony SoC z wykorzystaniem prototypowania FPGA****).*

Słowa kluczowe: układ FPGA, układ ASIC, projektowanie i weryfikacja, prototypowanie.
Keywords: FPGA, ASIC, design and verification, prototyping.

Introduction

Nowadays the design of digital system is very challenging task. The main problem is the system complexity. Typical design usually consists of many sub blocks, each of them containing a large number of digital gates and Flip-Flops (FFs). Additionally, there are various external devices which generate and receive data. To provide the correct operation of the design, the thorough testing and verification has to be done, which usually takes about 80% of the total design time. The second problem is that there is no universal simulator that can cover the whole system before the fabrication. Of course, there are many simulators which can be used for particular sub blocks, but simulation of the whole product is often problematic, due to the following reasons:

– mixed analog and digital simulations;
– simulation of digital chip with its peripherals (such as memory, bus interfaces or others);
– simulation of digital circuit containing processor unit together with its software stored in the memory;
– long time simulations;
– interpretation of huge amount of data (for example: interpretation of processed voice, pictures and movies).

The design and simulation process can become very difficult when all the above issues are present together in the product. Therefore the designers often build the prototypes and then test them before the final fabrication of the chip [1]. It is particularly important, when the final product is expensive and incurs a significant financial risk.

Fabrication of the Application Specific Integrated Circuit (ASIC) containing digital System on a Chip (SoC) is one of the examples when the prototyping can greatly help in the design process. This paper describes the design and prototyping of the ASIC designed at Technical University of Gdańsk.

Block Diagram of the Realized System

The block diagram of the hardware dedicated for integration, called the Sensor Network Processing Module (SNPM), is presented in Fig. 1 [2, 3]. The SNPM contains the custom microelectronic system with 32-bit processor BA12 from Beyond Semiconductor (the same class as Arm's ARM9TM) and the peripherals connected to the Wishbone bus. The other hardware blocks integrated into the SNPM are: the hardware image processing subsystem, the AES encryption block, the controller for low level operations of the radio transceiver and some other blocks. The SNPM has been defined using VHDL (approx. 18,000 lines of code) and Verilog (approx. 43,000 lines of code) languages. The most of the VHDL and Verilog code is common for FPGA and ASIC prototypes.

The final hardware consists of SNPM installed together with the external hardware modules on a single multi-layer printed circuit board (Fig. 2). The block diagrams are the same for FPGA- and ASIC-based prototypes.

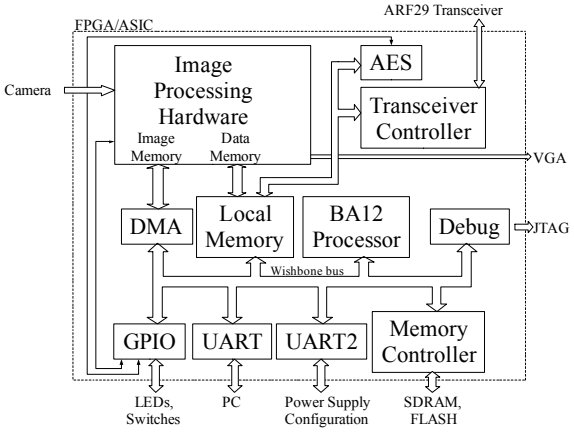

Fig. 1. Block diagram of the designed SoC - the Sensor Network Processing Module (SNMP) [2, 3]

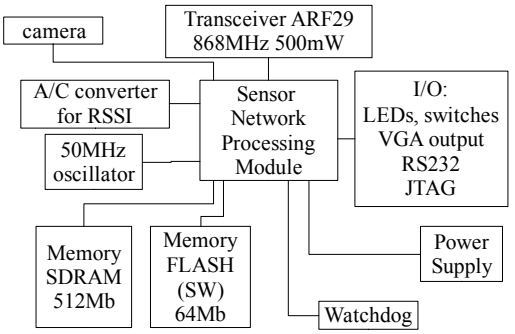

Fig. 2. The block diagram of the sensor network node, utilizing SNPM [2, 3]

FPGA Prototypes

Two FPGA-based prototypes (denoted as #1 and #2) have been built and tested before the final design of the ASIC and its fabrication. The FPGA prototype #1, based on AVNET board with Xilinx XC4VLX60 FPGA, has been additionally connected to the custom boards containing the

camera, radio transceiver and VGA interface (Fig. 3). This prototype helped to solve the following design problems:

– two soft processors (LEON3 and BA12) have been implemented and tested, due to resource utilizations and license conditions, BA12 has been chosen for the final design;
– FLASH memory upgrade subsystem has been developed and tested, this memory is automatically copied into processor's working memory at system startup;
– FPGA platform FLASH memory upgrade subsystem has been developed and tested, this memory contains FPGA chip configuration, the content of the memory is automatically copied into FPGA configuration memory at system startup;
– Printed Circuit Board (PCB) with CMOS camera MT9V111 has been designed, assembled and tested, the sub block for data acquisition from the camera has also been designed and tested (in FPGA);
– PCB board with ARF29 transceiver and VGA output has been designed and assembled, the circuits controlling the transceiver have been designed and tested (in FPGA).

As the result of the first FPGA prototype, the main modules of the design have been evaluated and tested separately, enabling to choose the appropriate size of the FPGA chip for the second prototype.

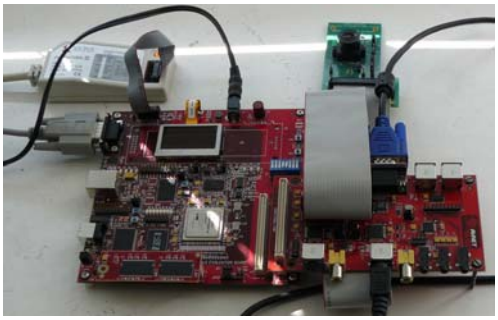

Fig. 3. The picture of the FPGA prototype #1

The second FPGA prototype has been designed to completely satisfy all the requirements of the system. Virtex-4 XC4VLX60 FPGA has been chosen as the target digital device. The schematic diagram has been drawn and the PCB with 6 interconnect layers has been designed and fabricated. The main board contains also: AFR29 transceiver, SDRAM memory, VGA camera, FLASH memory and additional devices, such as the switches, LEDS, the oscillators and the push-buttons. The power supply unit has been designed as a separate module and it is connected with the main board using 8 pin Molex connector. Fig. 4 presents the assembled main board of the system, Fig. 5 presents the set of the assembled sensor nodes, consisting of the case, the battery, the power supply unit and the main board.

The second FPGA prototype has been used for the design and testing of the entire system. All the sub blocks have been designed, simulated on PC, implemented and then tested in real life. Design-simulation-implementation-testing process has been carried several times, until the expected functionality was obtained. The tests have also been carried using the nodes placed on street lamp-pole, in the same environment where the nodes will be installed by end user. One of the node on street lamp-pole has been equipped with the wireless RS232 and video links what enabled reprogramming of hardware and software in the field and the control of the effectiveness of the implemented video processing algorithms. The summary of the FPGA resource utilization is presented in the Table 1.

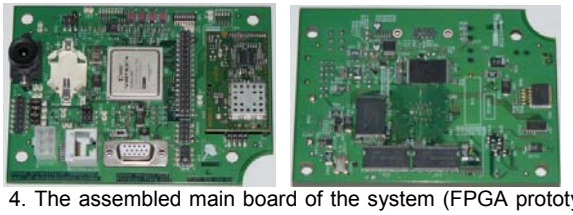

Fig. 4. The assembled main board of the system (FPGA prototype #2)

Fig. 5. The pictures of the assembled sensor nodes and one of them installed on the street lamp – pole (FPGA prototype #2)

Table 1. The resources used in the FPGA implementation with Virtex-4 XC4VLX60 (FPGA prototype #2)

Resource	Total used / Available
Flip Flops	10 325 / 53 248
LUTs (used as logic)	30 784 / 53 248
Total number of LUTs	31 676 / 53 248
Occupied Slices	19 220 / 26 624
18Kb Block RAMs	157 / 160

Asic Design And Verification

After a successful startup with the FPGA, the ASIC has been designed in 130nm UMC CMOS process and manufactured through Europractice (Fig. 6 and 7), using the RTL code from the FPGA prototype. Both FPGA and ASIC provide almost the same functionality. The design of ASIC has been made using Cadence SoC software with Faraday L130FSG (LP and HS) library of digital gates. The code used for FPGA prototype #2 has been adopted for ASIC realization. I/O blocks were inserted, memory blocks were generated (with Memaker software by Faraday Corp.) and inserted into VHDL code, what resulted in adding approx. 2000 lines of HDL code. The VHDL and Verilog code has been synthesized using Cadence RTL Compiler with clock gating optimization. Also DFT flip-flops and JTAG controller have been added to enable future tests. For the implementation, Cadence SOC Encounter GXL 6.2 has been used, with crosstalk and signal integrity analysis and power supply analysis (electromigration, IR drop). Before final ASIC fabrication, extensive checks were done: post synthesis and post implementation HDL model simulations with Cadence Ncsim tool, logic equivalence checks of pre and post synthesis and post implementation models using Cadence Conformal tool. The parameters of the designed ASIC are listed in Table 2. Comparing Tables 1 and 2, the large difference in the number of Flip Flops can be observed. The reason is that small memories and shift registers in FPGA are implemented using Look Up Tables (LUTs), while ASIC implementation uses FFs for that purpose. Moreover, in the FPGA, all the memory is composed of 18Kbit block memories, resulting in wasted bits. Each memory block used in ASIC is designed to exactly fit the required size.

The manufactured ASIC has been used to build the low-power version of the node shown in Fig. 7, which works with Li-Ion 3.7V 3.5Ah single cell rechargeable battery and can be supplied by a solar panel of area of 0.5m^2 (50W peak power).

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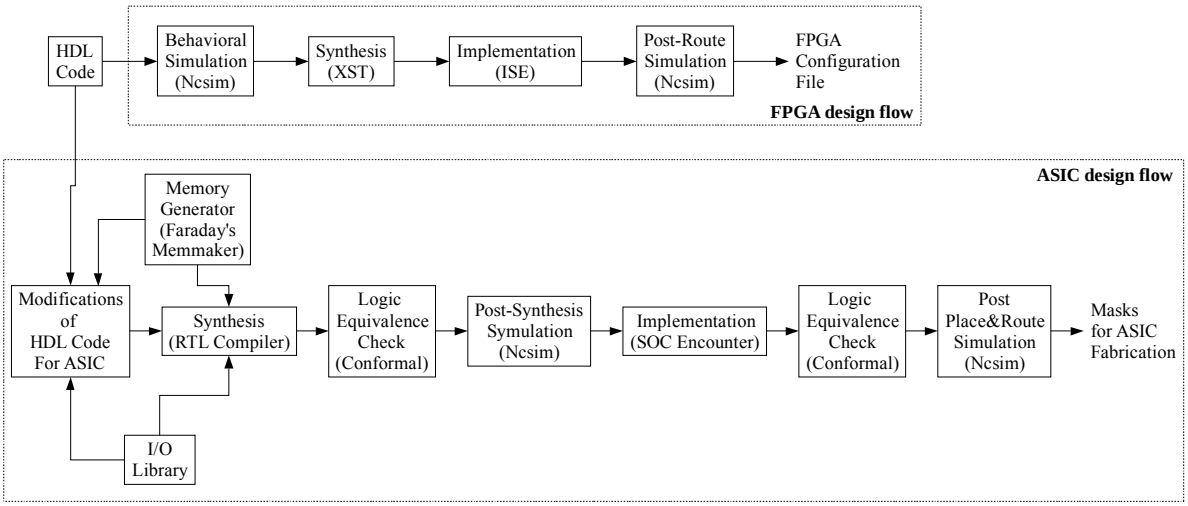

Fig. 6. Block diagrams of FPGA and ASIC design flows. The names of the tools used during the design are written in parentheses

Table 2. The resources used in the ASIC implementation using Faraday library and UMC130nm CMOS process

Resource	Total used
Flip Flops	18 478
Primitives (gates, buffers, flip flops, etc.)	549 062
Chip area	25mm^2
Memory blocks	75
Memory bits	1 661 952

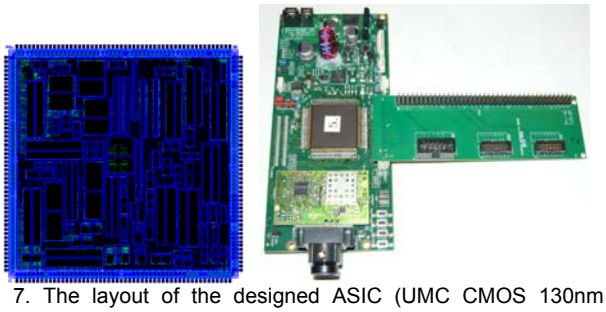

Fig. 7. The layout of the designed ASIC (UMC CMOS 130nm technology) and the picture of the assembled board with the connected additional service board

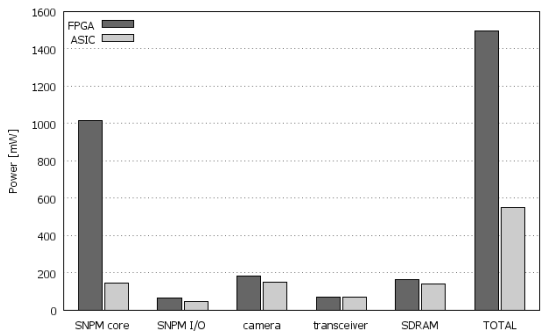

Fig. 8. Power consumed by the main blocks of the sensor network node prototypes during typical work (detecting traffic and exchanging data with 5 neighbors). FPGA prototype works with the following power supply voltages: 1.2 V and 2.5 V for the core, 3.3 V for SNPM I/O, camera and SDRAM and 3 V for the transceiver. ASIC prototype uses 1.2 V for the core, 3 V for all other blocks. The power losses at the power supply and battery charging circuitry are not included

The comparison of the power consumed by FPGA prototype #2 and the final ASIC is presented in Fig. 8. The total power of the whole system with the ASIC is about 3 times smaller than the FPGA realization. The power consumed by the ASIC itself is about 6 time smaller than the FPGA's power.

Conclusions

The paper presents the implementation process of the sensor network node using FPGA prototypes and the final CMOS UMC 130nm ASIC realization. The design of the described two FPGA prototypes took two years for three persons. The HDL code was then used to implement the ASIC. The FPGA-ASIC porting process took about four months for four persons. The FPGA prototyping offers the possibility of fast functional tests and gives the ability to make the necessary corrections before the final chip is designed and fabricated. It also offers the possibility to develop and test software before the final product is ready. This seems to be a vary good solution for SoC designs. On the other hand, the porting process requires additional effort, mainly due to the differences in IP cores available on both platforms, as well as different realizations of on-chip memories and I/O blocks.

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