

DIAGNOSIS OF FULLY DIFFERENTIAL CIRCUITS BASED ON A FAULT DICTIONARY IN POLAR COORDINATES IMPLEMENTED IN THE MICROCONTROLLER SYSTEMS

Wojciech Toczek Zbigniew Czaja

Gdansk University of Technology, Faculty of Electronics, Telecommunications and Informatics,
Department of Optoelectronics and Electronic Systems, Gdansk, Poland

Abstract

A new Built-In-Self-Test scheme for diagnosis of analog fully differential linear circuits embedded in a mixed-signal microsystem is presented. Only one testing frequency is used. During testing the magnitude and phase of the output differential voltage are measured. The fault detection and single fault localization procedure is based on the fault dictionary stored in the program memory of the microcontroller. The great advantage of the magnitude-phase measurement space is the shape of fault signature trajectories. In the polar coordinates trajectories have the shape of the segments of a circle or a line with simple analytical description. This implies that the dictionary has a very concise form. BIST can be realized by the internal resources of the microcontroller already existing in the tested system.

Keywords: BIST, fault diagnosis in fully differential circuits, fault dictionary, magnitude-phase measurement space

1. Introduction

Rapid changes in technology, shorter product lifecycles and increasing costs are driving the need for automated testing and diagnosis. The major test challenges are mainly due to embedded analog portions of the mixed-signal system [1]. Built-In-Self-Test (BIST) technique based on structural (fault-driven) testing is very attractive to solve the problems of testing embedded analog blocks. They reduce the test application time and the need of external testing by implementing test functions on a chip or on a board.

We assume that the architecture of the circuits under test (CUT) is fully differential. Such a solution has been very popular in the design of filters, A/D converters etc. because of many advantages. Due to the inherent redundancy within the circuit structure and symmetry, fully differential circuits are also easily testable.

Usually the BIST technique provides only fault detection capability [2,3,4,5,6]. In [7,8] an AC fault-based multifrequency test generation and fault diagnosis (detection, localization and identification) procedure is proposed. The test generation procedure finds a minimal set of test measures and a minimal

set of test frequencies, which achieve maximum fault coverage. The procedure for fault diagnosis corresponds to a pattern-matching approach, which is known as the “fault dictionary”. The fault-dictionary approach first determines the CUT responses that are likely to occur, given the anticipated faults. A list of fault/symptom pairs (encoded simulated circuit responses) makes up the fault dictionary. During testing, the measurement data are compared against the signatures from the fault dictionary and the data that best match the test circuit’s measurement data, indicate which component is faulty when a particular symptom is present. In [7] the fault dictionary containing a signature of the effects of each fault in the frequency domain is presented for the differential biquadrate filter, which requires 12 different frequencies to detect and distinguish: 30% deviations in each component, hard faults in each component and intermediate +100% and –50% deviations.

In the paper we consider a BIST scheme with functionality extended to localization of parametric faults of passive components with only one testing frequency, using very concise fault dictionary implemented in the microcontroller already existing in a mixed-signal tested system. The fault dictionary has the form of a family of fault signature trajectories in the measurement space.

The paper is organized as follows. In section 2, we present in details the design of the fault dictionary in the polar coordinates. In section 3, the measurement and diagnostic procedures based on microcontroller are presented. Experimental test results obtained from fully differential band-pass filter are described in section 4. Finally, section 5 concludes the paper.

2. The fault dictionary

The fault dictionary is built before the testing process by means of computer simulations of the CUT, under nominal and faulty conditions. Actually the fault dictionary is converted into the file with the full code of a program, compiled to a HEX file and placed in the program memory of the microcontroller in the In System Programming (ISP) mode. The ISP is the ability of programmable electronic chips (e.g. microcontrollers) to be programmed while installed in a complete system. With regard to the limited size of the microcontroller memory, the fault dictionary should have the smallest possible size. In order to fulfil this requirement we use the magnitude-phase measurement space in the polar coordinates.

2.1 Signature trajectories in the magnitude-phase measurement space

The presented method is suitable for a class of linear time-invariant systems, called minimum-phase networks which exhibit a unique gain-phase relationship. It is known that for the minimum phase class of networks the relations between the amplitude and phase functions in the complex plane is either a semi-infinite straight line or an arc of a circle with simple analytical description.



Parameter variations engender fault signature trajectories in the measurement space. In all examples we assume the continuous range of parameter variability from $0.1 \cdot p_{i\text{nom}}$ to $10 \cdot p_{i\text{nom}}$, ($p_{i\text{nom}}$ – the nominal value of the i -th component).

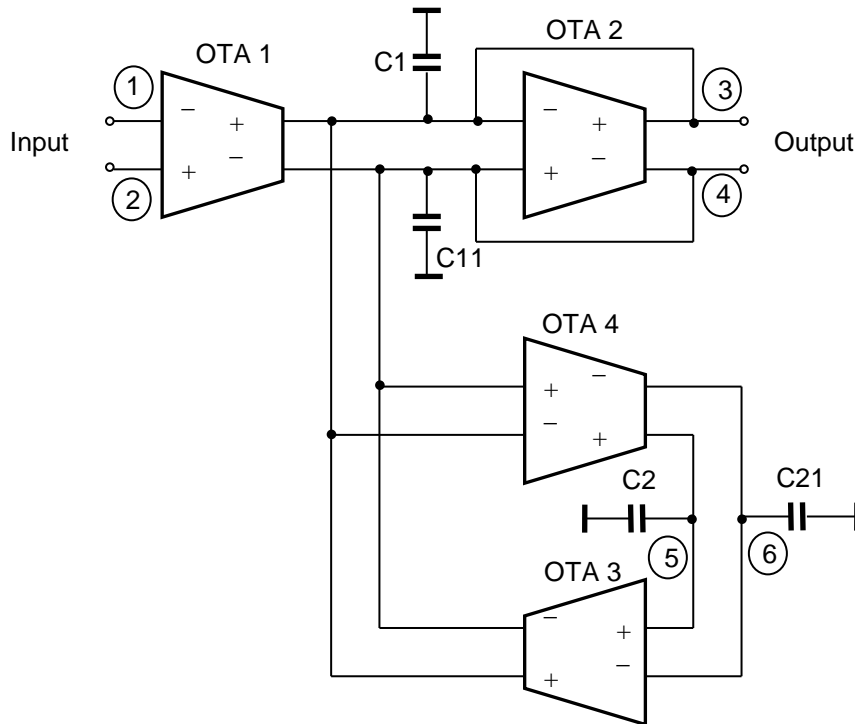


Fig. 1. Circuit under test – fully differential implementation of the OTA-C filter

As the first example let us consider the fully differential continuous-time transconductance-C (gm-C) filter which is based on the Tow-Thomas topology. Such filters have been widely used for several applications, e.g. digital video, RF/IF filters, etc. [9]. The filter consists of four operational transconductance amplifiers and four capacitors, as shown in Fig.1. For angular frequency normalized to 1, the nominal normalized component parameters are: capacitors $C_1 = C_{11} = C_2 = C_{12} = 2\text{ F}$, transconductances $gm_1 = gm_{11} = gm_2 = gm_{21} = gm_3 = gm_{31} = gm_4 = gm_{41} = 1\text{ S}$. We test the circuit by the differential mode excitation and measurement of the common voltage at test nodes. The Tow-Thomas filter has two outputs. The first one gives a lowpass response and the second one a bandpass response. The measured common mode output voltage is theoretically zero in the case of a fault-free (symmetrical) circuit under test and become non-zero if the symmetry is violated by a faulty component.

For fully differential circuits the magnitude-phase measurement space has central symmetry. All signature trajectories cross the origin. The number of trajectories depends on nodes chosen for differential voltage measurements. In the case of test nodes number 3 and 4 three trajectories appears in the measurement space (Fig. 2). The first trajectory belongs to components: $gm_1, gm_{11}, gm_2, gm_{21}$, the

second to C_{11} and gm_3 , the third to C_1 and gm_{31} . The rest of components, i.e. C_2 , C_{21} , gm_4 , gm_{41} cannot be tested from nodes 3 and 4. Choosing test nodes number 5 and 6 we obtain two trajectories (Fig. 3). The first belongs to components C_2 and gm_{41} , the second one to C_{21} and gm_4 . Hence, two measurements are necessary for testing the complete set of 12 components. Some trajectories superimpose each other, causing ambiguity. All 12 components are grouped in 5 sets each connected with one trajectory. Obviously, in the ambiguity group of components, only one is faulty, but we can't point which of them. Hence, the localization result contains a complete list of components belonging to the given ambiguity group.

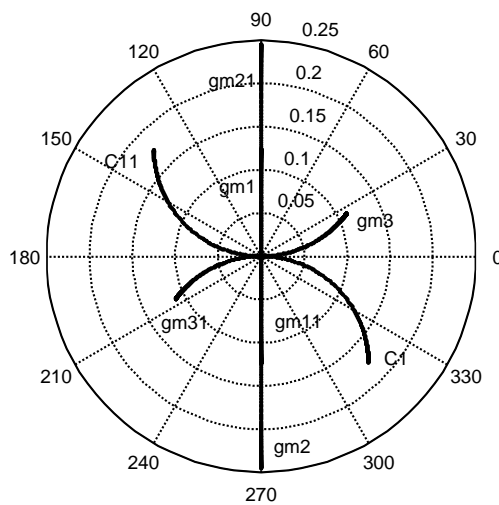


Fig. 2. Map of signature trajectories observed at nodes 3 and 4 of the OTA-C filter

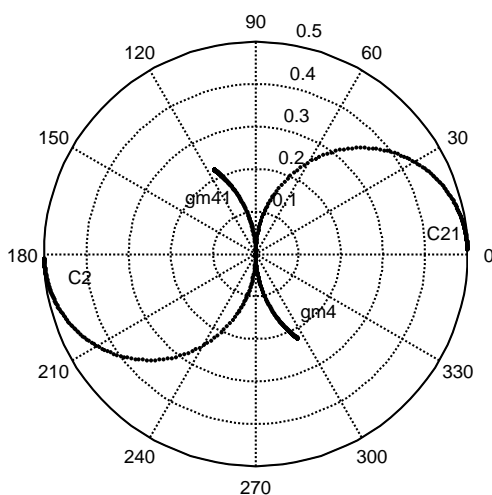


Fig. 3. Map of signature trajectories observed at nodes 5 and 6 of the OTA-C filter

As the second example, let us consider the fully differential Deliyannis-Friend band-pass filter (mounted on the circuit printed board), shown in Fig. 4, which is tested with the common-mode excitation at the reference input of the output common-mode voltage and measurement of the output differential voltage. The method is superior in test quality over the one that exploits a differential-mode excitation and gives result equivalent to testing the transfer function G_{DC} [10]. This function relates the output differential voltage to the input common-mode voltage [11]. In this case, the number of obtained trajectories is equivalent to the number of components (Fig. 5), which implies that all faulty components can be localized uniquely. We use only one testing frequency and only one pair of testing nodes for measurement. The testing frequency equivalent to the center frequency of the filter provides the best discrimination ability of faults in the measurement space because of the largest distances between trajectories [10]. Unfortunately there is also some form of ambiguity in this example created by points at which trajectories intersect.

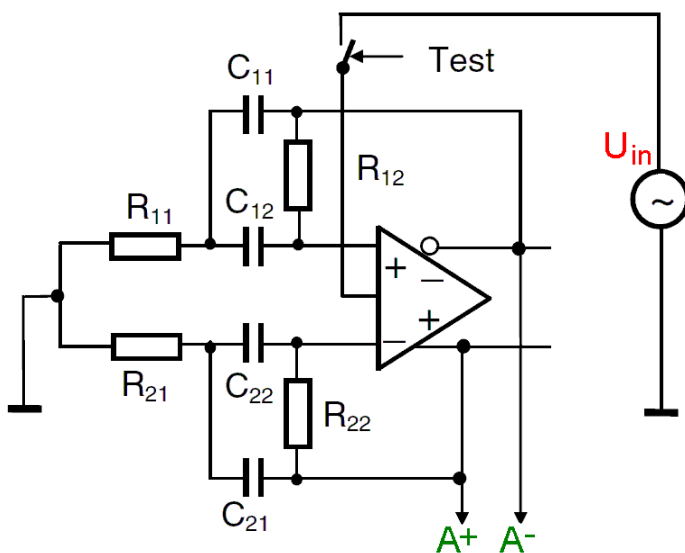


Fig. 4. Circuit under test – fully differential implementation of the band-pass Deliyannis-Friend filter

The fault dictionary contains descriptions of all I signature trajectories. In the case of the shape of a segment of a circle, the trajectory can be described by the magnitude A_i and the phase ϕ_i fulfilling

$$z = A_i \cdot \sin(\phi - \phi_i) \quad (1)$$

where (z, ϕ) are coordinates of the point in the polar coordinate system.

The values ϕ_i and A_i are determined from two points (ϕ_{i1}, A_{i1}) and (ϕ_{i2}, A_{i2}) generated for two values of the i -th component during simulation of the tested analog circuit.



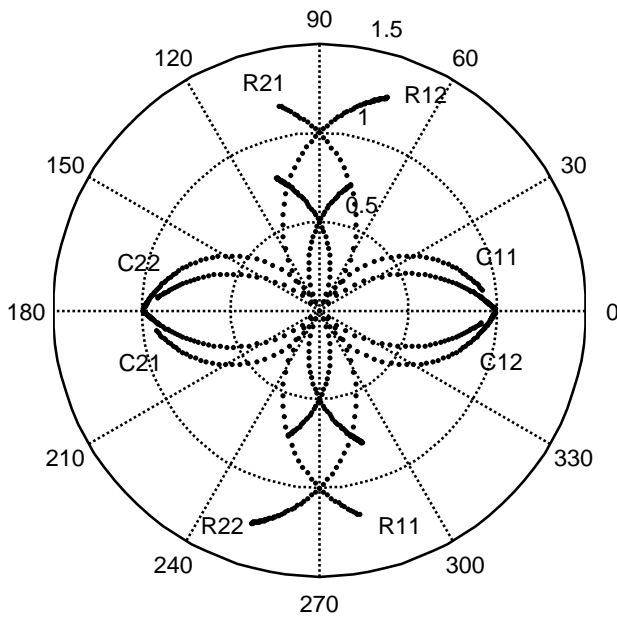


Fig. 5. Map of signature trajectories observed at nodes A^+ , A^- of the band-pass Deliyannis-Friend filter

Based on (1) and these points we can write the following relationships:

$$\begin{cases} A_{i1} = A_i \cdot \sin(\phi_{i1} - \phi_i) \\ A_{i2} = A_i \cdot \sin(\phi_{i2} - \phi_i) \end{cases} \quad (2)$$

Eq. (2) can be write out to the form:

$$\begin{cases} A_{i1} = \sin(\phi_{i1}) \cdot A_i \cdot \cos(\phi_i) - \cos(\phi_{i1}) \cdot A_i \cdot \sin(\phi_i) \\ A_{i2} = \sin(\phi_{i2}) \cdot A_i \cdot \cos(\phi_i) - \cos(\phi_{i2}) \cdot A_i \cdot \sin(\phi_i) \end{cases} \quad (3)$$

Setting

$$v_i = A_i \cdot \cos(\phi_i), \quad w_i = A_i \cdot \sin(\phi_i) \quad (4)$$

after transformations we obtain the following equations for values of v_i and w_i :

$$v_i = \frac{A_{i1} \cdot \cos(\phi_{i2}) - A_{i2} \cdot \cos(\phi_{i1})}{\sin(\phi_{i1}) \cdot \cos(\phi_{i2}) - \cos(\phi_{i1}) \cdot \sin(\phi_{i2})} \quad (5a)$$

$$w_i = \frac{A_{i2} \cdot \sin(\phi_{i1}) - A_{i1} \cdot \sin(\phi_{i2})}{\sin(\phi_{i1}) \cdot \cos(\phi_{i2}) - \cos(\phi_{i1}) \cdot \sin(\phi_{i2})} \quad (5b)$$

From (4) we obtain

$$A_i = \frac{v_i}{\cos(\phi_i)}, \quad \phi_i = \arctan\left(\frac{w_i}{v_i}\right) \quad (6)$$

From (5) and (6) we have the formulae for the magnitude A_i and the phase ϕ_i describing the i -th trajectory:

$$A_i = \frac{A_{i2} \cdot \sin(\phi_{i1}) - A_{i1} \cdot \sin(\phi_{i2})}{\cos(\phi_i) \cdot (\sin(\phi_{i1}) \cdot \cos(\phi_{i2}) - \cos(\phi_{i1}) \cdot \sin(\phi_{i2}))} \quad (7a)$$

$$\phi_i = \arctan\left(\frac{A_{i2} \cdot \sin(\phi_{i1}) - A_{i1} \cdot \sin(\phi_{i2})}{A_{i1} \cdot \cos(\phi_{i2}) - A_{i2} \cdot \cos(\phi_{i1})}\right) \quad (7b)$$

The magnitude A_i and the phase ϕ_i can be represented by values v_i and w_i (see (6)). Thus based on this fact we eliminate expressions with the angle ϕ_i from further analysis, which considerably simplifies calculations executed during the diagnosis process. Hence, v_i , w_i are indirect parameters describing the i -th signature trajectory.

2.2. Determination of the value of the fault detection threshold U_{A_th}

Due to manufacturing tolerances, the responses of the CUT show statistical distribution and a residual output voltage is generated even when no faults occur. To separate the faulty circuits from the fault-free ones it is necessary to apply a selected properly detection threshold to differentiate between faulty and fault-free responses.

In [10] a probabilistic model of performances of the CUT has been derived. The probability distribution function (pdf) of magnitude z of the residual voltage has the form:

$$f_z(z) = \frac{z}{\sigma_x \sigma_y \sqrt{1-r^2}} e^{-\frac{z^2}{2(1-r^2)}} I_0\left(\frac{z^2}{2(1-r^2)} \sqrt{b^2 + c^2}\right) \quad (8)$$

where x , y are the real and imaginary parts of the residual voltage, σ_x , σ_y are the respective standard

deviations, r is the correlation coefficient between x and y , $a = \frac{\sigma_x^2 + \sigma_y^2}{2\sigma_x^2 \sigma_y^2}$, $b = \frac{\sigma_x^2 - \sigma_y^2}{2\sigma_x^2 \sigma_y^2}$, $c = \frac{r}{\sigma_x \sigma_y}$,

I_0 – the modified Bessel function of the first kind and zero-th order.

The parameters of distribution (8): σ_x , σ_y , r can be evaluated using Taylor series expansion of the network function of interest around the point that represents the mean values of components and truncating the Taylor series after the first partial derivatives [10]. For example, assuming 1% component



tolerances with uniform distribution and frequency of testing signal equivalent to the center of the frequency response of the filter from Fig. 4, we obtain: $\sigma_x = 8.55 \text{ mV}$, $\sigma_y = 10.77 \text{ mV}$ and $r = 0$.

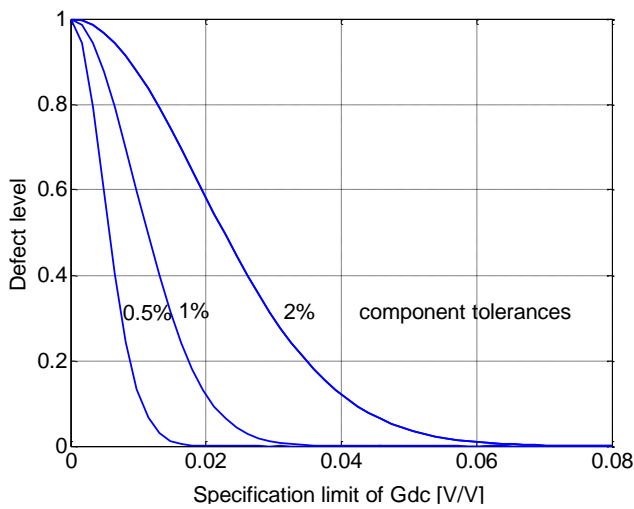


Fig. 6. The manufacturing process induced defect level versus specification limit of G_{DC} and component tolerances

The pdf (8) was applied for estimation of the manufacturing process induced defect level (1-yield), i.e., the likelihood of the CUT exceeding a given specification limit due to manufacturing tolerances. An approach to estimate the probability of a specification violation is to integrate the tail of pdf (8) outside the specification limit of parameter G_{DC} as follows:

$$1 - Y(G_{DCspec}) = \int_{G_{DCspec}}^{+\infty} f_Z(z) dz \quad (9)$$

The plots of calculated tail probability due to component tolerances from the range of 0,5% - 2%, versus specification limits of G_{DC} , are presented in Fig. 6. For tight specification limit, the number of circuits failing to meet this limit is high, resulting in a low yield. For wider specification limit, the number of failing circuits decreases, which results in higher yield but the less competitive the product in the market. For specification limit $G_{DCspec} = 0.044 \text{ V/V}$ the integral (9) evaluates to $1 - Y(G_{DCspec}) = 77 \text{ ppm}$.

The test is subject to measurement uncertainty that causes the risk of taking the wrong decision, which results in higher defect level. The test related defect level, is the probability of passing a defective device to the customer. In order to guarantee low test related defect level, the guard-band that needs to account the variation of the measurement result induced by noise, must be applied during the fault detection threshold U_{A_th} determination. Tightening the fault detection threshold will lead to lower the defect level but also to higher the test yield loss (Fig. 7). The data for analysis was obtained from a probability

framework for evaluation of test quality matrix presented in [10], which is based on the probabilistic model of performances of the CUT (8) and a probabilistic model for measurement process proposed by Rossi [12]. Many authors suggest that the low defect level is more important than the low yield loss because it is at least ten times more expensive to ship a faulty circuit than to discard a good one [13].

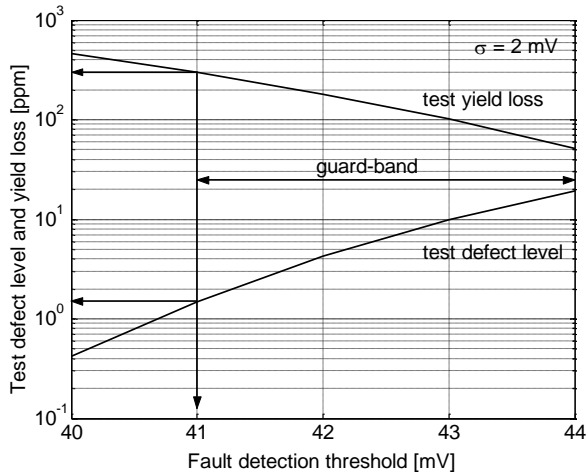


Fig. 7. Test defect level and yield loss versus the setting of the fault detection threshold (for the standard deviation of measurements $\sigma = 2$ mV)

For 1 V amplitude of the testing signal and the assumed standard deviation of measurements $\sigma = 2$ mV, the fault detection threshold U_{A_th} should be set at 41 mV, to obtain at least 3 mV guard band. This guard-band reduces the test related defect level to 2 – 3 ppm, and increases the test yield loss to 300 ppm.

2.3. Decision boundaries

Fault localization requires computing the decision boundaries for each faulty component. The third parameter η_i , describing together with v_i, w_i , the i -th signature trajectory, was used. It describes the average width of the i -th belt composed of trajectories distributed by tolerances. A value of the parameter η_i depends on tolerance values of circuit components. E.g. if values of the component tolerance increase, the widths of all trajectories also increase. Hence, the following algorithm of the η_i coefficient determination is proposed:

- In the first step of the algorithm M points, with coordinates (v_i^m, w_i^m) $m = 1, \dots, M$ representing two end areas of the i -th localization belt in the indirect parameters space, are generated using the Monte

Carlo method. The first end area $\{(V_{i,0.1}^m, w_{i,0.1}^m)\}_{m=1,\dots,M}$ is generated for the $0.1 \cdot p_{i\text{ nom}}$ value of the i -th component, the second one $\{(V_{i,10}^m, w_{i,10}^m)\}_{m=1,\dots,M}$ for the $10 \cdot p_{i\text{ nom}}$ component value.

- Next, for these areas the following parameters are defined and determined:

$$\eta_i^{0.1} = \max\left\{\left|\max_{m=1,\dots,M}\{V_{i,0.1}^m\} - \min_{m=1,\dots,M}\{V_{i,0.1}^m\}\right|, \left|\max_{m=1,\dots,M}\{w_{i,0.1}^m\} - \min_{m=1,\dots,M}\{w_{i,0.1}^m\}\right|\right\} \quad (10a)$$

$$\eta_i^{10} = \max\left\{\left|\max_{m=1,\dots,M}\{V_{i,10}^m\} - \min_{m=1,\dots,M}\{V_{i,10}^m\}\right|, \left|\max_{m=1,\dots,M}\{w_{i,10}^m\} - \min_{m=1,\dots,M}\{w_{i,10}^m\}\right|\right\} \quad (10b)$$

- Finally, we chose the maximum value which will be used as the width of the i -th trajectory family:

$$\eta_i = \max\{\eta_i^{0.1}, \eta_i^{10}\} \quad (11)$$

The full fault dictionary has the following very compressive form $\{U_{A_th}, \{v_i, w_i, \eta_i\}_{i=1,\dots,I}\}$.

The detection part of the fault dictionary for the circuit from Fig. 4 consists of only one element $U_{A_th} = 8 [\times 5 \text{ mV}]$. The localization part is presented in Table 1.

Table 1. The fault dictionary for the band-pass Deliyannis-Friend filter from Fig. 4

Faulty component	v_i [$\times 2.5 \text{ mV}$]	w_i [$\times 2.5 \text{ mV}$]	η_i [$\times 2.5 \text{ mV}$]
R ₁₁	-400	400	12
R ₁₂	404	400	12
R ₂₁	400	-400	12
R ₂₂	-404	-400	12
C ₁₂	200	400	8
C ₁₁	-200	400	8
C ₂₂	-200	-400	12
C ₂₁	200	-400	8

The parameters U_{A_th} , v_i , w_i , η_i , are converted to the form compatible with the form of direct measurement result of the ADC. The microcontroller operates on integer values, and what it is worth to notice, the ADC results are directly used by diagnosis procedures, what simplifies calculations made during the fault detection and localization. Hence, the fault dictionary has the size $F \cdot (I \cdot 3 + 1)$ bytes. When $I = 8$, $F = 2$ (F – the number of bytes for a given data type – we assumed an integer type of our data which is represented by two bytes) it is very small (50 bytes) in relation to the size of the program memory of a typical 8-bit microcontroller (e.g. ATmega16 has 16 kB of FLASH memory). Thanks to

this, the fault dictionary occupies only about 0.3% of the program memory space for typical small microcontrollers with 16 kB of FLASH memory.

3. Self-testing

Figure 8 shows the electronic system working in the self testing mode of its embedded analog part. The self-testing procedure is run by the control unit (implemented in the microcontroller). The control unit together with its internal measurement devices (ADCs, timers) creates the reconfigurable BIST like in [14, 15]. The self testing procedure consists of two stages: the measurement procedure using the internal ADC, triggered by the internal timer of the microcontroller to measure the magnitude and the phase of the differential output voltage of the analog part, and the fault detection and localization procedure, where the microcontroller, based on the fault dictionary and the measurement results, carries out fault detection, and when a fault is detected, its localization.

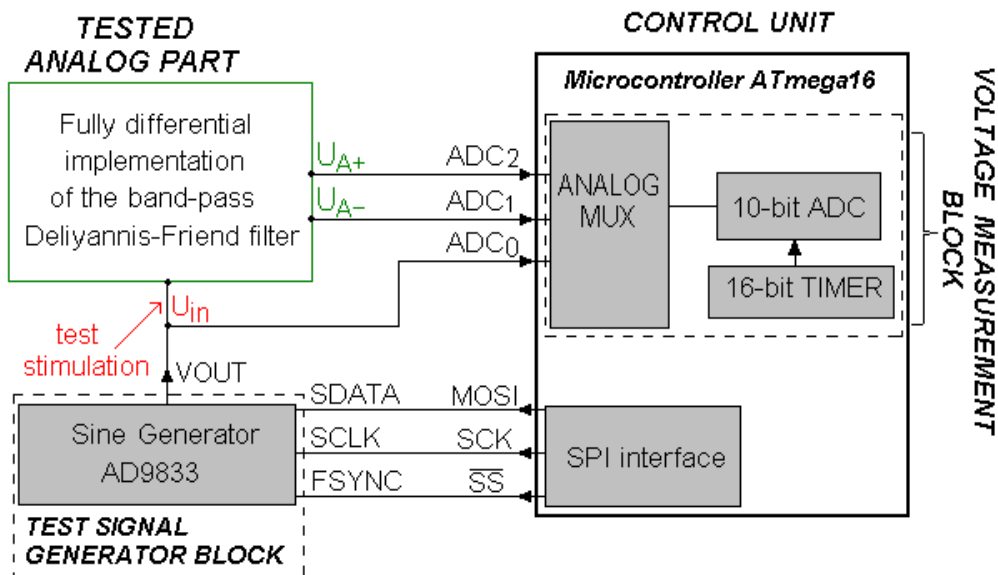


Fig. 8. Example of the electronic microsystem in the self-testing mode of the analog embedded part

3.1. The measurement procedure

The tested circuit is stimulated by a programmable sinusoidal generator. The input signal u_{in} is sampled by the ADC in moments established by the 16-bit Timer 1 of the microcontroller [16] similarly as in [17]. In the same way the output differential signal u_A is also sampled (Fig. 9). But, in this case the ADC works in the Differential Gain Channels (DGC) mode. Hardware possibility of sampling of differential signals by the ADC significantly simplifies the BIST structure and the measurement algorithm, what is an advantage of this solution.

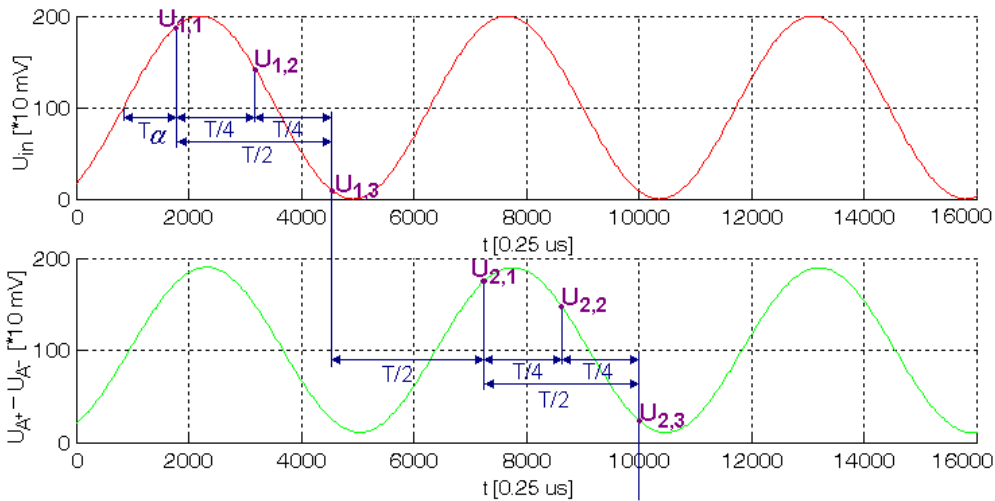


Fig. 9. Timings of the measured signals during the self-testing procedure

It is seen from Fig. 9, that each signal is sampled three times, where time distances between samples are set to one fourth of the input signal period T . Time distances between samples for subsequent signals are equal to a half of the period. We can say that it allows to sample all signals at the same moments in relation to beginning of sampling, because sampling of the next signal is shifted by the period. Sampling of the input signal u_{in} is needed to establish a random shift time T_α of the sampling series. The third sample of each signal is used for elimination of the voltage offset. The first and second samples of the output differential signal u_A are used to calculate its real x_A and imaginary y_A parts and its magnitude U_A .

The idea of the measurement procedure is as follows. We know the values of the amplitude U_1 and the period T of the stimulant signal u_{in} . We measure voltage samples $u_{1,1}$, $u_{1,2}$, $u_{1,3}$ of the u_{in} input signal and voltage samples $u_{2,1}$, $u_{2,2}$, $u_{2,3}$ of the u_A output signal in the way shown in Fig. 9.

Next, we calculate and eliminate from all samples the offset $u_{n,offset}$:

$$u_{n,offset} = \frac{u_{n,1} + u_{n,3}}{2}, \quad n = 1, 2 \quad (12)$$

We start to sample the sinusoidal signal in a random moment moving, in relation to beginning of this signal, about a random shift time T_α as shown in Fig. 9. Thus we have to eliminate this unknown time, that is we calculate a correction following from the time T_α expressed as sine and cosine of the angle

$$\alpha = \frac{2\pi}{T} T_\alpha :$$

$$\sin \alpha = \frac{u_{1,1}}{U_1} \quad \cos \alpha = \frac{u_{1,2}}{U_1} \quad (13)$$

We assume that the output differential signal u_A has the form $u_A = x_A + jy_A$. The voltage samples are described by the equations:

$$\begin{cases} u_{2,1} = U_A \sin(\alpha + \phi_A) \\ u_{2,2} = U_A \sin(\alpha + \phi_A + \frac{\pi}{2}) \end{cases} \quad (14)$$

where ϕ_A is the phase of the output differential signal.

Eq. (14) can be write out to the form:

$$\begin{cases} u_{2,1} = U_A \cdot \sin(\alpha) \cdot \cos(\phi_A) + U_A \cdot \cos(\alpha) \cdot \sin(\phi_A) \\ u_{2,2} = U_A \cdot \cos(\alpha) \cdot \cos(\phi_A) - U_A \cdot \sin(\alpha) \cdot \sin(\phi_A) \end{cases} \quad (15)$$

Setting

$$x_A = U_A \cdot \cos(\phi_A), \quad y_A = U_A \cdot \sin(\phi_A) \quad (16)$$

and putting them to (15) we obtain the equations:

$$\begin{cases} u_{2,1} = x_A \cdot \sin(\alpha) + y_A \cdot \cos(\alpha) \\ u_{2,2} = x_A \cdot \cos(\alpha) - y_A \cdot \sin(\alpha) \end{cases} \quad (17)$$

Determining x_A and y_A we have:

$$\begin{cases} x_A = u_{2,1} \cdot \sin(\alpha) + u_{2,2} \cdot \cos(\alpha) \\ y_A = u_{2,1} \cdot \cos(\alpha) - u_{2,2} \cdot \sin(\alpha) \end{cases} \quad (18)$$

Next, we put (13) to (18), what after transformations gives the following formulae on the real x_A and imaginary y_A parts, the magnitude U_A and its square of the output differential signal:

$$\begin{cases} x_A = (u_{2,1} \cdot u_{1,1} + u_{2,2} \cdot u_{1,2}) \cdot \frac{1}{U_1} \\ y_A = (u_{2,1} \cdot u_{1,2} - u_{2,2} \cdot u_{1,1}) \cdot \frac{1}{U_1} \\ U_{A_square} = x_A \cdot x_A + y_A \cdot y_A \\ U_A = \sqrt{U_{A_square}} \end{cases} \quad (19)$$

Magnitude U_1 is constant and known, what considerably simplifies calculations of the values x_A and y_A . It follows from the fact, that calculations base only on addition, subtraction and multiplication operators.

Hence, the microcontroller proceeding according to the measurement procedure whose algorithm is shown in Fig. 10, measures three voltage samples of the stimulus and the output differential signal, and next calculates all parameters of the output differential signal based on (19).

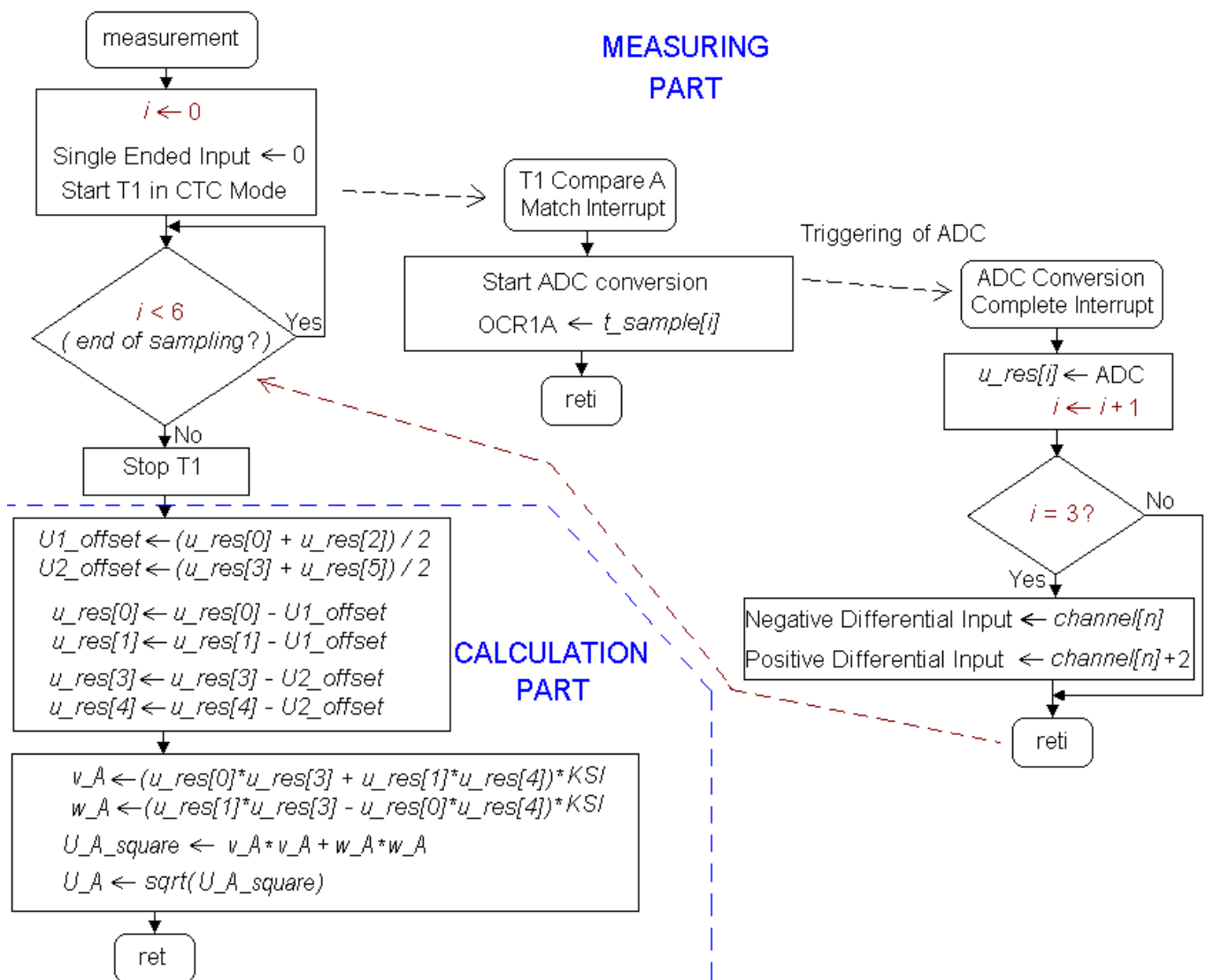


Fig. 10. The algorithm of the measurement procedure

The algorithm of the measurement procedure consists of two parts (Fig. 10). The first part is responsible for control of the measurement. The main function starts the timer and waits for the end of sampling, that is it waits for measurement of six voltage samples. The interrupt service of the timer starts the ADC conversion and actualizes the counting time between next samples. The interrupt service of the ADC conversion complete saves the voltage samples and changes the channel of the analog multiplexer. The calculation part computes the magnitude, its square and the real and imaginary parts of the output differential signal according to (19).

3.2. Fault diagnosis procedure

The purpose of fault diagnosis is fault detection and fault localization. The fault *detection* step is very simple and it bases on the test if the measured magnitude of the output differential signal U_A is smaller than the value of the threshold U_{A_th} .

Thus, if the condition $U_A \leq U_{A_th}$ is fulfilled the detection function returns 0, what means that the tested fault circuit is fault free (Listing. 1). Else it returns the MAX value, what calls the localization functions.

```
uint8_t detection(void)
{
    if(U_A < U_th) return(0);
    else return(MAX);
}
```

Listing 1. The code of the fault detection function

In the *localization* step for all I components the localization condition is tested. Generally this condition has the form:

$$|U_A - A_i \cdot \sin(\phi_A - \phi_i)| \leq \eta_i \quad (20)$$

which can be write out to the form:

$$|U_A - A_i \cdot \cos(\phi_i) \cdot \sin(\phi_A) - A_i \cdot \sin(\phi_i) \cdot \cos(\phi_A)| \leq \eta_i \quad (21)$$

because of (4), the (21) can be presented in the form:

$$|U_A - v_i \cdot \sin(\phi_A) - w_i \cdot \cos(\phi_A)| \leq \eta_i \quad (22)$$

To eliminate the expression with the phase ϕ_i , we multiply the inequality (22) by the magnitude U_A :

$$|U_{A_square} - v_i \cdot U_A \cdot \sin(\phi_A) + w_i \cdot U_A \cdot \cos(\phi_A)| \leq \eta_i \cdot U_A \quad (23)$$

Putting (16) to (23) we obtain the final localization condition:

$$|U_{A_square} - v_i \cdot y_A + w_i \cdot x_A| \leq \eta_i \cdot U_A \quad (24)$$

where: v_i, w_i, η_i – values describing the i -th localization belt.

The localization function (Listing 2) calculates and tests the localization condition (24) for all I components, and if for given i -th component this condition is fulfilled, it sets the i -th bit in the *fault_i*

variable. If any bit in the *fault_i* variable isn't set (*fault_i* = 0), that is the localization condition isn't fulfilled for any component in spite that the circuit is faulty, it means that there are multiple faults what is signaled by the proper message.

```
uint8_t localization(void)
{
    uint8_t i, fault_i;
    int16_t left, right;
    fault_i = MAX;
    for(i=0; i<I; i++)
    {
        left = U_A_square - (v_i[i]*y_A) + (w_i[i]*x_A);
        right = ni_i[i]*U_A;
        if(left < right)
        {
            fault_i |= (0x01 <<i);
        }
    }
    return(fault_i);
}
```

Listing 2. The code of the fault localization function

The control unit according to the fault diagnosis result, obtained by the detection and localization procedures, can run a definite alarm and it can send the results via any wired or wireless interface to the main computer.

One should underline the fact that these self-testing procedures of analog parts of the electronic embedded systems should be treated as part of full self-testing of this system, where the software, memories, the microprocessor core, digital circuits and remaining important components of the system are tested. Hence, self-testing procedures of analog circuits and the fault dictionary were elaborated with regard to minimal occupation of the program memory space of the control unit and minimal requirement on computing power.



4. Experimental verification

The diagnosis method was experimentally verified for the example of the band-pass Deliyannis-Friend filter (Fig. 4). The nominal values for R_{11} , R_{12} , R_{21} , R_{22} are [10 k Ω , 46711 Ω , 10 k Ω , 46711 Ω], respectively, all the capacitors have the same value C_{11} - C_{22} = 10 nF. The filter was realized on the basis of the Texas Instruments THS 4131 op-amp.

The stimulating sine wave was applied with a frequency 736.4 Hz an amplitude equal to $V_I = 1$ V. The tester was implemented in the 8-bit microcontroller Atmega16, which has a rich set of multifunctional and flexible peripheral devices, e.g. two 8-bit timers/counters, one 16-bit timer counter, 10-bit SAR-type ADC with a sample and hold circuit. The microcontroller works with a 4 MHz quartz crystal oscillator. The Timer 1 is clocked directly by the system clock ($t_{CLK} = 0.25$ μ s). It determines interval times $T = 1414.5$ μ s (a value 5658 loaded to Timer 1) and $T/2 = 707.25$ μ s (a value 2829) and $T/4 = 353.5$ μ s (a value 1414) of the ADC triggering. The 10-bit ADC has the following configuration: the voltage reference is set to V_{CC} , the result is right adjusted and the ADC is auto triggered by the interrupt from Timer 1.

Different soft faults of each passive p_i -component were physically entered to the circuit under test and diagnosed on the level of fault detection and localization. Measurements were carried out for element change in the range from 0.1 $p_{i\ nom}$ to 10 $p_{i\ nom}$. The following values were assumed for R_{11} and R_{21} {1, 2, 3, 4, 6, 7, 8, 9, 10, 11, 12, 20, 50, 100} * 1 k Ω , for R_{12} and R_{22} {5, 10, 20, 30, 40, 45, 50, 55, 60, 80, 100} * 1 k Ω , and for all capacitors {2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 15, 20, 50, 100} * 1 nF.

Localization results of tested components are shown in a graphical way in Fig. 11. The belts represent family of signature trajectories (with component tolerances) and single symbols represent the measurement results (measurement points). Correct fault location implies matching the measurement result with a certain trajectory. An example of experimental results is shown in Tables 2 and 3. Table 2 shows fault localization results for resistors and Table 3 fault localization results for capacitors. Points at which trajectories intersect cause ambiguity. In the ambiguity group of components, we can't point which of them is faulty. Hence, the localization result contains a complete list of components belonging to the given ambiguity group. It is seen from Fig. 11 and from Tables 2 and 3 that the diagnosis method for all assumed parameter deviations gives correct results of fault localization.

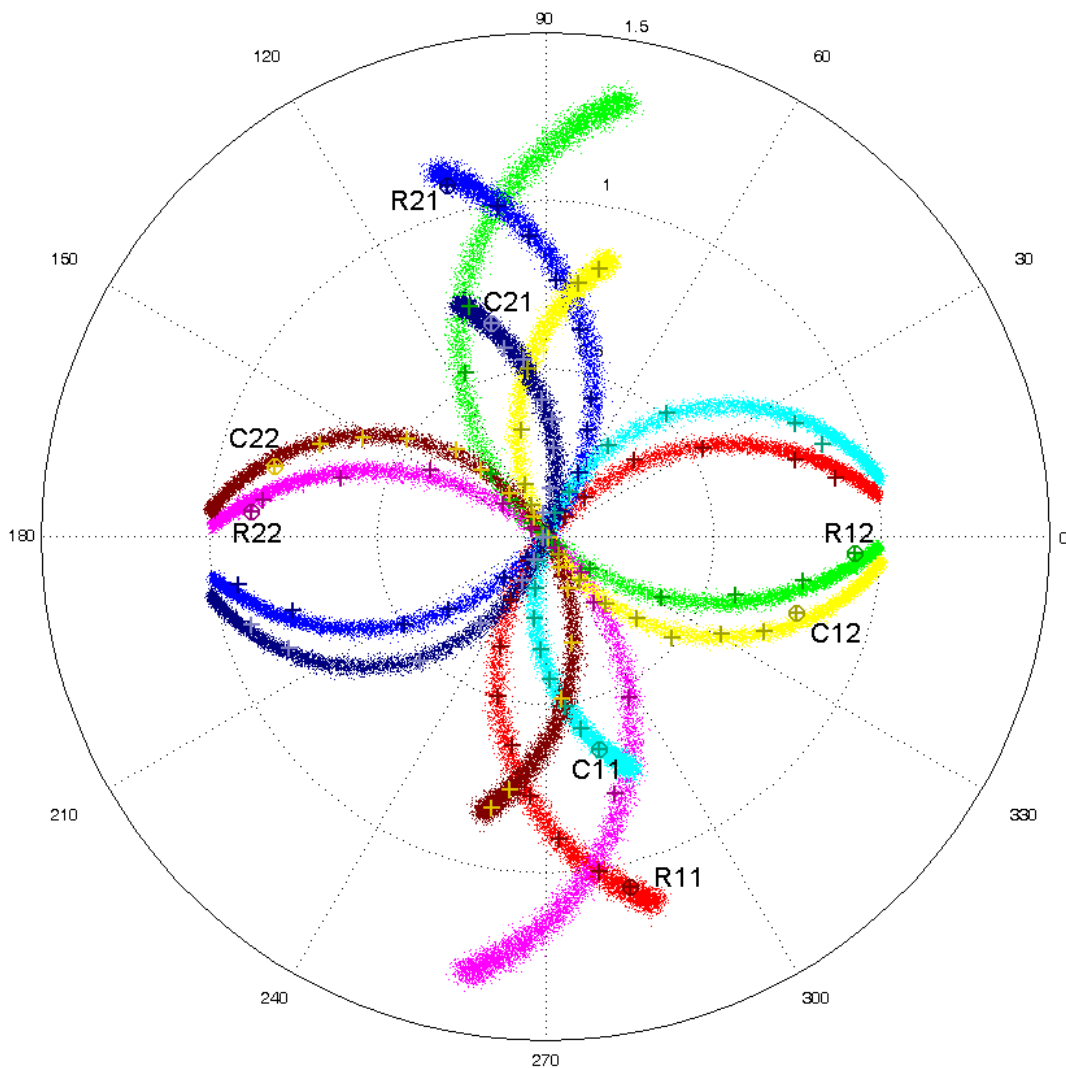


Fig. 11. Map of signature trajectories for passive components of the Deliyannis-Friend filter together with measurement results

Table 2. Fault localization results for resistors

Faulty component	R ₁₁	R ₂₁	Faulty component	R ₁₂	R ₂₂
Value (kΩ)	Diagnosis		Value (kΩ)	Diagnosis	
1	R ₁₁	R ₂₁	5	R ₁₂	R ₂₂
2	R ₁₁	R ₂₁ , R ₁₂	10	R ₁₂	R ₂₂
3	R ₁₁	R ₂₁	20	R ₁₂	R ₂₂
4	R ₁₁	R ₂₁	30	R ₁₂	R ₂₂
6	R ₁₁	R ₂₁	40	R ₁₂	R ₂₂
7	R ₁₁	R ₂₁	45	R ₁₂ , R ₂₂ , C ₁₂ , C ₂₂	R ₂₂ , R ₁₂ , C ₁₂ , C ₂₂
8	R ₁₁ , C ₂₁	R ₂₁ , C ₁₁	46	fault free	fault free
9	R ₁₁ , C ₂₁ , R ₂₁	R ₂₁ , C ₁₁ , R ₁₁ , C ₂₁	47	fault free	fault free
10	fault free	fault free	48	fault free	fault free
11	R ₁₁ , R ₂₁	R ₂₁ , R ₁₁ , C ₂₁	50	R ₁₂ , R ₂₂ , C ₁₂ , C ₂₂	R ₂₂ , R ₁₂ , C ₁₂
12	R ₁₁	R ₂₁	55	R ₁₂ , C ₂₂ , R ₂₂	R ₂₂ , C ₁₂
20	R ₁₁	R ₂₁	60	R ₁₂ , C ₂₂	R ₂₂
50	R ₁₁	R ₂₁	80	R ₁₂	R ₂₂
100	R ₁₁	R ₂₁	100	R ₁₂ , C ₂₁	R ₂₂

Table 3. Fault localization results for capacitors

Faulty component	C_{11}	C_{12}	C_{21}	C_{22}
Value (k Ω)	Diagnosis			
2	C_{11}	C_{12}	C_{21}	C_{22}
3	C_{11}	C_{12}	C_{21}	C_{22}
4	C_{11}, C_{22}	C_{12}	C_{21}	C_{22}
5	C_{11}	C_{12}	C_{21}	C_{22}
6	C_{11}	C_{12}	C_{21}	C_{22}
7	C_{11}	C_{12}	C_{21}	C_{22}
8	C_{11}	C_{12}, R_{22}	C_{21}	C_{22}, R_{21}
9	$C_{11}, R_{21}, C_{21}, R_{11}$	$C_{12}, C_{22}, R_{22}, R_{12}$	$C_{21}, R_{11}, C_{11}, R_{21}$	$C_{22}, R_{21}, C_{12}, R_{22}$
10	fault free	fault free	fault free	fault free
11	$C_{11}, R_{21}, C_{21}, R_{11}$	C_{12}, C_{22}, R_{12}	$C_{21}, R_{21}, R_{11}, C_{11}$	$C_{22}, R_{21}, R_{22}, C_{12}$
12	C_{11}, R_{21}	C_{12}	C_{21}, R_{11}	C_{22}
15	C_{11}	C_{12}	C_{21}	C_{22}
20	C_{11}	C_{12}	C_{21}	C_{22}, C_{11}
50	C_{11}	C_{12}	C_{21}	C_{22}
100	C_{11}	C_{12}	C_{21}	C_{22}

5. Conclusions

In the paper, the BIST scheme for a fully differential analog part of an electronic embedded system covering circuit measurement and fault diagnosis is presented. The diagnosis procedure consists of two steps. In the first step the self-test (fault detection) is performed. In the second step localization of single fault of passive components is made using fault dictionary approach in the magnitude-phase measurement space.

It has been shown on the examples of the fully differential circuits that the fault signature trajectories in measurement space have the shape of a line segment or the segment of a circle, crossing the origin. Each trajectory can be represented by only three parameters. Hence, the fault dictionary is easily designed and has a very concise form. The magnitude-phase measurement space is very attractive for fault diagnosis procedures based on dictionary approach, it is both highly discriminative and low dimensional.

To minimize the probability of an incorrect test decision in the first step due to manufacturing tolerances and measurement uncertainty, the fault detection threshold has been thoroughly chosen by analysis with the aid of a probabilistic model of the CUT performances.

The major advantages of the proposition are: computational simplicity, fault localization with only one testing frequency. The BIST is configured from the internal resources of the microcontroller already existing in the tested system. The results of fault localization can also be used in the process of the on-chip tuning of the OTA filters, which is the most effective way to overcome fabrication tolerances, component nonidealities, aging, and changing operating conditions such as temperature [18].

References

- [1] Huertas JL. Test and Design-for-Testability in Mixed-Signal Integrated Circuits. Kluwer Academic Publishers: Boston; 2004.
- [2] Francesconi F, Liberali V, Lubaszewski M, Mir S. Design of high-performance band-pass sigma-delta modulator with concurrent error detection, ICECS'96, p. 1202-05.
- [3] Harjani R, Vinnakota B. Analog Circuit Observer Blocks, IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, 1997; 44:154-63.
- [4] Lubaszewski M, Mir S, Kolarik V, Nielsen C, Courtois B. Design of Self-Checking Fully Differential Circuits and Boards. IEEE Transactions on Very Large Scale Integration (VLSI) Systems; 2000; 8:113-27.
- [5] Stratigopoulos HD, Makris Y. An Adaptive Checker for the Fully Differential Analog Code, IEEE Journal of Solid-State Circuits, 2006, 41:1421-29.
- [6] Stessman NJ, Vinnakota B, Harjani R. System-Level Design for Test of Fully Differential Analog Circuits, IEEE Journal of Solid-State Circuits, 1996; 31:1526-34
- [7] Mir S, Lubaszewski M, Courtois B. Fault-Based ATPG for Linear Analog Circuits with Minimal Size Multifrequency Test Sets, Journal of Electronic Testing: Theory and Applications, 1996; 9:43-57.
- [8] Mir S, Lubaszewski M, Courtois B. Unified Build-In Self-Test for fully Differential Analog Circuits, Journal of Electronic Testing: Theory and Applications, 1996 ; 9:135-151.
- [9] Cortes F. P., Bampi E. F. S. Analysis and design of amplifiers and comparators in CMOS 0.35 μm technology, Microelectronics Reliability 44 (2004), pp. 657-664.
- [10] Toczek W., Self-testing of fully differential multistage circuits using common-mode excitation, Microelectronics reliability, vol. 48, pp.1890-1899, 2008.
- [11] Van Peteghem P.M., Duque-Carillo J.F., A general description of common-mode feedback in fully-differential amplifiers, ISCAS'90, IEEE Int. Symp. Circ. Systems, pp. 3209-3212, New Orleans, LA, USA, 1990.
- [12] Rossi G.B., A probabilistic model for measurement processes, Measurement; vol. 34, pp. 85-99, 2003.



- [13] Stratigopoulos H. G., Tongbong J., Mir S. A General Method to Evaluate RF BIST Techniques Based on Non-parametric Density Estimation, Design, Automation and Test in Europe, 2008, pp. 68-73.
- [14] Czaja Z., A fault diagnosis algorithm of analog circuits based on node-voltage relation, 12th IMEKO TC1-TC7 Joint Symposium, pp. 297 – 304, Annecy, France, September, 2008.
- [15] Czaja Z., Using a square-wave signal for fault diagnosis of analog parts of mixed-signal electronic embedded systems, IEEE Transactions on Instrumentation and Measurement, vol. 57, n°. 8, pp. 1589 – 1595, August, 2008.
- [16] Atmel Corporation, 8-bit AVR microcontroller with 16k Bytes In-System Programmable Flash, ATmega16, ATmega16L, PDF file, Available from: www.atmel.com, 2003.
- [17] Czaja Z., A diagnosis method of analog parts of mixed-signal systems controlled by microcontrollers, Measurement, vol. 40, n° 2, pp. 158-170, 2007.
- [18] Deliyannis T., Sun Y., Fidler J.K. Continuous-Time Active Filter Design. CRC Press 1999.