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EMI mitigation of GaN power inverter leg by local shielding techniques

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***Abstract*—This paper presents local shielding techniques applied to a half-bridge inverter leg with the aim to reduce the common mode (CM) current noise at converter's DC input. The research study is conducted for 650V Enhancement mode Gallium Nitride (GaN) power transistor switches. Main contributors of parasitic capacitances referred to the inverter-leg middle point node are identified. Then, shielding solutions are proposed to reduce CM current emission by these capacitances. Respecting the precautions concerning the isolation of CM currents of the half-bridge inverter leg, the electromagnetic compatibility measurement setup is developed. Experimental step-by-step addition of local shielding copper layers to different contributors of middle point capacitance shows progressive attenuation of CM noise spectra.**

***Index Terms*—Half-Bridge Inverter, CM current, GaN power transistor, Electrostatic shielding, Switching cell, Electromagnetic Interference (EMI) mitigation, Electromagnetic Compatibility (EMC)**

I. Introduction

PROGRESSIVE employment of GaN based transistors in power electronics converters reveals their advantages of higher switching frequency, and improved efficiency and power density [1], [2]. However, high switching speed of power devices in a range of few nanoseconds results in extremely high $\mathrm{d}v/\mathrm{d}t$ (over 100V/ns) of the associated voltage waveforms across power switches or between dynamically changing circuit nodes potentials and the ground. These phenomena induce severe Common Mode (CM) electromagnetic interference (EMI) in the form of conducted and radiated emissions. To minimize their impact on converter operation, different precautions have to be taken at early stages of power and gate circuits layout design.

Since the stray inductance in the commutation loop has a significant impact on the level of EMI, many papers propose optimization of PCB. In [3], the power loop parasitic inductance and the device package common source inductance have been shown to be critical for the performance and efficiency of synchronous buck converter operation. However, low-inductance commutation loops overlapping the bus-bar planes and gate drive tracks increase parasitic capacitances between dynamically changing circuit nodes and the ground. At power switching instants with high $\mathrm{d}v/\mathrm{d}t$, they cause that the CM current circulation paths deteriorate the reliability of converter operation [4], [5]. In order to optimize this design trade-off diverse integration technologies of GaN power module assemblies were extensively investigated: encapsulation of switching cell in package [6], gate drive circuit integration [7], 3D packages for inverter leg [8].

Other solutions are based on improving the control and modulation strategy or filtering. Attempts to attenuate the CM current noise triggered a number of research efforts: soft-switching converter topologies [9], [10] optimization of EMI filter design [11], balanced switching circuits [12], passive component location with printed circuit board (PCB) layout optimization [13], or shielding-cancellation techniques in isolation transformer converters [14], [15]. However, since full cancellation of stray components is not physically possible, then the design objectives were oriented toward managing CM current circulation paths in the nearest proximity of the power switching cell [16]. Thus, the resulting CM current flowing outside the converter in the line impedance stabilization network (LISN) could be reduced. Furthermore, requirements for the EMI input filter design could be progressively reduced in both complexity and volume.

The approved and effective ways to reduce the CM noise include electrostatic shielding techniques that are integrated in a multiconductor circuit layout [17]. In this way stray capacitances between shielded nodes and the ground are split to enable CM current to recycle around the perturbation source via low impedance of the conductive plane. Previous solutions based on shielding the pulsating node of a boost converter by means of bipolar output voltage tracks for a two-layer PCB were described in [18]. The technique proposed in [19] added a conductive shielding plane between or under tracks and the ground plane. In a similar way to diverting the noise back to the DC bus, a method of two stacked direct-bonded-copper (DBC) substrates was proposed in [20].

In this paper, another shielding solutions are applied to the inverter leg middle track, the gate driver power supplies and the power switch cooling pads by connecting conductive shielding layers with bus bars. Thus, the resulting arrangement of parasitic capacitances is changed. Based on the half-bridge inverter topology, the paper objectives are to prove quantitatively the shielding effectiveness by measuring the reduction of CM current spectra at the LISN inverter DC input.

The paper is organized as follows. Section II briefly introduces the electrostatic shielding concept of PCB track. Next, in Section III the demonstrator board of a half-bridge inverter

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switching cell is described with focus on the electromagnetic compatibility (EMC) measurement setup. The proposed shielding techniques applied step-by-step to the tested converter are presented in Section IV, and the corresponding experimental CM current attenuation spectra in Section V.

II. Shielding Concept

Fig. 1a illustrates the basic phenomenon involved in CM generation: the switching cell generates a high $\mathrm{d}v/\mathrm{d}t$ slope which excites the CM current flow through parasitic capacitance C_{cm}, due to natural existence of grounded elements such as metal enclosure, copper/aluminum heat sink, etc, nearby PCB tracks. The LISN is used to close the CM current circulation path and to provide stable input impedance. This action can be represented by a simplified model (Fig. 1b) using the voltage source V_{DS}, and the LISN impedance $Z_{LISN}/2$ in CM to close the loop. Using a conductive shielding foil between the floating point of the switching leg and the ground (Fig. 2) changes the distribution of stray capacitances, as illustrated in Fig. 1c. Three capacitances can be distinguished: C_{cm1}, C_{cm2}, C_{cm3}. The capacitances C_{cm1} & C_{cm2} come from the capacitive divider and depend on the distance between the shield-ground and shield-track nodes. Their series association is equal to the initial capacitance C_{cm} of the unshielded case. The parasitic capacitance C_{cm3} represents the remaining capacitance between the floating point and the ground, which is not exactly equal to zero, due to misalignment of the shield (e.g when the shield area does not fully cover of the track) and some edge effects. In the case of perfect alignment of shield and middle point areas the capacitance C_{cm3} can be neglected.

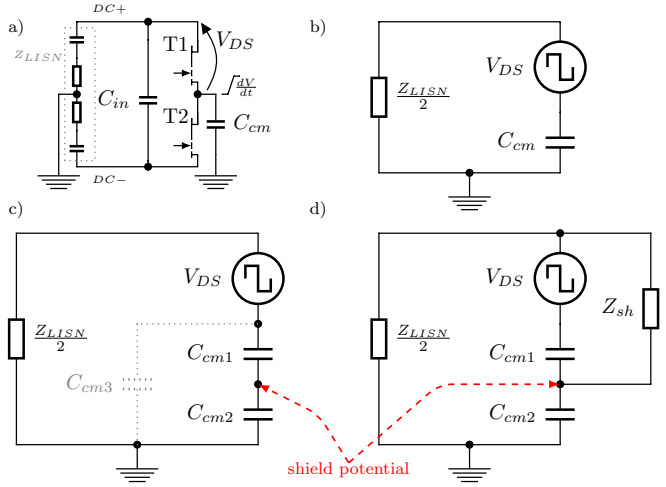

Fig. 1. Lumped CM models of PCB track shielding: a) generic circuit of inverter leg; b) unshielded; c) conductive shielded plane floating, d) conductive shielded plane with bus-bar connection

Hence, the use of the shield according to Fig. 1c will not be effective if there is no connection of the shield potential to other potentials of PCB tracks (due to no alternative path for the CM current). In [19] the authors have introduced this type of shield along a wide area of PCB as results of which alternative paths have been created through stray capacitances of other tracks. However, this approach provides paths with high impedance, which results in poor effectiveness of the shield. Based on these considerations, a shield is proposed as a low conductive plane impedance (Z_{sh}) connected to the stable potential - positive bus-bar track of the converter (Fig. 1d).

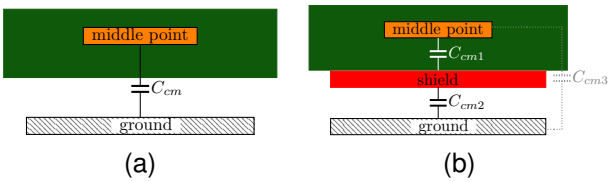

Fig. 2. Geometrical presentation of the PCB middle point track with stray capacitances: a) unshielded; b) shielded

In the idealized circuit of Fig. 1d, the CM current I_{cm} splits into two branches: one flowing through C_{cm2} and the ground to LISN, and the other circulating through the inserted shielding (Z_{sh}). The ratio between these two currents is corresponds to the impedance ratio of the two branches. The simulation of circuits in Fig. 1b and Fig. 1d was performed using Saber@Sketch simulator to compare the LISN CM current spectra without shielding and with shielding for two values of shielding impedance 1Ω (4% of $Z_{LISN}/2$) and 0.1Ω (0.4% of $Z_{LISN}/2$), where $Z_{LISN}/2$ for CM was equal to 25Ω. The V_{DS} waveform of voltage was trapezoidal with 20V/ns slope corresponding to the experimental $\mathrm{d}v/\mathrm{d}t$ in this paper, see Fig. 6. The preformed simulation results (Fig. 3) confirm significant CM noise mitigation, up to 70dB, for the low impedance conductive shielding plane.

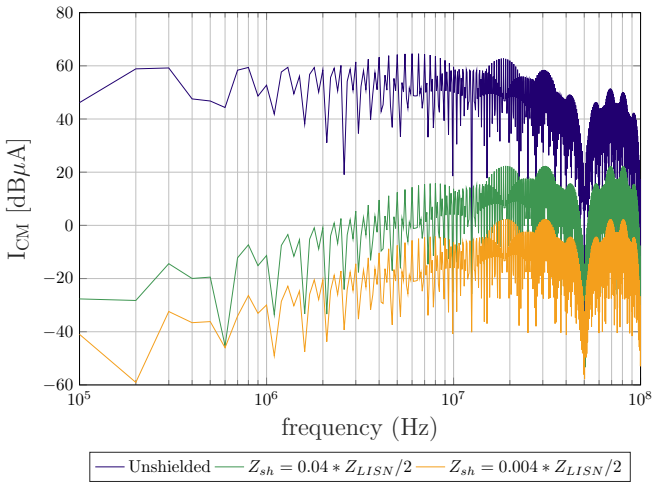

Fig. 3. CM current spectra for different shielding conditions: unshielded referring to Fig. 1b, and two Z_{sh} values referring to Fig. 1d

This section has illustrated the basic shielding principle of CM current, with the shield being connected to a stable potential with low impedance, to facilitate internal recirculation of the CM current. The following section will describe the GaN switching cell to which the above concept was applied.

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III. Demonstrator System Description

A. Half-bridge inverter description

A half-bridge inverter switching cell (Fig. 4) is used to investigate CM stray capacitances and the impact of shielding techniques on modification of CM current paths. The inverter is fed from a DC voltage source (V_i=250V) through the LISN. Two input capacitors $C_{in}/2$ split the DC link voltage V_i to create a 0V midpoint connection for the load. The inverter feeds the resistive load R_{load} via an inductive output filter L=15µH. To attenuate CM current circulation path through the load circuit, a CM filter choke L_{CMC}=705µH with coupling factor k=0.99675 and differential inductance of 3.4µH is installed between the inverter output terminals and the filter.

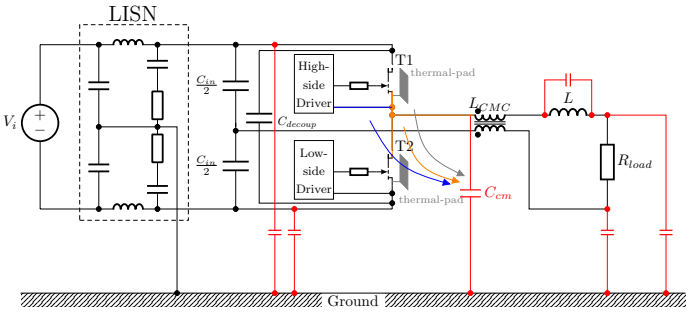

Fig. 4. Half-bridge inverter in the laboratory setup with stray capacitances location

The inverter is switched at 250kHz. The global waveforms of load voltage and current are depicted in Fig. 6. Due to the resistive-inductive load, all four consecutive conduction states of the half-bridge inverter at rectangular voltage operation mode are obtained. The zoom of the voltage waveform at turn off in Fig. 6 shows a reduced voltage overshoot, which validates the inverter circuit design layout by minimizing the stray inductance (see section B).

B. PCB layout design

The inverter demonstrator was designed using a four-layer PCB. It is composed of: positive (DC+) and negative (DC-) power bus-bars, two series-connected electrolytic capacitors $C_{in}/2$, T1-T2 inverter leg, decoupling capacitors C_{decoup}, and CM filter choke L_{CMC}.

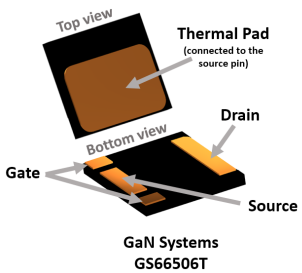

Fig. 5. Description of GaN package

The enhancement mode GaN power transistors (GS66506T) T1 and T2 are used in the inverter leg. Since GaN HEMT transistors have reverse conduction capability, the synchronous operation of the inverter leg is obtained without freewheeling diodes. The transistors are top-side cooled: they possess thermal pads internally connected with the source terminal and substrate (Fig. 5). A planar 2D placement of power switches [8] has been chosen where both transistors are soldered at the top of the PCB. Owing to top-side cooling devices, heat dissipation is easily realized by the heat sink mounted directly on both devices. In further consideration, the heat sink potential is assumed as the ground. Its location is crucial for CM noise generation. In detail, the source potential of the High-Side switch (T1) is connected to its thermal pad located close to the grounded heat sink. It increases the total CM stray capacitance C_{cm} of the inverter middle point. To reduce the power loop, decoupling capacitors have been placed directly beneath the transistors, on the bottom side of the PCB. Also, the layout of the DC+ and DC- tracks (bus-bars) has been designed such as to provide a symmetrical and as-short-as-possible power loop (Fig. 7). Close to the transistor gate terminals is placed a half-bridge driver with two isolated channels for top and bottom transistor control. The gate circuit consists of two branches with resistors R_{on} & R_{off} and diode D_{off} to separately tune the speed of transients. The isolated secondary sides of the driver are supplied from a separate PCB, mounted perpendicular to the main board to reduce the impact of parasitic capacitances of the power supply circuit on CM current generation. Particular consideration has been taken to the layout of the inverter middle point track, which is forced to change dynamically the voltage during inverter operation. The layout of this track was designed using the two middle layers of PCB (Yellow & Cyan layers in Fig. 7) with the same tracks' geometry connected by vias to increase the current capability of the converter. The size of this track was intentionally increased to obtain the values of track stray capacitances comparable with the capacitance between the GaN transistor thermal pad and the ground (Fig. 7).

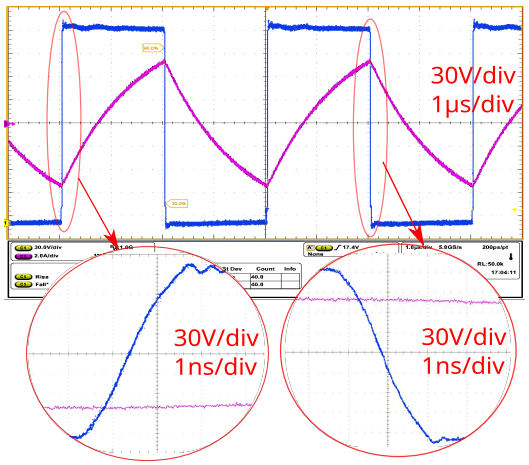

Fig. 6. Inverter voltage and current waveforms

C. Test setup for conducted EMI measurement

To perform the comparative study of shielding effectiveness, a dedicated setup for conducted EMI measurements has been built (Fig. 8). In this test bench, the converter is supplied from an external power source through a CISPR-16 compliant

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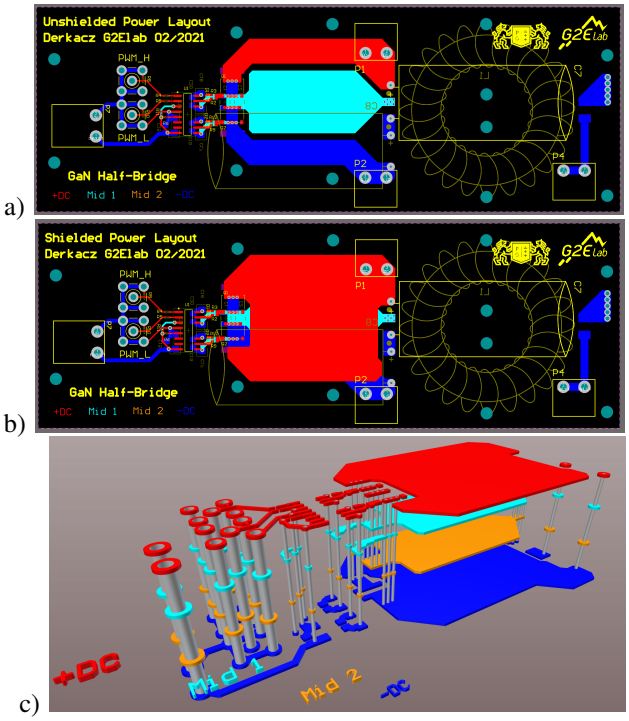

Fig. 7. View of the demonstrator with middle track: a) unshielded, b) shielded, c) exploded 3D view of shielded PCB: sandwich between DC+, middle point and DC- as described in section IV.A, (thickness of the board in scale 10:1) (colors: Red - Top Layer, Blue - Bottom Layer, Yellow&Cyan - Middle Layers)

LISN. The gate transistor drivers are fed by two 9V batteries (Fig. 9). The CM current is captured on a Spectrum Analyzer with a current probe including both plus and minus wires between the LISN and the converter input. To provide clean and fully repeatable measurements, several precautions have been introduced:

- The converter board and the output filter have fixed position and distance to the ground (2.5cm above the copper ground plane) (Fig. 8);
- Power and signal wires are mounted on dedicated stands with fixed position and distance to the ground (2.5cm);
- All unnecessary equipment (auxiliary power supplies, signal generator, oscilloscope, etc.) are moved out of the table (far from the ground area) to mitigate stray capacitances and to avoid unknown CM paths;
- As mentioned earlier, a CM Choke is placed between the middle point of the inverter and the output inductor. Its aim is to significantly increase the CM impedance path through the load and therefore to prevent flowing of CM current in this direction;
- The resistive load is built from discrete parts in a TO-247 package mounted on the aluminum heat sink. This set is placed perpendicularly 40cm above the ground plane to reduce stray CM capacitance of the load;
- A dedicated stand with wires and spot for the current probe is used between the LISN and the converter input to provide the same conditions and position of the measurement device.

Fig. 8. EMC measurement setup with introduced all precautions

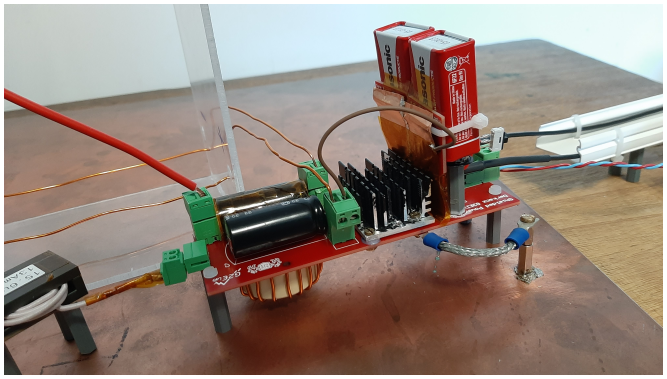

Fig. 9. Zoom on converter with driver fed by two 9V batteries, and output inductance on the left (L_{CMC} is on the bottom side of PCB)

IV. Shielding of The Three Main CM Capacitance Contributors

Common mode noise generation in inverters is mainly related to the existence of parasitic capacitance between the inverter leg midpoint and the ground. A systematic experimental study of a half- bridge inverter leg based on the lateral GaN HEMT structure has indicated three main contributors of CM capacitance: middle point PCB track to ground, thermal pad of the top switch (T1) to ground, gate circuit of the top switch (T1) to ground (Fig. 10). All these three parts are connected to the point with high $\mathrm{d}v/\mathrm{d}t$, and each of them increases the area of this point (by copper tracks), thus resulting in the increased stray capacitance to ground. The application of shielding techniques, as described in details in next paragraphs, provides new paths for the CM current to recirculate inside the converter (Fig. 11)), which leads to the reduction of CM noise.

A. Inverter middle track shielding

The middle point track (power part) shielding by conductive local plane is realized by extending the surface of the DC+ and DC- bus-bars planes. These planes are acting as a shield, as referred to in Section II, and overlapping the middle point track in 92.55% of the area for shielded layout (Fig. 7b). For comparison, only 2.14% of the middle point area is overlapped for unshielded layout (Fig. 7a). For the unshielded version shown in Fig. 12a the CM current flows mainly through the capacitance between

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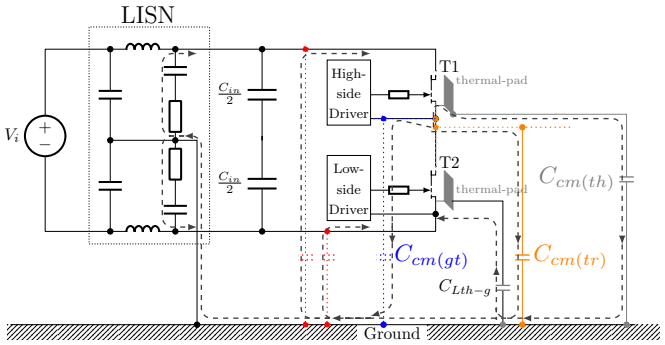

Fig. 10. CM stray capacitances and current circulation paths of the unshielded converter

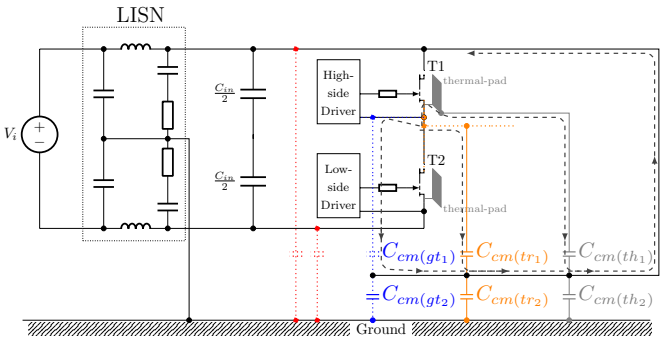

Fig. 11. CM stray capacitances and CM current paths (recirculation) for shielded converter (shielded: middle point track, thermal pad, gate supply circuit)

the middle track and the heat sink. The capacitance C_{cm} (as in Fig. 2) is approximately equal to $C'_{m\leftrightarrow h}$ (Fig. 12a), since the capacitances $C'_{m\leftrightarrow DC+}$ and $C'_{m\leftrightarrow DC-}$ between the middle track and DC+ and between the middle track and DC-, respectively, are relatively small (Table I). It is noteworthy that in the unshielded version, the capacitance $C'_{DC+\leftrightarrow h}$ between DC+ and heat sink has a significant value, but it is series connected with small $C'_{m\leftrightarrow DC+}$, and therefore can be neglected as a component of capacitance C_{cm}. Additionally, this capacitance is not connected to a floating point but to a stable potential. Therefore, it does not contribute to CM generation, but rather to CM internal recycling.

TABLE I
STRAY CAPACITANCE VALUES FOR UNSHIELDED AND SHIELDED MIDDLE POINT TRACK

Capacitance	Value [pF]
Unshielded (Fig. 12a)	
$C'_{m\leftrightarrow h}$	5.8
$C'_{DC+\leftrightarrow h}$	3.7
$C'_{m\leftrightarrow DC+}$	1.09
$C'_{m\leftrightarrow DC-}$	0.9
Shielded (Fig. 12b)	
$C''_{m\leftrightarrow h}$	0.56
$C''_{DC+\leftrightarrow h}$	10.3
$C''_{m\leftrightarrow DC+}$	33.7
$C''_{m\leftrightarrow DC-}$	33.6

When shielding is applied, the extended surfaces of DC+ and DC- bus-bars (Fig. 12b) increase the capacitances between the bus-bars and the middle track, which affects the switching speed (described in Section V.A). The capacitance $C'_{DC+\leftrightarrow h}$ between DC+ and the heat sink is increased by the parallel-connected capacitance $C''_{DC+\leftrightarrow h}$. The CM current I_{cm} flows through the capacitance $C''_{m\leftrightarrow DC+}$. At the DC+ node, I_{cm} splits in two parts: the -first component recirculates within the switching cell through low impedance of the shield and the DC+ tracks, while the -second component flows through capacitance $C'_{DC+\leftrightarrow h}$ + $C''_{DC+\leftrightarrow h}$ to the heat sink. Since the value of $C''_{m\leftrightarrow DC+}$ is much larger than that of $C'_{DC+\leftrightarrow h}$ + $C''_{DC+\leftrightarrow h}$, a proportionally smaller current flows to the heat sink. Most of the I_{cm} current recirculates inside the switching cell according to Equation (1) (with a given value of $C''_{DC+\leftrightarrow h}$ and the assumption that Z_{sh}=0.1Ω):

@150kHz, $I_{cm\text{-}heatsink}$= 0.00000097·$I_{cm\text{-}recirculation}$,
@30MHz $I_{cm\text{-}heatsink}$= 0.00019·$I_{cm\text{-}recirculation}$.

$$\frac{I_{cm-heatsink}}{I_{cm-recirculation}} = \frac{Z_{sh}}{\frac{Z_{LISN}}{2} + j\omega C''_{DC+\leftrightarrow h}} \quad (1)$$

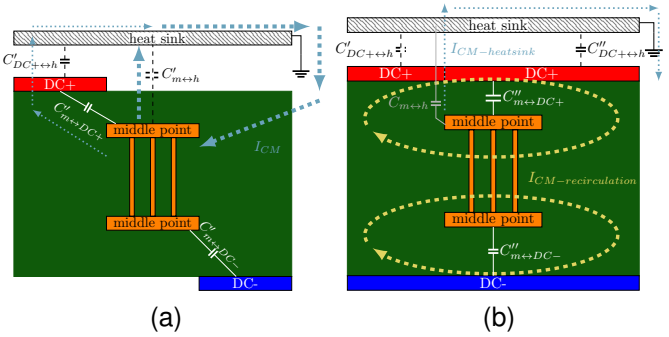

Fig. 12. Stray capacitance distribution in the PCB cross-section a) unshielded, b) shielded middle track

B. GaN thermal pad shielding – lab solution

The next step of recirculating the I_{cm} current in internal path is mounting the shielding layer between the thermal pad and the heat sink (Fig. 13). This approach is a further extension of middle point shielding. However, its practical realization in this study had to be adapted to laboratory conditions. A copper foil was used as a conductive shield connected to the constant potential DC+. The isolation between the thermal pad and the shield, and between the shield and the heat sink was made using a Kapton insulator, as presented in Fig. 14. It ensured capacitive coupling between the transistors' thermal pads (source connected) and the DC+ bus-bar, which resulted in increasing the total C_{cm} capacitance but also in providing an additional path for CM recirculation (as described in the previous paragraph) The application of thermal pad shielding to the lower switch (T2) created an additional stray capacitance C_{Lth-g} (Fig. 10) which increased the total DC- to ground stray capacitance and helped in CM current recirculation inside the GaN power inverter leg.

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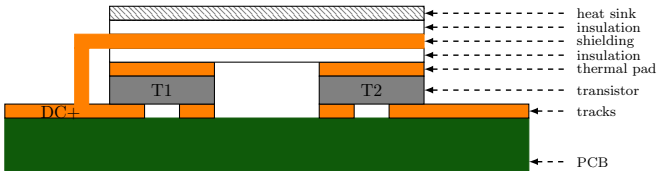

Fig. 13. Thermal pad shield cross view

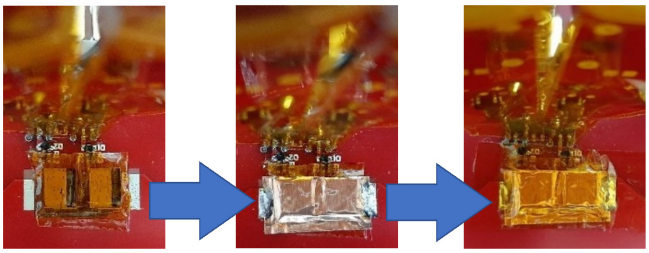

Fig. 14. Stages of thermal pad shield application: a) placing 1st insulation layer on thermal pad of GaN package, b) applying copper foil shield and soldering it to the bus-bar, c) placing 2nd insulation layer between shield and grounded heat sink

C. Shielding of Power Supply Boards for Gate Drivers

The isolated secondary sides of the gate driver are supplied from dedicated PCB boards. On these boards, 9V batteries with voltage conditioning circuits are used as the voltage sources for each channel of the dual channel gate driver. To minimize CM capacitance of these circuits to the reference ground plane, the boards are mounted perpendicularly to the main board (Fig. 15b). However, a grounded heat sink is still placed in the nearby of these boards, which increases the CM capacitance. As in the previous case, shielding can also be applied to this part of the converter. In laboratory conditions, similarly to the thermal pad, Kapton insulation and copper foil were used to create the shield, which was by short wire connected to the DC+ potential (Fig. 15a).

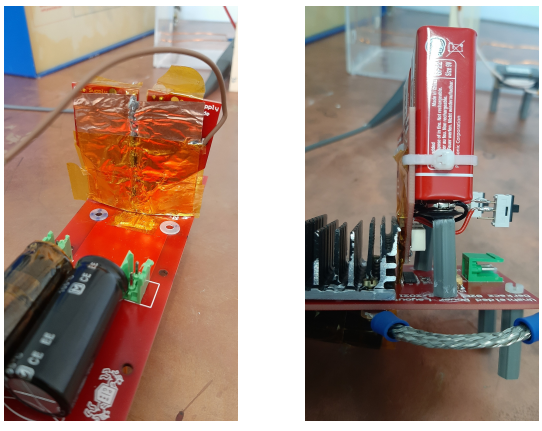

Fig. 15. Gate driver power supply boards: a) view with applied shielding, b) perpendicular installation of supply boards in the converter

V. Experimental Results

A. Impact of individual shielding

The laboratory measurement of I_{cm} current was performed in four steps for progressive shielding application variants. The first variant represented the middle point track shielding being the result of introduction of additional parasitic capacitance parallel to the transistor internal capacitance C_{DS} which changed the rising time of V_{DS} (Fig. 16a). To check the effectiveness of shielding, an additional capacitor C=80pF was installed in the unshielded PCB between the drain and source transistors' nodes to get the voltage slopes the same in both cases, as presented in Fig. 16b. The I_{cm} spectra of unshielded PCB with additional capacitor and the PCB with unshielded middle point are compared in Fig. 17. Slight differences are noticed in the spectrum for frequencies above 15MHz. Then, a significant difference is observed above 20MHz, which depicts the impact of slope reduction on I_{cm} generation. Adding 80pF to the (unshielded) reference case allowed having the same $\mathrm{d}v/\mathrm{d}t$ for comparison.

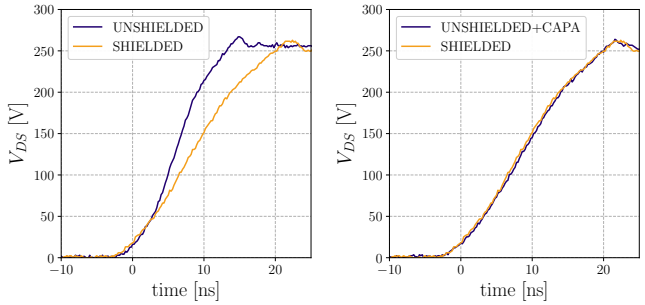

Fig. 16. Comparison of V_{DS} slopes: a) PCB with shielded (orange) and unshielded (blue) middle point; b) PCB with shielded (orange) middle point and unshielded with additional lumped capacitors C=80pF (blue)

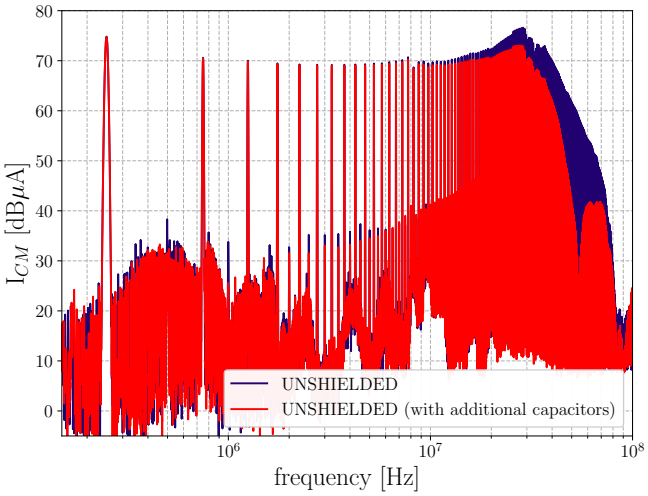

Fig. 17. CM current emissions of unshielded middle point and unshielded with additional lumped capacitors

The I_{cm} spectra for the unshielded PCB and with the shielded middle point track are compared

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in Fig. 18. It can be noticed that for PCB with shielded middle point track, the basic harmonic and its subharmonics are reduced by about 2-3dB, while for frequencies above 10MHz, this reduction reaches 5.5dB. Comparing these results with Fig. 17 proves that the reduction of I_{cm} emission in the frequency range up to 20MHz is caused by shielding the middle point track (and not due to $\mathrm{d}v/\mathrm{d}t$ reduction, as the $\mathrm{d}v/\mathrm{d}t$ values have been equalized with the 80pF capacitance in the unshielded case).

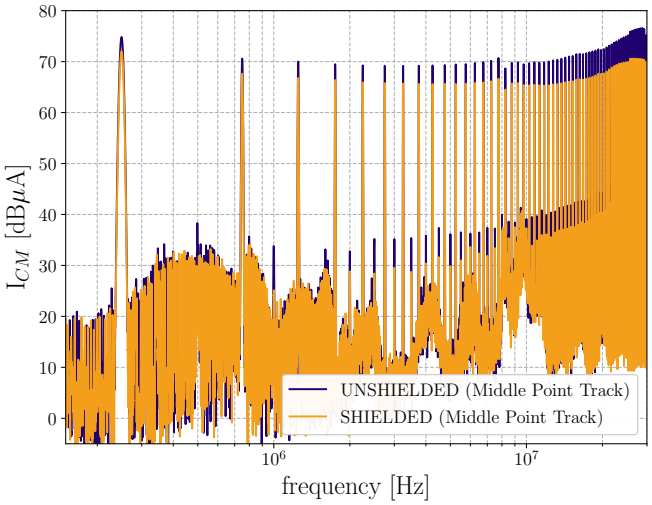

Fig. 18. CM current emissions with and without shielded middle point track

Further reduction of I_{cm} can be obtained via shielding of the thermal pad. The effectiveness of thermal pad shielding is demonstrated in Fig. 19 by comparing the spectrum of shielded middle point track with that of shielded middle point track and shielded thermal pad, (here the orange spectrum from Fig. 18 is used as reference and plotted blue). The emission attenuation is observed in the whole frequency range, from 0.8 to 30MHz, with the greatest diminution amounting to 7dB.

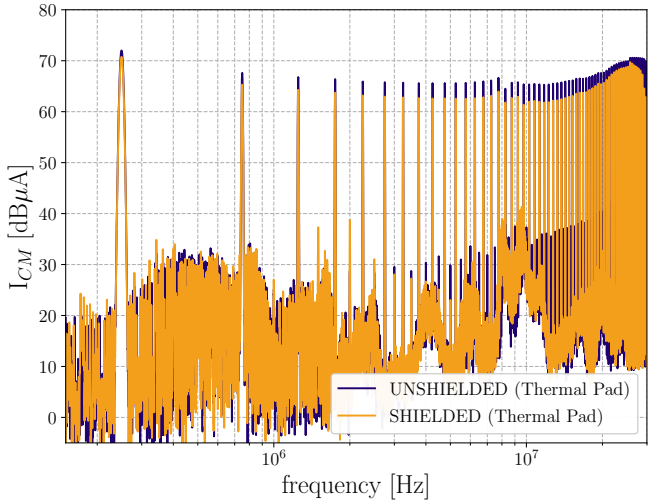

Fig. 19. The effectiveness of thermal pad shielding

In the next step, shielding of the gate circuit power supplies was investigated. The copper foil was used to create a low conductive shield. As a result, successive decrease of I_{cm} level by 2-5.5dB was observed in the spectrum (Fig. 20).

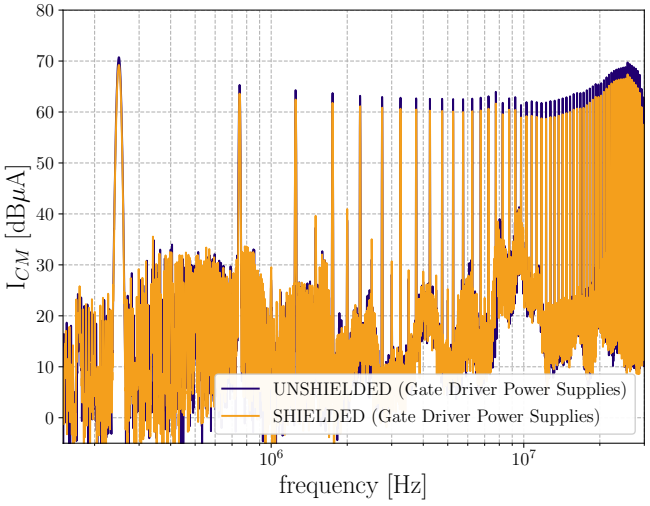

Fig. 20. The effectiveness of shielding of gate driver supplies

B. Total shielding effectiveness and quantitative data comparison

The comparison of the unshielded and totally shielded converters is presented in Fig. 21, where significant reduction of I_{cm} noise is achieved in the whole investigated frequency range.

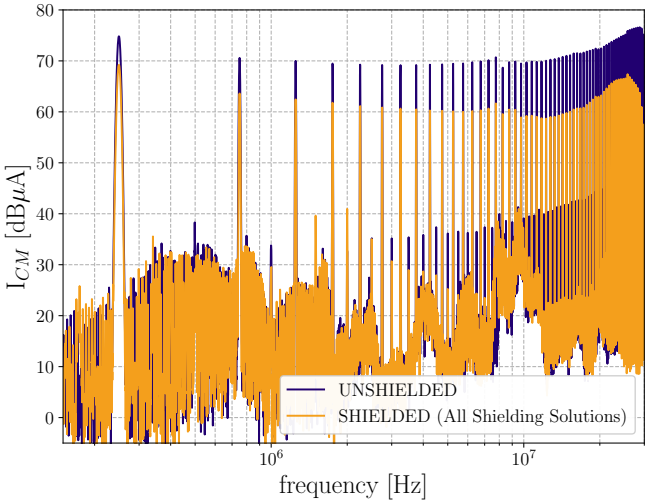

Fig. 21. CM current emissions with and without total shielding solutions

The comparison of quantitative data is presented in Table II. The noise levels for specific frequencies (beginning, middle and the end of the conducted emission spectrum range) are put together. In this way, the impact of individual contributors of shielding can be compared. Moreover, the scale of reduction with respect to the unshielded version is given in Table II in brackets for each shielding step.

TABLE II
COMPARISON OF CM NOISE LEVELS AT SPECIFIC FREQUENCIES (REDUCTION INDICATED IN BRACKETS)

Specific frequency of spectrum	Unshielded [dBµA]	Shielded: middle point [dBµA]	Shielded: middle point & thermal pad [dBµA]	Shielded: middle point & thermal pad & gate power supplies [dBµA]
1.25MHz	70.01	66.79 **(-3.22)**	64.29 **(-5.72)**	62.43 **(-7.58)**
10.025MHz	69.72	65.36 **(-4.36)**	61.95 **(-7.77)**	59.2 **(-10.52)**
29.76MHz	75.17	69.91 **(-5.26)**	62.87 **(-12.3)**	57.5 **(-17.67)**

C. Discussion of EMC vs thermal performances

The application of shielding by conductive copper layers increases parasitic capacitances between the drain and source terminals of switching transistors, thus introducing extra power switching losses.

The thermal pad shielding requires two layers of insulation. It doubles the thermal resistance from the case to the heat sink ($R_{th(c-h)}$), which is one of the disadvantages of this CM suppression method. The use of Kapton as insulation and thermal interface material, as presented in Section IV.B., is sufficient to verify the effectiveness of the thermal pad shielding. However, it does not present a commercial solution. The impact of doubling Kapton can be minimized in the designing step by the appliance of other materials.

These constrains should be taken into account in the designing process and global optimization of the converter to achieve the trade-off between CM current emission, power switching losses and thermal performance [21].

VI. CONCLUSION

In this paper, the proposed shielding technique is described and explained in detail. The new approach by shielding connecting to the positive or negative potential of the stable bus-bar has been presented, simulated, and measured, and its effectiveness has been proved. Moreover, three different contributors of Common Mode capacitance: middle point track, thermal pad and gate circuit power supplies were extracted and highlighted. The shielding concept was successfully applied to each of them, which resulted in a total of over 17dB reduction of CM noise. In order to guarantee that the CM reduction is directly the effect of shield implementation, care has been taken to have the same $\mathrm{d}v/\mathrm{d}t$ for the unshielded and shielded cases.

The proposed shielding solutions can be used in embedded integration of power device dies in PCBs. Due to the obtained reduction of CM current noise, they can be essentials for wide band gap power devices. Resulting in weight and volume reduction of EMI filters, and do not impacting power density of converter without noticeable increase of additional copper layer weight.

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