Improving Control Dynamics of PMSM Drive by Estimating Zero-Delay Current Value

Leszek Jarzebowicz[1], Artur Opalinski[1], Maciej Cisek[1]
[1]Faculty of Electrical and Control Engineering, Gdansk University of Technology,
G. Narutowicza 11/12, 80–233 Gdansk, Poland
leszek.jarzebowicz@pg.gda.pl

***Abstract*—Dynamic performance of current control loop still remains crucial for position-, speed-, and torque-controlled drives. In the study, a current loop solution has been designed for field oriented control of permanent magnet synchronous motors (PMSM). It enhances typical PI controller with an estimator of zero-delay current (ZDC) value. The ZDC estimation allows for selecting substantially higher controller gain. It reduces control loop step response rise time to a single control cycle, which is the shortest technically possible value, while avoiding overshoot. The method does not require any hardware changes and it needs only negligible processing overhead. Both simulations made and experimental results obtained in the study have proved the effectiveness of the proposed solution.**

***Index Terms*—Control performance, permanent magnet motors, variable speed drives, synchronous sampling.**

I. INTRODUCTION

Dynamic properties of electric drives are crucial to many industrial applications. The most demanding devices are typically fitted with permanent magnet synchronous motors (PMSM), which allow for very fast torque and speed response due to their low stator inductances and low moment of inertia, respectively.

Control structure of electric drive consists of those: an inner current control loop and of outer speed and position loops, optionally. Some recent efforts aim at improving the speed and position control algorithms [1]–[3]. However, dynamic response of the drive is ultimately limited by the properties of the inner control loop. Therefore, the dynamic performance of the current control loop remains crucial for position-, speed-, and torque-controlled drives.

A typical current control loop is based on proportional-integral (PI) controller, highly appreciated in industry due to its simplicity and reliability. Alternative approaches, e.g. predictive controllers, while being superior to PI-based solutions in terms of dynamic properties, are substantially more difficult to implement and require dedicated efforts to reduce their dependency on inaccuracy and variability of pre-determined drive parameters [4].

The work described in this paper addresses the gap between PI and alternative controllers, to find balance between implementation complexity and dynamic performance. The proposed current loop solution enhances the capabilities of typical PI controller by an estimation of

motor current value for the beginning of forthcoming control cycle, i.e. zero-delay value. This reduces the control loop step response rise time to a single control cycle, i.e. to the shortest technically possible value, without hardware changes and with negligible processing overhead.

II. APPROACHES TO IMPROVEMENT OF CURRENT CONTROL LOOP PERFORMANCE

Recent works related to current control loop performance can be classified into three groups. The first group aims at improving current measurement accuracy. The second proposes to improve the dynamic properties of current loop by increasing the rate of control algorithm response without increasing the pulse width modulation (PWM) carrier frequency. The last one is focused on predicting the control variables for the forthcoming control cycles.

Impact on the control performance of electric drive from scaling and offset errors in current measurement is analysed by Kim *et al.* [5]. Jarzebowicz analyses the errors resulting from transformation of sampled phase currents into rotating coordinate frame [6]. Both papers contain methods for compensating systematic errors which improve general performance of current control.

Bocker and Buchholz prove that updating the PWM generator with a ratio of 8 to 16 may significantly improve control bandwidth [7]. Typical controllers allow for single or double update of reference voltage in a PWM cycle [8]. Therefore, the proposed solution requires an extraordinary PWM generator.

A predictive approach to field oriented current control algorithm in electric drives is proposed by Cortes *et al.* [9]. Predictive current controller calculates future behaviour of the system based on a model and a set of possible actuations for the horizon of two forthcoming control cycles. Similar method using Smith predictor is applied to an inverter operating in active power filter by Zhou and Liu [4]. Both approaches increase computational complexity and share dependency on using exact system parameters, inherent to model-based prediction. In turn, Anuchin and Kozachenko propose to extend PI controller with a current predictor which uses oversampling and digital filtering to calculate the zero-delay value of DC motor armature current [10].

The aim of this work is to indicate an algorithm for estimating zero-delay current (ZDC) values for PMSM drive and to investigate how this estimation will influence the dynamic performance of PI-based current control loop.

The structure for field oriented control (FOC) of PMSM is shown in Fig. 1. The motor currents are controlled in *d-q* rotating reference frame [11]. For motors with surface mounted permanent magnets the value of current i_d is forced to zero. The reference value of current i_q is set according to the required torque. Both currents are regulated by PI controllers fitted with decoupling and electromotive force (EMF) compensation block [12].
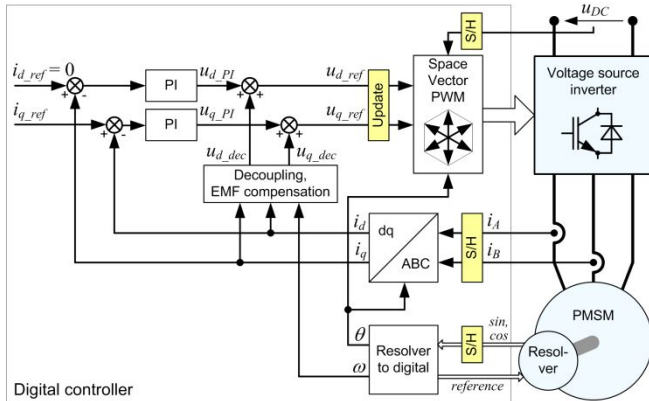

Fig. 1. General structure of FOC applied to PMSM drive.

Motor current contains ripple component induced by modulated voltage (Fig. 2). The frequencies of the ripples are much higher than the control bandwidth, thus controller is capable to influence only fundamental current component. This component should be extracted by control feedback in order to provide stable and accurate torque control. A convenient solution to this problem was reported by Blasko *et al*. [13]. The authors proved that instantaneous current, when sampled at the mid-points of passive inverter states, corresponds to the fundamental component. This method of sampling currents simultaneously with valleys or peaks of PWM carrier is referred to as synchronous sampling.

PWM voltage sequence for k^{th} control cycle has to be set up before this cycle starts, i.e. before the $t_{V[k]}$ instant in Fig. 2. Therefore the PWM update must be computed using the current value sampled either at $t_{V[k-1]}$ or $t_{P[k-1]}$ instants. This causes a delay of T or $T/2$, respectively, between current measurement instant and PWM update instant. The delay reduces the dynamics of current control.
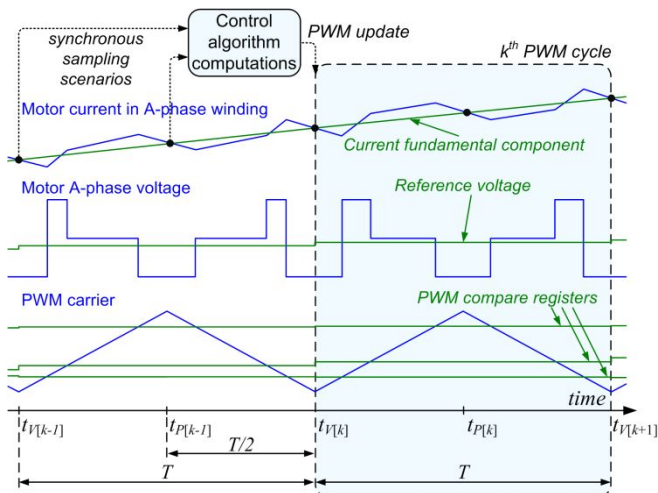

Fig. 2. Selected waveforms in PMSM drive supplied by space vector PWM-controlled voltage source inverter.

The contribution of this work consists of: enhancing PI

controller in PMSM drive FOC with linear extrapolation to estimate ZDC value from synchronous sampling; a method for selecting ZDC-enhanced PI controller gain; a time-domain model of digitally controlled drive to verify the effectiveness of the enhancement; implementing the ZDC PI controller; an experimental validation procedure; an assessment of increase in control algorithm computational complexity due to the enhancement.

III. ESTIMATING ZERO-DELAY CURRENT

The fundamental current component for a single PWM cycle can be well approximated by linear dependency [13], [14]. Thus the zero-delay current value $i(t_{V[k]})$ for the kth control cycle can be estimated by

$$\underline{i}\left(t_{V[k]}\right) = 2 \times \underline{i}\left(t_{P[k-1]}\right) - \underline{i}\left(t_{V[k-1]}\right). \tag{1}$$

Estimation requires sampling frequency being only twice the PWM frequency. The last current measurement $i(t_{P[k-1]})$ used by (1) takes place in the midpoint of $(k-1)^{th}$ PWM cycle, leaving half of cycle for control algorithm execution. As measurements are carried out synchronously with PWM carrier, no signal filtering is required to isolate the fundamental current component.

The impact of the proposed ZDC estimation on the dynamic performance of PMSM drive is investigated below by the analysis of i_q current step response. A mixed continuous-discrete model of the drive was implemented in MATLAB-Simulink. The general view of the model consisting of PMSM and digital controller is in Fig. 3.
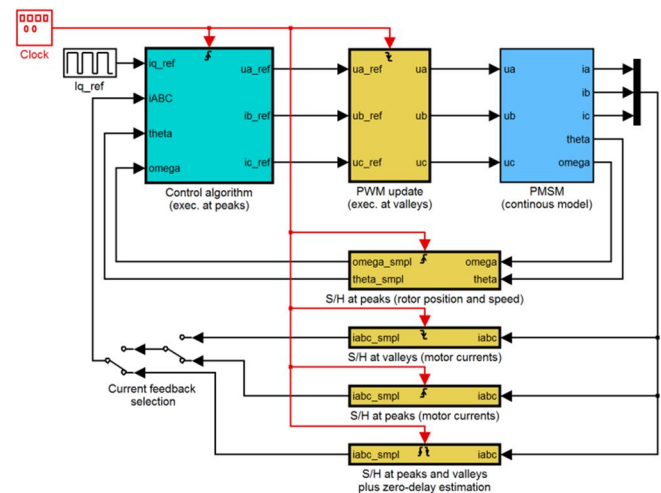

Fig. 3. Top-level view of a model of digitally controlled PMSM drive implemented in Simulink.

The PMSM model relies on standard continuous-time equations [2], [15]. The controller is modelled with triggered subsystems executed at the midpoints or at the endpoints of control cycles. This corresponds to instants of signal sampling and to instants of inverter output update. The implemented control structure is as shown previously in Fig. 1.

To assess fundamental component rise time, one has to get rid of the ripple component of motor currents resulting from changes of inverter states in each PWM cycle. These states depend on such factors as rotor position or instantaneous DC-bus voltage. To make the rise time

measurements independent from such uncontrolled factors, the modulated voltage was replaced in the model by voltage mean value calculated for each control cycle. As a result, the motor currents consist of only fundamental component.

The scope of the analysis includes the proposed ZDC approach and two typical current sampling scenarios, i.e. sampling at $t_{V[k-1]}$ or $t_{P[k-1]}$ instants. The model was set up to match laboratory drive parameters listed in Table I. The controller I-term reset time was set to $T_I = L_q/R_s$ which follows the common practice of pole-zero-cancelation [8]. The controller gain K_P was adjusted by experimenting individually for each case to obtain 5 per cent overshoot. Quantitative comparison of control loop dynamic performance is based on measuring rise time $T_{90\%}$, defined as the time required for the response to rise from 0 % to 90 % of its final value. The results of simulation including individual controller gains K_P and rise times $T_{90\%}$ are given in Fig. 4. The comparison shows the superiority of using ZDC approach over typical synchronous sampling scenarios. ZDC estimation enables for setting substantially higher controller gains to obtain the same overshoot. Therefore the rise time is reduced over 3 or over 2.5 times when compared to sampling at valleys or peaks, respectively.
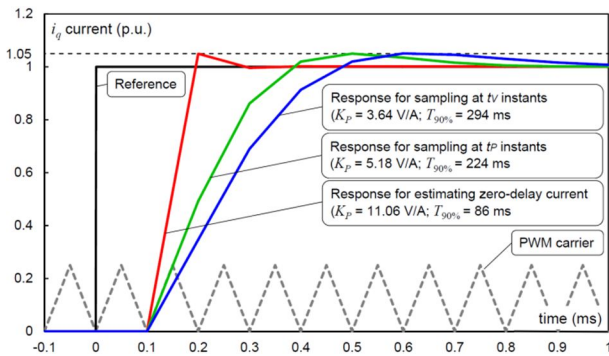

Fig. 4. Comparison of step response rise times for ZDC approach and typical synchronous sampling scenarios.

TABLE I. PMSM DRIVE PARAMETERS.

Parameter	Value
PWM carrier frequency $f = 1/T$	10 kHz
Rated phase current I_n	10 A
Rated DC-bus voltage U_{DCn}	216 V
Rated speed (mechanical) $\check{S}_{mn}$	120 rad/s
d-axis component of stator inductance L_d	0.9 mH
q-axis component of stator inductance L_q	1.05 mH
Flux linkage due to the rotor magnets $Œ_f$	75 mWb
Number of pole pairs p	9

IV. SELECTING CONTROLLER GAIN

In typical synchronous sampling scenarios the response time is a trade-off with respect to overshoot. The proposed ZDC approach allows for avoiding overshoot without increasing the rise time considered as number of control cycles. The response may still be achieved in a single control cycle if only the inverter output voltage does not reach the limit resulting from DC bus voltage.

The fastest digital control response would bring the current to its commanded value at the endpoint of the forthcoming cycle, i.e. $i_q(t_{v[k+1]}) = i_{q\_ref}(t_{v[k]})$. Simultaneously, such a response would be featured by null overshoot. The following analysis aims to select the controller gain K_P to obtain such a response.

Changes of q-axis current in PMSM can be calculated as [16], [17]

$$\frac{d i_q}{d t} = \frac{1}{L_q}\left(-R_s i_q - L_d p \check{S}_m i_d - p\check{S}_m Œ_f + u_q \right). \qquad (2)$$

The term $u_{q\_dec} = - L_d p\check{S}_m i_d - p\check{S}_m Œ_f$ is computed by the decoupling and EMF-compensation block and bypasses the PI controller [12], [15]. The voltage drop $u_R = - R_s i_q$ has a negligible impact on dynamic behavior. Therefore (2) can be simplified in terms of controller activity

$$\frac{d i_q}{d t} = \frac{u_{q\_PI}}{L_q}, \qquad (3)$$

and reformulated into discrete time-domain

$$\frac{\Delta i_{q[k]}}{T} \cong \frac{u_{q\_PI[k]}}{L_q}. \qquad (4)$$

Following the requirements of desired dynamic response the current has to change by $\Delta i_{q[k]} = i_q(t_{v[k+1]}) - i_{q\_ref}(t_{v[k]})$ during time T of PWM cycle. Thus the gain K_p of the controller should be selected to satisfy

$$K_P = \frac{u_{q\_PI[k]}}{\Delta i_{q[k]}} \cong \frac{L_q}{T}. \qquad (5)$$

The step response with controller gain set according to (5) was investigated by simulation (Fig. 5). Under step command the controller sets the output voltage u_{q_PI} to a value which cancels the error at the endpoint of the nearest control cycle (Fig. 5(a)). The decoupling and EMF-compensation function produces the u_{q_dec} component which removes the influence of motor speed on controller activity. Therefore, the control performed by the PI controller is not affected by rotor speed as long as maximum inverter output voltage is not exceeded (Fig. 5(b)).
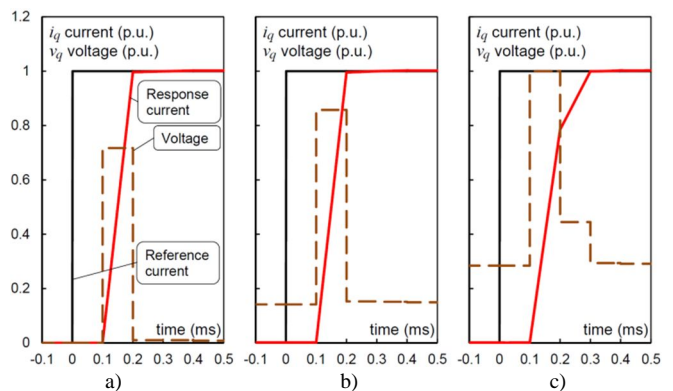

Fig. 5. Step responses in ZDC-enhanced controller for gain set accordingly to (5) and for various rotor speeds: a) $\check{S}_m = 0$; b) $\check{S}_m = 0.25$ p.u.; c) $\check{S}_m = 0.5$ p.u.

For relatively high speeds and high current steps the sum of responses from the controller and EMF-compensation function $u_{q\_ref} = u_{q\_PI} + u_{q\_dec}$ may exceed the maximum inverter output voltage. In such a case, the response takes more than one control cycle (Fig. 5(c)). Nevertheless, controller still ensures the shortest technically possible response, considering voltage limitation.

V. EXPERIMENTAL VALIDATION

The ZDC estimator was implemented in the controller of a laboratory drive with parameters listed in Table I. The control algorithm from Fig. 1 is performed by TMS320F2812 digital signal processor (DSP) running at 120 MHz. Executing ZDC formula (1) for 16-bit integer variables of i_A and i_B currents takes 6 cycles of CPU clock, i.e. 50 ns. This constitutes a negligible fraction of the total control algorithm execution time per cycle which equals 35 µs.

The i_q current is only a variable of control algorithm which is calculated based on i_A and i_B motor currents, so it cannot be measured directly. Therefore the experiment was performed with the rotor of PMSM fixed at electrical angle of $3\pi/2$ rad. In this position, the q-axis is aligned to A-axis, hence $i_q = i_A$. This allows for measuring the i_q current indirectly, by sensing motor phase current i_A.

The i_A current waveform upon a step change of i_q reference value was recorded using LEM LTS-15NP transducer and a digital oscilloscope (Fig. 6). The recording is supplemented with waveforms of controller digital outputs which indicate sample-and-hold instances and control algorithm execution duration. The current rises from zero to the nominal value in a single control cycle. Substantial ripples visible in the current waveform are caused by PWM switching. The digital controller only controls the fundamental current component (dotted line in Fig. 6) which is featured by null overshoot. This proves that ZDC method offers single-cycle rise time with no overshoot if the inverter output voltage does not reach the limit resulting from DC bus voltage.

VI. CONCLUSIONS

The ZDC approach demonstrates its ability to substantially improve the dynamic properties of PMSM current loop, while only marginally increasing PI controller computational complexity. Both simulation and experimental results verify the effectiveness of the proposed solution.
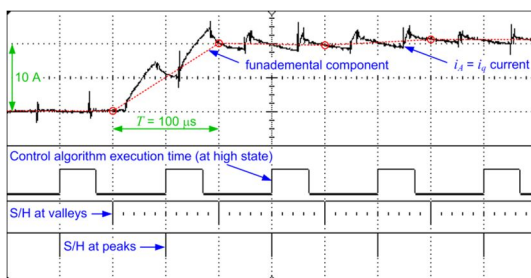

Fig. 6. Oscilloscope-registered waveforms of i_q step response for ZDC-enhanced controller.

The presented solution allows the controller to obtain single-cycle step response rise time if only enough DC-bus voltage is available to produce the reference voltage on inverter output. At the same time, the overshoot may be avoided if the recommended controller setting is applied.

The approach does not require any hardware changes. The current sampling frequency is only twice the typically applied one, which is easily achievable on modern DSPs. Due to synchronous sampling no signal filtering is required. The impact of applying ZDC on control algorithm execution time is negligible.

In future works, more formal analysis of ZDC control loop dynamics, to allow for comparing ZDC to competitive solutions in terms of bandwidth, should be aimed.

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