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Single-phase, Five-level Inverter with SPWM-Based Neutral Point Voltage Balancing Scheme

Dmytro Kondratenko[1], Arkadiusz Lewicki[1] and Charles Odeh[1]
[1]GDAŃSK UNIVERSITY OF TECHNOLOGY
Gabriela Narutowicza 11/12

80-233 Gdansk, Poland
Tel.: +48 58 347 14 02
Fax: +48 58 347 18 02
E-Mail: dmytro.kondratenko@pg.edu.pl
URL: https://eia.pg.edu.pl/kaneike/main

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Keywords

«Pulse Width Modulation (PWM)», «T-type inverter», «Capacitor voltage balancing», «Voltage Source Inverter (VSI)».

Abstract

Multilevel inverter topologies provide several advantages over two-level inverter configuration. These benefits are the reason for the growing interest in multilevel topologies among research society. One of the most popular topological concepts (diode and active switch clamping) requires neutral-point potential balancing due to series-connected capacitor banks across the input dc link in such derived inverter configurations. This paper presents a Sinusoidal PWM (SPWM) scheme that ensures balanced and reduced input capacitor voltages' variations in single-phase T-type inverter. Comparison analyses with existing carrier-based pulse-width modulation methods are provided. Simulation results are provided which showcase the effectiveness of the control approach. Experimental validation of these results was provided with a five-level single-phase T-type VSI; that supplies single-phase RL load.

Introduction

In last decade, there is growing interest in multilevel inverter (MLI) topologies. Recently, MLI topologies have been widely used in various applications such as: photovoltaic (PV) generations, wind turbine systems, electric vehicle (EV) and telecommunication power systems, etc [1]-[3]. The multilevel topologies provide some advantages such as: reduced voltage on the switches and lower total harmonic distortion (THD) of the output voltages [3], [4].

In general, MLI can be classified into five main group: the flying capacitor, diode-clamped, cascade H-bridge (CHB), matrix converters and hybrid topologies, [5]. The imbalance of the neutral point voltage is an inherent problem of multilevel diode-clamped-inverter-derived topologies (neutral-point clamped – NPC [6], T-type [7] and F-type [8] converters). NPC and T-type inverters are the most prominent, with three-level configuration. NPC is the most widely used; nevertheless, T-type topology has low conduction losses when compared to NPC inverter, [9]. Operationally, all variants of the diode-clamped topologies are equivalent. Numerous modulation techniques have been proposed to improve the output waveforms quality and achieve the dc-link voltage balance for various operational conditions. The most popular modulation techniques can be divided into two groups: sinusoidal or carrier-based pulse-width

modulation (SPWM or CBPWM), [10]-[14] and space vector pulse-width modulation (SVPWM), [15]-[19]. Several studies propose different modification of SVPWM and SPWM to solve the problem of input split dc-link voltage balancing. For space vector technique, the most popular technologies are different variations of a virtual space vector PWM (VSVPWM). This modulation concept leads to effective control of the dc-link voltage and reduced common-mode voltage (CMV), [20]. The main disadvantages of the balancing scheme based on virtual vector approach are various characteristics under different modulation index and power factor values. The higher the modulation impact is, the slower the DC-link voltage balancing is. Another approach to control the DC-link voltage is to use different types of controllers. This approach could be utilized by both modulation techniques, SVPWM and SPWM. The basic solution is a proportional, P, controller utilized as an additional stage in the PWM generation process, proposed in [21]. In the article presented in [22], the proportional resonant (PR) controller was developed. This control approach was aimed at reduction of voltage drifts and as well as voltage ripples. Due to the proposed structure, PR-controller utilizes two coefficients; similar to the conventional PI controller, but with an additional integrator block. These parameters depend on the duty cycle of small vectors and neutral point current, [22]. Just as different modifications of space vector modulation algorithms were presented, many variations of carrier-based modulation algorithms were proposed for the multilevel diode-clamped inverters, [23]-[25].
Natural balancing effect can be used for dc-link voltage control without any additional control scheme. However, it can be applied only in proper conditions. Two approaches for natural balancing exist: use of additional RLC balancing circuit, [26], and utilization of hybrid modulation method, [27].

This paper presents the concept of natural balancing in a single-phase T-type inverter shown in Fig. 1. The natural balancing of the split dc-link capacitor voltages for this inverter is achieved by the injection of balancing signal to the modulating signal. This work is organized as follows. Modulation method and natural balancing of the neutral-point voltage is presented in section 2. The comparative analysis with existing modulation method, simulation and experimental verifications are presented in section 3. Conclusions are drawn in section 4.

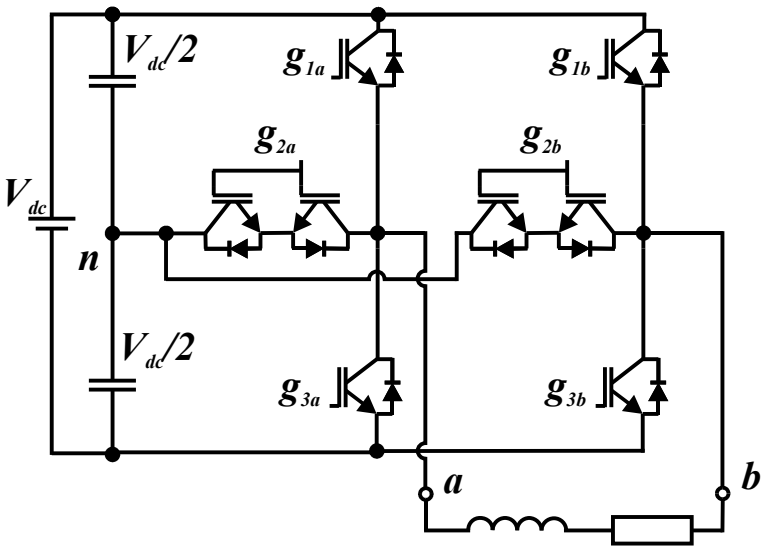

Fig. 1: Single-phase, five-level T-type inverter power circuit

Sinusoidal PWM with natural DC-link balancing

The simplified control block scheme of the modulation method is shown in Fig. 2. The index *i* is the phase-leg number/notation, *i=a,b*. Sinusoidal reference waveforms, *SIN*, and balancing injection signal, *NPB*, are obtained using (1) and (2).

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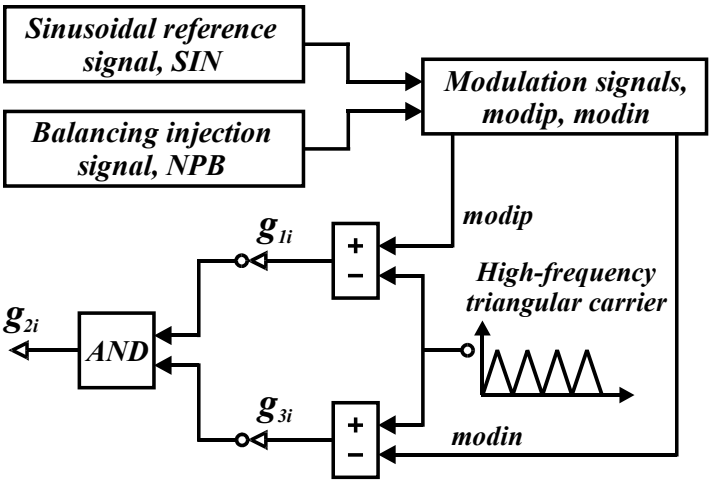

Fig. 2: Proposed SPWM control block scheme

$$SIN = m \cdot \sin(\omega \cdot t) \tag{1}$$

where m is a modulation index and ω is the fundamental output frequency.

$$NPB = B_p \cdot i_o \tag{2}$$

where i_o is an output current and B_p is a balancing component of the injected signal. The structure of the B_p signal is similar to proportional regulator and value of B_p could be obtain using (3).

$$B_p = k_p \cdot (\mathrm{V}_{C1} - \mathrm{V}_{C2}) \tag{3}$$

where k_p is a gain coefficient and V_{C1} and V_{C2} are lower and upper capacitor voltages.

The modulation signals block receives reference sinusoidal signal, *SIN*, and balancing component, *NPB*. This block computes two signals, *modip* and *modin*, per each inverter leg. Modulation signal generating at this step is expressed in (4).

$$\begin{aligned} &if\,(SIN > 0) \\ &modap = SIN + NPB;\ modan = 1; \\ &modbp = 0;\ modbn = 1 - SIN - NPB; \\ &else: modap = 0;\ modan = 1 + SIN + NPB; \\ &modbp = -SIN - NPB;\ modbn = 1; \end{aligned} \tag{4}$$

At the last step, modulation signals are compared with triangular carrier signal, *T*; whose peak values are 0 and 1. The comparison equations that generate the gating signals are expressed in (5).

$$g_{1i} = modip > T;\ g_{3i} = modin < T;\ g_{2i} = !g_{1i}\ AND\ !g_{3i}; \tag{5}$$

Finally, three gating signals per one leg are generated. The switching sequence generated in such way provides a high-quality output voltage and current waveforms; and efficient neutral-point balancing.

Simulation and experimental verification

To verify the effectiveness and performance of the proposed modulation technique, simulation studies were conducted and experimental prototype was built. The power and logic circuit models of the inverter topology in Fig. 1 and the proposed control scheme were derived in PLECS software simulation

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environment. Capacitances of the DC-link capacitors are 750 μF, the switching frequency is 5 kHz and the dc-link voltage is 400 V. An RL load, 20 Ω and 20 mH, is connected at the inverter output terminals. Using the proposed modulation scheme, Fig. 3 shows the simulated inverter output voltage and current waveforms; along with the input split capacitor voltages' variations. With the same circuit parameters, classical control method was deployed in the inverter control; corresponding input and output waveforms are also shown in Fig. 3. Therein, the dynamic performances of these control approaches are displayed.

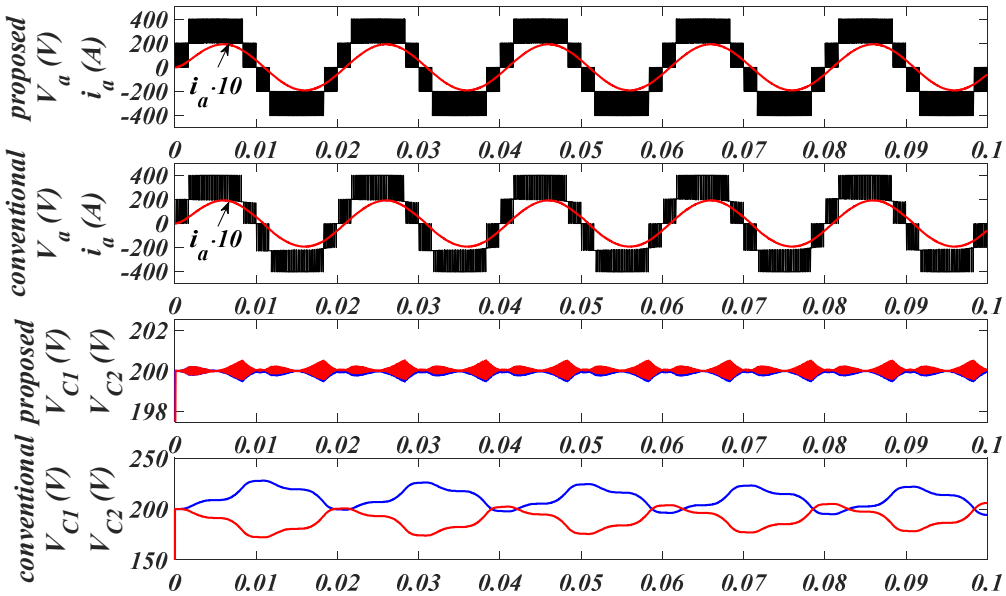

Fig. 3: Simulated output voltage, current and dc-link capacitor voltages waveforms for proposed and conventional modulation techniques.

The FFT analysis of the output current and voltage waveform is shown in Fig. 4. The harmonic performance of the proposed modulation method provides better THD value of the current, 0.34% compare to 1,1% for conventional method. The THD values of the output voltage are relatively similar, 26.55% for proposed and 27,0% for conventional method.

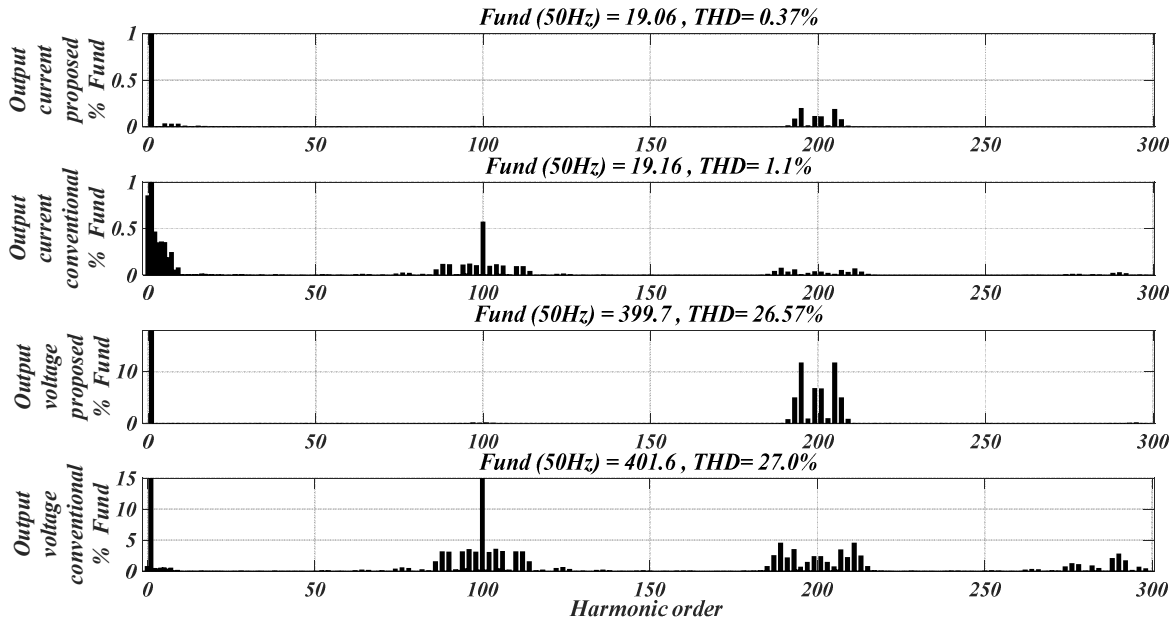

Fig. 4: Simulated output voltage, current and dc-link capacitor voltages waveforms for proposed and conventional modulation techniques.

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To validate the effectiveness of the proposed modulation strategy, experimental study was conducted using single phase T-type experimental prototype. Table I gives the main prototype parameters. The Altera Cyclone II FPGA and ADSP21363L DSP processor were utilized to implement the proposed modulation scheme.

Table I: Prototype specification

	Specification
Capacitor bank	1100μF, 600V
RL load	40Ω, 20mH
Switching frequency	5kHz
Fundamental frequency	50Hz
DC-link voltage	400V
Power switches	AIKW50N60C

Using the proposed modulation scheme, Fig. 5 shows the experimental inverter output voltage and current waveforms; along with the input split capacitor voltages' variations. Modulation index was set to 0.8 and dc-link voltage value is 400 V.

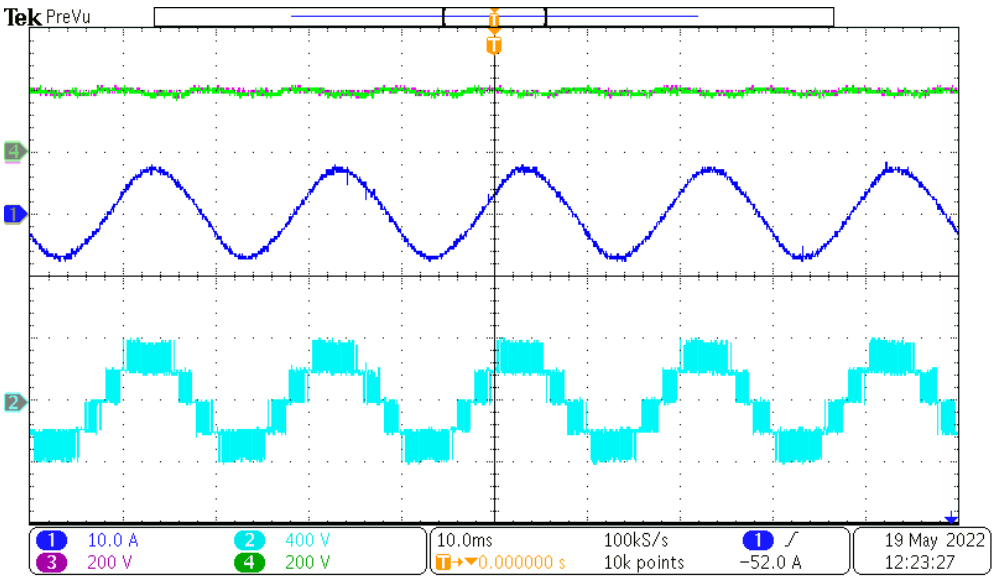

Fig. 5: Experimental output voltage, current and dc-link capacitor voltages waveforms for proposed modulation technique.

The dynamic performance of the proposed control approach, under step changes in the modulation index, is shown in Fig. 6. The modulation index value was changed from 0.8 to 0.4 and back to 0.8.

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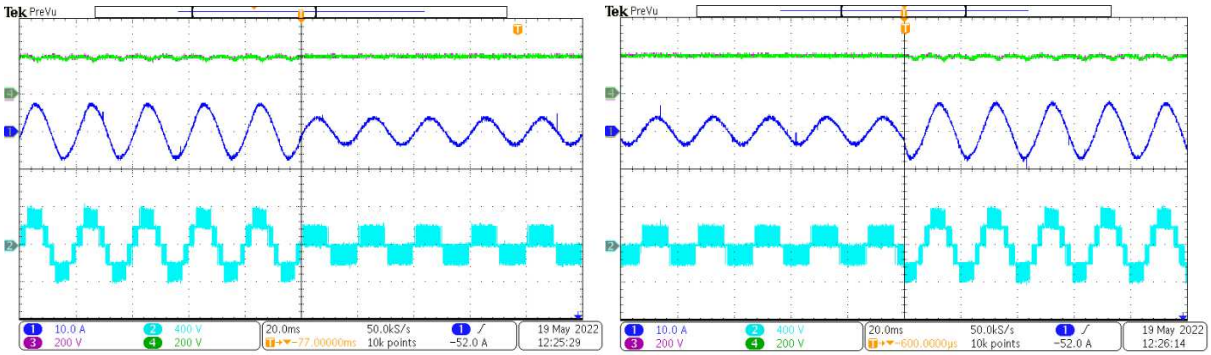

Fig. 6: Simulated output voltage, current and dc-link capacitor voltages waveforms for proposed and conventional modulation techniques.

Fig. 7 shows the balancing effectiveness of the proposed modulation strategy during the experimental verification studies.

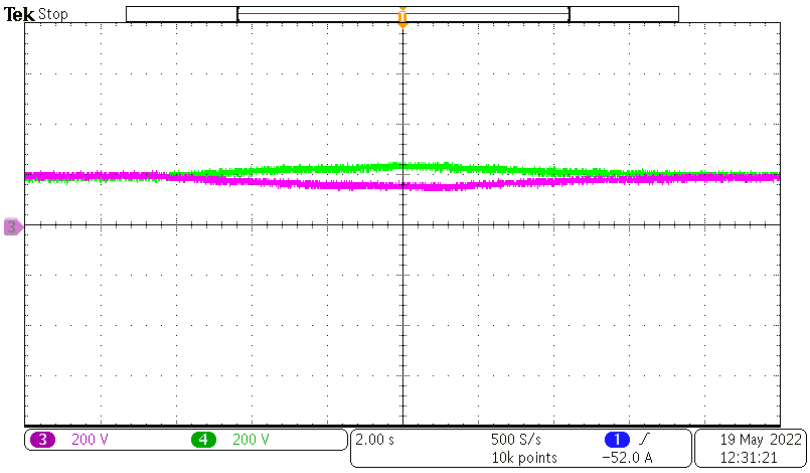

Fig. 7: DC-link capacitor voltages' variation without and with the neutral-point voltage balancing component.

Conclusion

Presented in this paper is a novel SPWM technique for single-phase, T-type inverter characterized by effective input split capacitor natural voltage balancing and reduced capacitor voltage variations. The proposed modulation strategy allows the minimization of number of regulators in the neutral-point voltage control scheme. The good performances shown in comparison with conventional modulation strategies validate the effectiveness and prospects of this control approach. Simulation results have been provided that show the effectiveness of the natural balancing in the proposed modulation technique for three-level, single-phase, T-type inverter. Experimental validations have been performed on a prototype inverter. Obtained experimental output waveforms matched in all respect with those of simulation studies.

References

[1] S. Amamra, K. Meghriche, A. Cherifi and B. Francois, "Multilevel Inverter Topology for Renewable Energy Grid Integration," in IEEE Transactions on Industrial Electronics, vol. 64, no. 11, pp. 8855-8866, Nov. 2017, doi: 10.1109/TIE.2016.2645887.

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[2] T. D. Nguyen, Phan Quoc Dzung, D. N. Dat and N. H. Nhan, "The carrier - based PWM method to reduce common-mode voltage for three - level T - type neutral point clamp inverter," 2014 9th IEEE Conference on Industrial Electronics and Applications, 2014, pp. 1549-1554, doi: 10.1109/ICIEA.2014.6931415.

[3] R. Stala, "Application of Balancing Circuit for DC-Link Voltages Balance in a Single-Phase Diode-Clamped Inverter With Two Three-Level Legs," in IEEE Transactions on Industrial Electronics, vol. 58, no. 9, pp. 4185-4195, Sept. 2011, doi: 10.1109/TIE.2010.2093477.

[4] J. Chen, C. Zhang, A. Chen, X. Xing and F. Gao, "A Carrier-Based Fault-Tolerant Control Strategy for T-Type Rectifier With Neutral-Point Voltage Oscillations Suppression," in IEEE Transactions on Power Electronics, vol. 34, no. 11, pp. 10988-11001, Nov. 2019, doi: 10.1109/TPEL.2019.2900496.

[5] S. Kouro et al., "Recent Advances and Industrial Applications of Multilevel Converters," in IEEE Transactions on Industrial Electronics, vol. 57, no. 8, pp. 2553-2580, Aug. 2010, doi: 10.1109/TIE.2010.2049719.

[6] A. Nabae, I. Takahashi and H. Akagi, "A New Neutral-Point-Clamped PWM Inverter," in IEEE Transactions on Industry Applications, vol. IA-17, no. 5, pp. 518-523, Sept. 1981, doi: 10.1109/TIA.1981.4503992.

[7] B. Fuld, "Aufwandsarmer Thyristor-Dreistufen-Wechselrichter mit geringen Verlusten," in etzArchiv, vol. 11, pp. 261-264, VDE-Verlag, Berlin, Germany, 1989.

[8] C. I. Odeh, A. Lewicki, M. Morawiec and D. Kondratenko, "Three-Level F-Type Inverter," in IEEE Transactions on Power Electronics, vol. 36, no. 10, pp. 11265-11275, Oct. 2021, doi: 10.1109/TPEL.2021.3071359.

[9] M. Schweizer and J. W. Kolar, "Design and Implementation of a Highly Efficient Three-Level T-Type Converter for Low-Voltage Applications," in IEEE Transactions on Power Electronics, vol. 28, no. 2, pp. 899-907, Feb. 2013, doi: 10.1109/TPEL.2012.2203151.

[10] J. Pou, J. Zaragoza, S. Ceballos, M. Saeedifard and D. Boroyevich, "A Carrier-Based PWM Strategy With Zero-Sequence Voltage Injection for a Three-Level Neutral-Point-Clamped Converter," in IEEE Transactions on Power Electronics, vol. 27, no. 2, pp. 642-651, Feb. 2012, doi: 10.1109/TPEL.2010.2050783.

[11] W. Srirattanawichaikul, Y. Kumsuwan, S. Premrudeepreechacharn and B. Wu, "A carrier-based PWM strategy for three-level neutral-point-clamped voltage source inverters," 2011 IEEE Ninth International Conference on Power Electronics and Drive Systems, 2011, pp. 948-951, doi: 10.1109/PEDS.2011.6147369.

[12] A. Videt, P. Le Moigne, N. Idir, P. Baudesson and X. Cimetiere, "A New Carrier-Based PWM Providing Common-Mode-Current Reduction and DC-Bus Balancing for Three-Level Inverters," in IEEE Transactions on Industrial Electronics, vol. 54, no. 6, pp. 3001-3011, Dec. 2007, doi: 10.1109/TIE.2007.907001.

[13] N. Li, Y. Wang, R. Niu, W. Guo, W. Lei and Z. Wang, "A novel neutral point voltage automatic balancing carrier-based modulation strategy of three-level NPC converter," 2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA), 2014, pp. 475-479, doi: 10.1109/IPEC.2014.6869626.

[14] S. Bo, L. Xinyi, L. Wanting, Z. Hui and L. Ning, "A New Carrier Based Neutral Point Potential Control Strategy for Three-Level NPC Converter," 2018 IEEE 4th Information Technology and Mechatronics Engineering Conference (ITOEC), 2018, pp. 427-431, doi: 10.1109/ITOEC.2018.8740588.

[15] S. Busquets-Monge, J. Bordonau, D. Boroyevich and S. Somavilla, "The nearest three virtual space vector PWM - a modulation for the comprehensive neutral-point balancing in the three-level NPC inverter," in IEEE Power Electronics Letters, vol. 2, no. 1, pp. 11-15, March 2004, doi: 10.1109/LPEL.2004.828445.

[16] H. Lin et al., "A Simplified 3-D NLM-Based SVPWM Technique With Voltage-Balancing Capability for 3LNPC Cascaded Multilevel Converter," in IEEE Transactions on Power Electronics, vol. 35, no. 4, pp. 3506-3518, April 2020, doi: 10.1109/TPEL.2019.2938606.

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[17] F. Guo, T. Yang, S. Bozhko and P. Wheeler, "A Novel Virtual Space Vector Modulation Scheme for Three-Level NPC Power Converter with Neutral-Point Voltage Balancing and Common-Mode Voltage Reduction for Electric Starter/Generator System in More-Electric-Aircraft," 2019 IEEE Energy Conversion Congress and Exposition (ECCE), 2019, pp. 1852-1858, doi: 10.1109/ECCE.2019.8913186.

[18] C. Xia, G. Zhang, H. Shao and Y. Zhang, "Hybrid space vector PWM strategy for three-level NPC inverters with optimal extension mode," IECON 2014 - 40th Annual Conference of the IEEE Industrial Electronics Society, 2014, pp. 4649-4655, doi: 10.1109/IECON.2014.7049203.

[19] B. Fan, W. -g. Zhao, W. Yang and R. -q. Li, "A simplified SVPWM algorithm research based on the neutral-point voltage balance for NPC three-level inverter," 2012 IEEE International Conference on Automation and Logistics, 2012, pp. 150-154, doi: 10.1109/ICAL.2012.6308188.

[20] C. Hu et al., "An Improved Virtual Space Vector Modulation Scheme for Three-Level Active Neutral-Point-Clamped Inverter," in IEEE Transactions on Power Electronics, vol. 32, no. 10, pp. 7419-7434, Oct. 2017, doi: 10.1109/TPEL.2016.2621776.

[21] H. Kitidet and Y. Kumsuwan, "A CB-SVPWM control strategy for neutral-poin voltage balancing in three-level NPC inverters," TENCON 2017 - 2017 IEEE Region 10 Conference, 2017, pp. 1766-1771, doi: 10.1109/TENCON.2017.8228144.

[22] X. Lin, S. Gao, J. Li, H. Lei and Y. Kang, "A new control strategy to balance neutral-point voltage in three-level NPC inverter," 8th International Conference on Power Electronics - ECCE Asia, 2011, pp. 2593-2597, doi: 10.1109/ICPE.2011.5944742.

[23] U. A. Sipai and P. N. Tekwani, "Capacitor Voltage Balancing for Five-Level Neutral-Point Clamped Inverter using Modified Carrier Waves for Carrier-Based PWM Technique," 2019 IEEE 16th India Council International Conference (INDICON), 2019, pp. 1-4, doi: 10.1109/INDICON47234.2019.9028994.

[24] Logapriya J. and S. Mohamedyousuf, "Improved multilevel inverter with neutral point potential balancing for high power application," 2015 International Conference on Innovations in Information, Embedded and Communication Systems (ICIIECS), 2015, pp. 1-6, doi: 10.1109/ICIIECS.2015.7192987.

[25] Y. Li, Y. W. Li, H. Tian, N. R. Zargari and Z. Cheng, "A Modular Design Approach to Provide Exhaustive Carrier-Based PWM Patterns for Multilevel ANPC Converters," in IEEE Transactions on Industry Applications, vol. 55, no. 5, pp. 5032-5044, Sept.-Oct. 2019, doi: 10.1109/TIA.2019.2928240.

[26] R. Stala, "A Natural DC-Link Voltage Balancing of Diode-Clamped Inverters in Parallel Systems," in IEEE Transactions on Industrial Electronics, vol. 60, no. 11, pp. 5008-5018, Nov. 2013, doi: 10.1109/TIE.2012.2219839.

[27] M. Aly, E. M. Ahmed and M. Shoyama, "Modulation Method for Improving Reliability of Multilevel T-Type Inverter in PV Systems," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 2, pp. 1298-1309, June 2020, doi: 10.1109/JESTPE.2019.2898105.

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