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Space-Vector Pulse Width Modulation for Three-Level NPC Converter with the Neutral Point Voltage Control

Arkadiusz Lewicki, Zbigniew Krzeminski, Haitham Abu-Rub

***Abstract*— This paper proposes new space-vector pulse width modulation (SV-PWM) strategy for a three-level NPC inverter. The presented SV-PWM strategy makes it possible to control the neutral point voltage by optimum choice of switch sequence for any position and length of output voltage vector. The proposed solution takes into consideration the unbalance of the DC-link voltages. It also analyzes the influence of vector sequences on the predicted unbalance of the DC-link voltage. The solution allows selecting optimum vectors and their on-time durations in order to reduce quickly the DC-link voltage unbalance. The calculation of space vector area, proposed in this paper takes into consideration voltage unbalance and its influence on the length and position of vectors. The proposed approach assures properly generating the voltage output vectors, even in the case of the existing large voltage unbalance in the DC-link. Results of experimental investigation of the proposed modulation strategy are presented in the paper.**

***Index Terms*— Multilevel Inverter, NPC Inverter, Pulse Width Modulation, Neutral Point Voltage Control**

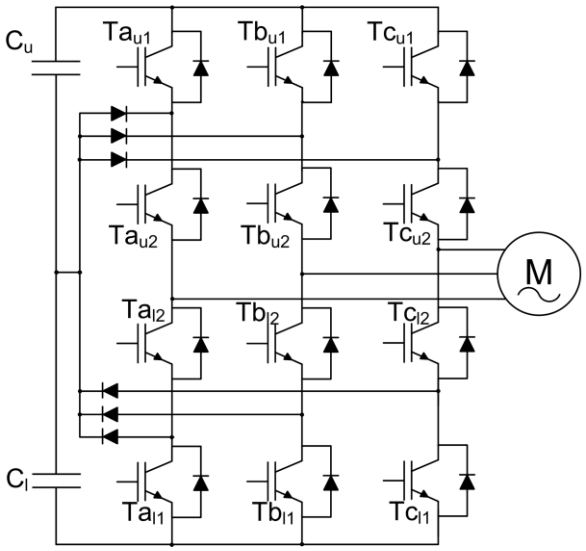

Fig. 1. Three-phase NPC inverter

I. Introduction

MULTILEVEL inverter topologies are experiencing increased application in the industrial environment, particularly in high power drive systems [1, 2, 3, 4]. The main advantages of these inverters are improving quality of voltage waveforms and an increase in the DC-link voltage for a given blocking voltage capacity of the semiconductors. Generation of voltage vectors in multilevel inverters requires taking into consideration all the phenomena which have an influence on the accuracy of output vectors. While the neutral point clamped (NPC) multilevel inverter (Fig.1) converts higher voltages using devices with lower rating, the DC-link voltage balancing problem seriously limits the applicability of these inverters, if not solved. The DC-link voltage unbalance causes an increase of voltage stress on switching devices and additional harmonic distortion in the inverter output voltage. To maximize the performance of three-level inverter, the voltages of the series connected DC-link capacitors should be equal.

Different methods of DC-link voltage balance control are proposed in many papers [5, 6, 7, 8, 9, 10, 11, 12, 13, 14]. In most solutions of the PWM strategies, the lengths of active and passive vectors, with an assumption of balanced DC-link voltages, are calculated. This approach allows to divide the space vector area into six equal sectors (Fig.2). Each of them can be divided into equal subsectors. In many solutions of the SV-PWM strategies for three-level NPC inverter, one or two switching sequences are strictly assigned to specific subsectors [5, 6]. The control strategies of DC-link voltage balance are based on the change of switching sequences depending on the DC-link voltage unbalance [7, 15, 16, 17]. Most of the PWM solutions are based on using controllers to control neutral point voltages [8, 18, 19, 20, 21]. The duration of redundant vectors in the switching sequence is rearranged in order to reduce the

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A. LEWICKI is with Electrical and Control Engineering Department, Gdansk University of Technology, ul. G. Narutowicza 11/12, 80-233 Gdansk, POLAND, (phone: +48-58-347-11-76; fax: +48-58-341-08-80; e-mail: alewicki@ely.pg.gda.pl).

Z. KRZEMINSKI is with Electrical and Control Engineering Department, Gdansk University of Technology, ul. G. Narutowicza 11/12, 80-233 Gdansk, POLAND, (e-mail: zkrzem@ely.pg.gda.pl).

H. ABU-RUB is with the Electrical and Computer Engineering Department, Texas A&M University at Qatar, (e-mail: haitham.abu-rub@qatar.tamu.edu).

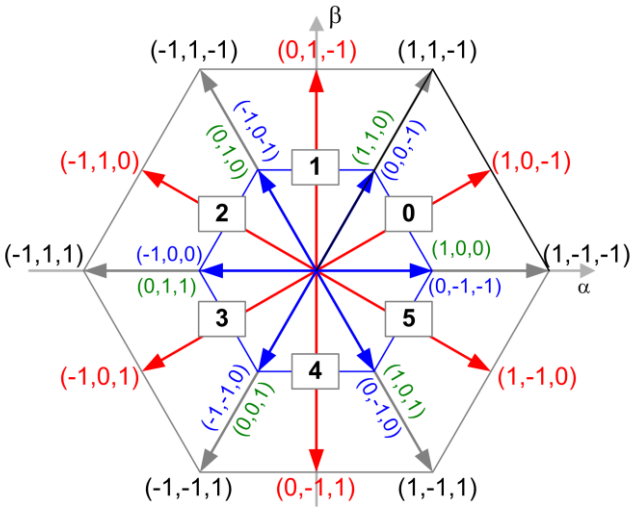

Fig. 2. Space vectors of three-level inverter in the case of DC-link balance: u_{cu}/u_{cl}=0.5/0.5

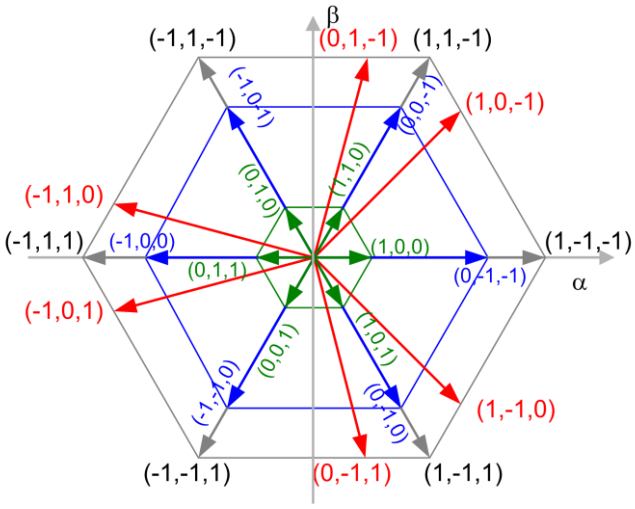

Fig.3 Space vectors of three level inverter in the case of DC-link unbalance occurrence: u_{cu}/u_{cl}=0,3/0,7

voltage unbalance in the DC-link [7, 9, 15, 16, 22, 23, 24]. A similar solution was proposed in [25]. The voltage balance control strategy for one-phase NPC converter is based on the adjusting of effective time of the positive and the negative small vectors in response to the DC-link voltage unbalance and the direction of the load current.

In the case of unbalanced DC-link voltages, the approach, based on assumption of equal voltages in the DC-link may be a reason of incorrect output voltage vector generation. A corrective method of vector duration dependent on the DC-link voltage unbalance was proposed in [26]. The PWM strategy, proposed in [26], takes into consideration the influence of DC-link voltage unbalance on the length and position of active vectors in the space vector area. The DC-link voltage unbalance is reduced by appropriate choice of redundant vectors due to direction of neutral point current and voltage unbalance on the DC-link capacitors. The calculation of active vectors duration considers the actual difference between voltages on upper and lower DC-link capacitors. The influence on medium voltage vector, used in a switching sequence, on DC-link voltage unbalance is compensated in next steps of the proposed algorithm.

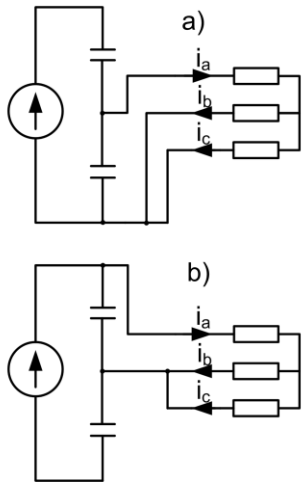

Fig.4. Influence of redundant vectors: (0,-1,-1) a) and (1,0,0) b) on DC-link voltages.

The modulation strategy, proposed in [27] for single-phase multilevel cascaded converter, takes into consideration movement of voltage vectors in switching sequence due to the voltage unbalance. The proposed solution makes it possible to properly generate an output voltage in the case of large voltage unbalance occurring on DC-link capacitors. The strategy to balance the DC-link voltages based on appropriate choice of switching sequence depends on the actual voltage unbalance and direction of output current.

A similar strategy for the DC-link unbalance compensation for three-phase NPC-converter was proposed in [28]. In this paper the influence of the DC-link unbalance on length and position of voltage vectors in three-dimensional control region was presented. The appropriate choice of switching sequence and duration times due to the DC-link voltages in [28] permits properly generating the converter output voltage.

The control of DC-link unbalance in NPC converter can be realized using different algorithms, proposed in many papers. The common property of these strategies is the application of redundant vectors as the "unbalance-controlled" vectors. The main limitations of commonly used strategies are:

-stiff sector division: only one switching sequence to any sector is assigned. It is not possible to choice other switching

TABLE I
THE VOLTAGES BETWEEN A MOTOR CLAMP "X" (X=A,B,C) AND DC-LINK NEUTRAL POINT "N" AND THE ACTIVATION SIGNALS FOR "X" PHASE TRANSISTORS

Activation signals for upper (u) and lower (l) transistors in phase "x" Tx_{u1},Tx_{u2}, Tx_{l2},Tx_{l1}	u_{xn}	Description of transistor state for a "x" phase
1 , 1 , 0 , 0	uc_u	1
0 , 0 , 1 , 1	-uc_l	-1
0 , 1 , 1 , 0	0	0

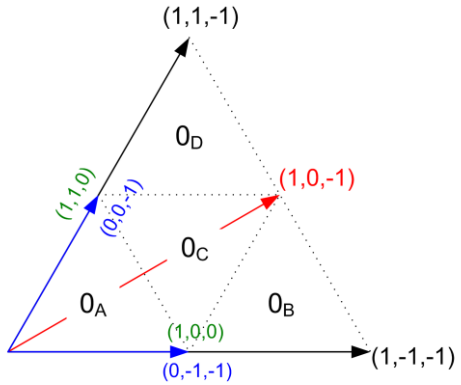

Fig.5. Sector and subsectors in space vector area.

sequence, which will reduce the voltage unbalance faster.

- no voltage unbalance prediction –commonly used strategies don't take into consideration the influence of medium vectors on DC-link voltage unbalance. The balancing algorithms are based on actual measured voltage unbalance, while it is possible to predict the voltage unbalance for any switching sequence before its activation,
- the activation times of redundant vectors are usually set by controllers. It is possible to precisely calculate the duration of compensation vectors.

In this paper a new SV-PWM strategy is proposed. The presented solution makes it possible to generate the desired inverter output voltage vector, independently of the DC-link voltage unbalance. The analysis of the DC-link voltage unbalance on parameters of voltage vectors in two-dimensional control region is realized. As distinct from other existing modulation strategies, the choice of vectors in switching sequence and the calculations of vector duration takes into consideration predicted voltage unbalance in the DC-link. The prediction algorithm for the DC-link voltage unbalance takes into consideration an influence of all active vectors in a switching sequence, before their activation. The prediction of voltage unbalance for all possible switching sequences is performed and the optimum switching sequence is realized.

The durations of redundant vectors are calculated in relation to the neutral point current, DC-link voltage unbalance, selected switching sequence, and DC-link capacity. The introduction of the DC-link capacity to the compensation algorithm allows calculating exact duration of redundant vectors, which makes the reduction of voltage unbalance very fast.

II. Pulse Width Modulation For Three-Level NPC Inverter

It is possible to switch-on only two transistors at the same time in any phase of a three-level NPC inverter. In the upper leg there are Tx_{u1}, Tx_{u2}, in the lower leg: Tx_{l2}, Tx_{l1}, and in the middle leg: Tx_{u2}, and Tx_{l2}. ("x" denotes the inverter phase (a, b or c)). The voltages between the induction motor clamp and DC-link neutral point for any transistor combination and state

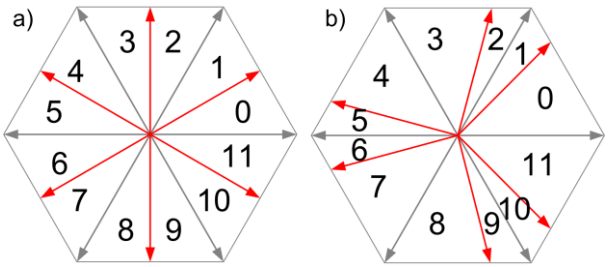

Fig.6. Proposed sector division of space vector area in the case of balance (u_{cu}/u_{cl}=0.5/0.5) a) and unbalance (u_{cu}/u_{cl}=0.3/0.7) b) of DC link voltages .

description are presented in table 1. The length and position of large active vectors: (1,-1,-1), (1,1,-1), (-1,1,-1), (-1,1,1), (-1,-1,1), (1,-1,1) and passive vectors: (111), (000), (-1,-1,-1) do not depend on the DC-link voltage unbalance. Activating these vectors has no influence on the DC-link unbalance occurrence. Activation of one of the redundant vectors: (1,0,0), (0, -1,-1), (1,1,0), (0,0,-1), (0,1,0), (-1,0,1), (0,1,1), (-1,0,0), (0,0,1), (-1,-1,0), (1,0,1), (0,-1,0) or one of medium active vectors (1,0,-1), (0,1,-1), (-1,1,0), (-1,0,1), (0,-1,1), (1,-1,0) connects the motor clamps to the DC-link neutral point and has an impact on the voltage change on DC-link capacitors (fig.4). The changes of voltages on upper and lower DC-link capacitors can be estimated from:

$$u_c(t) = \frac{1}{2C}\int_0^t i(\tau)\,d\tau + u_c(0), \qquad (1)$$

where C - DC-link capacity ($C=C_u=C_l$), u_c - voltage on the upper capacitor of DC-link, $i(\tau)$ – neutral point current, τ - the duration of redundant or medium vectors.

The amplitude and position of the redundant and medium vectors depend on the DC-link voltage unbalance (Fig.2 and Fig.3). Activating one of the medium vectors gives no possibility to full control of neutral point voltage – the length of medium vector, used in switching sequence, depends on position and amplitude of the inverter output voltage. The direction of the neutral point current can be controlled only if redundant vectors are used in switching sequence – the direction of neutral point current can be changed by substituting redundant vector for an equivalent vector. For example, during activation of redundant vector (0,-1,-1), the "a" phase current is a neutral point current. Positive current direction charges the upper capacitor and discharges the lower capacitor in the DC-link. The substitution of redundant vector (0,-1,-1) for an equivalent vector (1,0,0) will cause discharging of the upper capacitor and charging of the lower one (Fig. 4). Typical switching sequence contains two or more redundant vectors. The switching sequences, proposed in [7]

$$(1,0,0)\rightarrow(1,0,-1)\rightarrow(0,0,-1)\rightarrow(0,-1,-1), \qquad (2)$$

$$(1,1,0)\rightarrow(1,0,0)\rightarrow(1,0,-1)\rightarrow(0,0,-1), \qquad (3)$$

contains a pair of redundant vectors: (0,0,-1) in (2) and (1,0,0) in (3), which have an opposite influence on DC-link voltage balance. The control of neutral current can be done by choosing one of sequences (2)-(3), depending on the DC-link voltage unbalance.

In the SV-PWM strategies for three-level inverters, the space vector area is usually divided into six sectors, limited by large active vectors (Fig.2) . Each sector can be divided into subsectors, as shown in Fig. 5 [5, 6, 29, 30]. In many solutions of SV-PWM strategies, the switching sequences are strictly defined for subsectors. For example, in [6] the switching sequences for subsectors 0_A-0_C were defined as:

0_A:

$$\begin{aligned}&(-1,-1,-1)\rightarrow(0,-1,-1)\rightarrow(0,0,-1)\rightarrow\\&(0,0,0)\rightarrow(1,0,0)\rightarrow(1,1,0)\rightarrow(1,1,1)\end{aligned}, \quad (4)$$

0_B:

$$(0,-1,-1)\rightarrow(1,-1,-1)\rightarrow(1,0,-1)\rightarrow(1,0,0), \quad (5)$$

0_C:

$$(0,-1,-1)\rightarrow(0,0,-1)\rightarrow(1,0,-1)\rightarrow(1,0,0)\rightarrow(1,1,0), \quad (6)$$

In this case, the neutral-point voltage can be controlled by rearranging the duration of redundant vectors [6, 7, 16, 22]. The neutral point voltages can be adjusted using controllers [8], where the difference between voltage on the upper u_{cu} and lower u_{cl} capacitors (fig.1):

$$\Delta u = u_{Cu} - u_{Cl}\,, \quad (7)$$

is used as a feed-back signal.

III. Proposed SV-PWM Strategy

In three-phase NPC inverters the amplitude and position of active vectors depend on the DC-link voltage unbalance. The sector division proposed in this paper takes into account the change of position and length of the active vector. The space vector area contains twelve sectors, as shown in Fig.6. This approach properly assigns a position of the output voltage vector to a sector, even in the case of large unbalance in DC-link. This strategy requires recalculation of the lengths and positions of the redundant and medium vectors and requires redefinition of the sectors for any PWM cycle. For any of the sectors, there are four switching sequences defined. The vector durations are calculated simultaneously for four sequences. For example, if an output voltage vector takes a position in "0" sector, the durations are calculated for the following sequences:

$$(0,0,0)\rightarrow(1,1,0)\rightarrow(1,0,0)\rightarrow(0,0,0), \quad (8)$$
$$(0,0,0)\rightarrow(0,-1,-1)\rightarrow(0,0,-1)\rightarrow(0,0,0), \quad (9)$$
$$(0,0,0)\rightarrow(1,-1,-1)\rightarrow(1,0,-1)\rightarrow(0,0,0), \quad (10)$$
$$(0,0,0)\rightarrow(1,-1,-1)\rightarrow(1,1,-1)\rightarrow(0,0,0). \quad (11)$$

The switching sequence (11) utilizes only vectors which have no influence on the DC-link voltage balance.

Sequences (8) and (9) contain the active vectors, which have an influence on DC-link voltage unbalance. Activating of these sequences will increase or decrease the voltage unbalance, depending on neutral-point current direction. The amplitude of active vectors, utilized in (8), depends on the voltage on upper capacitor, while the amplitude of active vectors in seq. (9) depends on the voltage on lower capacitor. The amplitude of output voltage vector, generated using sequences (8)-(9), depends on the unbalance of the DC-link voltages and doesn't depend on the output voltage vector position (Fig.3). This permits choosing one of the sequences (8)-(9) in the case of voltage unbalance occurrence, if the amplitude of inverter output voltage is higher than half of the DC-link voltage. The sequences (8)-(9) may be used only in case if the inverter output voltage vector can be inscribed into hexagon, bounded by ends of vectors (1,1,0), (1,0,0),(1,0,1), (0,0,1), (0,1,1), (0,1,0) (for seq.(8)) and vectors (0,0,-1), (0,-1,-1), (0,-1,0), (-1,-1,0), (-1,0,0), (-1,0,-1) (for seq.(9)) (fig. 3). None of these sequences can be used if their activation increases the DC-link voltage unbalance.

Sequence (10) contains only one vector, which has an influence on the DC-link voltage balance. Additionally, the position and amplitude of the medium vector (1,0,-1) depend on voltage unbalance (fig.3). The vector components of (1,0,-1) vector can be calculated as:

$$\begin{aligned}u_{\alpha(1,0,-1)} &= \sqrt{\frac{2}{3}}\left(u_{Cu}+\frac{1}{2}\cdot u_{Cl}\right),\\ u_{\beta(1,0,-1)} &= \frac{\sqrt{2}}{2}u_{Cl}.\end{aligned} \quad (12)$$

Vector components of all active and passive vectors for 3-level NPC inverter can be calculated using following equations:

$$\begin{aligned}u_\alpha &= \sqrt{\frac{1}{6}}\cdot\begin{pmatrix}u_{Cu}\cdot\begin{pmatrix}2\cdot(Ta_{u1}\cdot Ta_{u2})-\\(Tb_{u1}\cdot Tb_{u2})-(Tc_{u1}\cdot Tc_{u2})\end{pmatrix}\\-u_{Cl}\cdot\begin{pmatrix}2\cdot(Ta_{l2}\cdot Ta_{l1})-\\(Tb_{l2}\cdot Tb_{l1})-(Tc_{l2}\cdot Tc_{l1})\end{pmatrix}\end{pmatrix},\\ u_\beta &= \sqrt{\frac{1}{2}}\cdot\begin{pmatrix}u_{Cu}\cdot((Tb_{u1}\cdot Tb_{u2})-(Tc_{u1}\cdot Tc_{u2}))\\-u_{Cd}\cdot((Tb_{l2}\cdot Tb_{l1})-(Tc_{l2}\cdot Tc_{l1}))\end{pmatrix},\end{aligned} \quad (13)$$

Where $Tx_{(u,l)(1,2)}$ denotes the signals of transistor activation in phase x (x=(a,b,c)). The values of Tx are: 1 – if transistor is switched-on, 0 – if transistor is switched-off. For example: Ta_{u1}=1 denotes that the first upper transistor in phase "a" is switched on (fig.1)

The choice of switching sequence has to ensure proper generation of the output voltage vector, as well as the minimization of the DC-link voltage unbalance. The control strategy of neutral point voltage should take into consideration the influence of switching sequence on DC-link voltage. For any of the sequences (8)-(11) an unbalance criterion "x" is calculated:

TABLE II
THE REDUNDANT VECTORS INTRODUCED TO SWITCHING SEQUENCES FOR SECTORS 0 AND 3

Sector	Sequence number	Base sequence	Sequence with redundant vectors
0	(8)	$(0,0,0)\rightarrow(1,1,0)\rightarrow(1,0,0)\rightarrow(0,0,0)$	---
	(9)	$(0,0,0)\rightarrow(0,-1,-1)\rightarrow(0,0,-1)\rightarrow(0,0,0)$	---
	(10)	$(0,0,0)\rightarrow(1,-1,-1)\rightarrow(1,0,-1)\rightarrow(0,0,0)$	$(0,0,0)\rightarrow(0,-1,-1)\rightarrow(1,-1,-1)\rightarrow(1,0,-1)\rightarrow(0,0,0)$ or $(0,0,0)\rightarrow(1,-1,-1)\rightarrow(1,0,-1)\rightarrow(1,0,0)\rightarrow(0,0,0)$
	(11)	$(0,0,0)\rightarrow(1,-1,-1)\rightarrow(1,1,-1)\rightarrow(0,0,0)$	$(0,0,0)\rightarrow(0,-1,-1)\rightarrow(1,-1,-1)\rightarrow(1,1,-1)\rightarrow(0,0,0)$ or $(0,0,0)\rightarrow(1,-1,-1)\rightarrow(1,1,-1)\rightarrow(1,1,0)\rightarrow(0,0,0)$
3	(8)	$(0,0,0)\rightarrow(0,1,0)\rightarrow(1,1,0)\rightarrow(0,0,0)$	---
	(9)	$(0,0,0)\rightarrow(-1,0,-1)\rightarrow(0,0,-1)\rightarrow(0,0,0)$	---
	(10)	$(0,0,0)\rightarrow(-1,1,-1)\rightarrow(0,1,-1)\rightarrow(0,0,0)$	$(0,0,0)\rightarrow(-1,0,-1)\rightarrow(-1,1,-1)\rightarrow(0,1,-1)\rightarrow(0,0,0)$ or $(0,0,0)\rightarrow(-1,1,-1)\rightarrow(0,1,-1)\rightarrow(0,1,0)\rightarrow(0,0,0)$
	(11)	$(0,0,0)\rightarrow(1,1,-1)\rightarrow(-1,1,-1)\rightarrow(0,0,0)$	$(0,0,0)\rightarrow(1,1,0)\rightarrow(1,1,-1)\rightarrow(-1,1,-1)\rightarrow(0,0,0)$ or $(0,0,0)\rightarrow(1,1,-1)\rightarrow(-1,1,-1)\rightarrow(-1,0,-1)\rightarrow(0,0,0)$

$$x = x_{pred} + x_{act}\,, \tag{14}$$

where: x_{pred} is the predicted unbalance criterion, calculated for sequences (8)-(11), before their activation:

$$x_{pred} = \sum_{k=1}^{n} t_k \cdot i_k\,,\,, \tag{15}$$

i_k is the neutral point current, specified for k-th vector in considered switching sequence, t_k is the duration of k-th vector, n – is a number of vectors in a switching sequence.

The x_{act} specifies an actual voltage unbalance on the DC-link capacitors and can be determined from (1) as:

$$x_{act} = i_x \cdot t_x = 2 \cdot C \cdot \Delta u\,, \tag{16}$$

where: t_x is the time to balance the voltages in DC-link, when the neutral point current is equal to i_x. Δu is a difference between voltages in the DC-link (7).

The switching sequence (10) is used if the voltage output vector cannot be generated using sequences (8)-(9) because of its amplitude and possibility to voltage unbalance reduction. If the criterion:

$$x = \sum_{k=1}^{n} t_k \cdot i_k + x_{act} = 0\,, \tag{17}$$

is not fulfilled, the redundant vectors should be introduced to (10). The switching sequence (10) can be rewritten as:

$$(0,0,0)\rightarrow(0,-1,-1)\rightarrow(1,-1,-1)\rightarrow(1,0,-1)\rightarrow(0,0,0)\,, \tag{18}$$

or

$$(0,0,0)\rightarrow(1,-1,-1)\rightarrow(1,0,-1)\rightarrow(1,0,0)\rightarrow(0,0,0)\,, \tag{19}$$

depending on the sign of "x" coefficient and direction of the neutral point current:

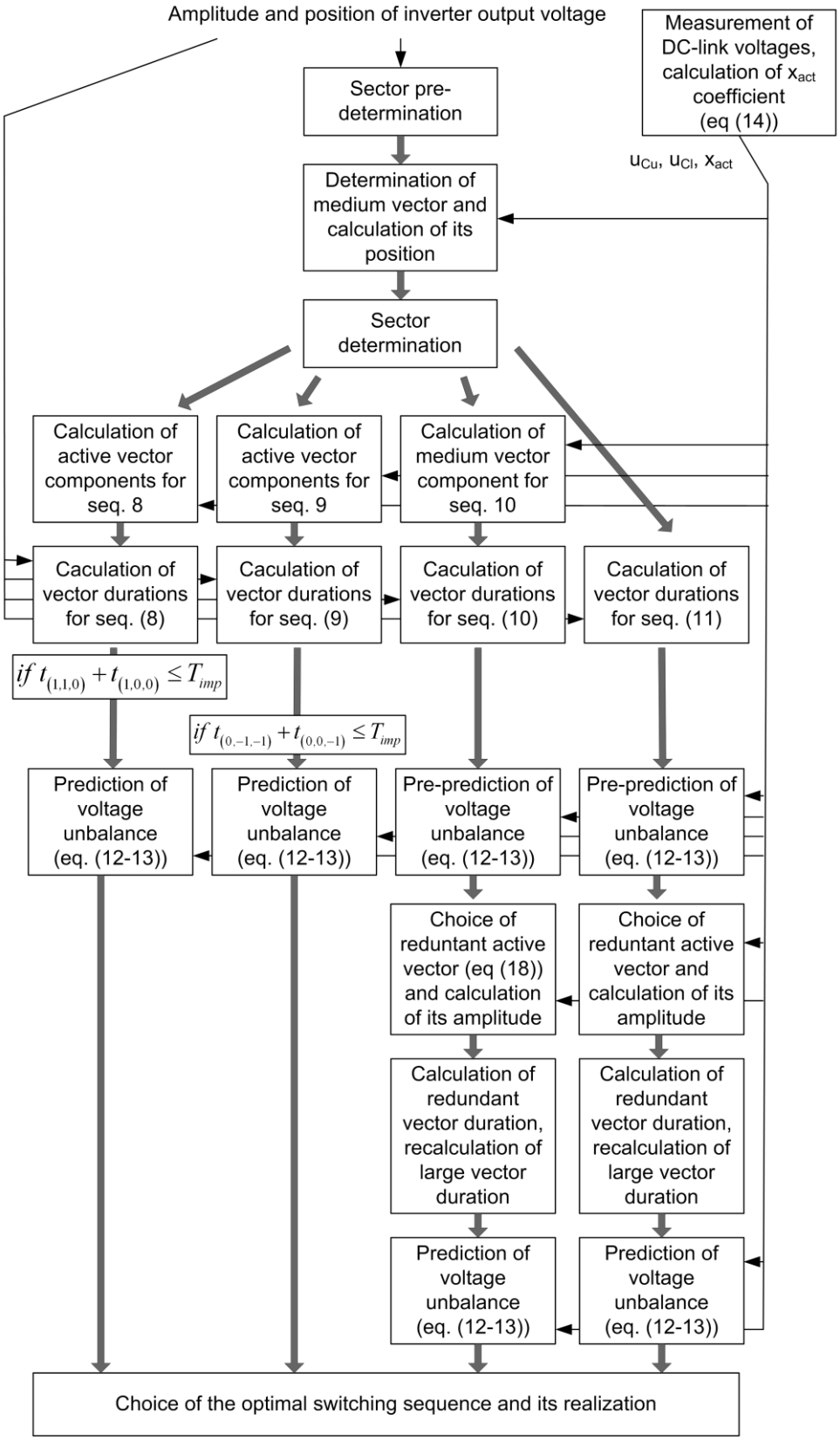

Fig.7. Graphical representation of proposed algorithm

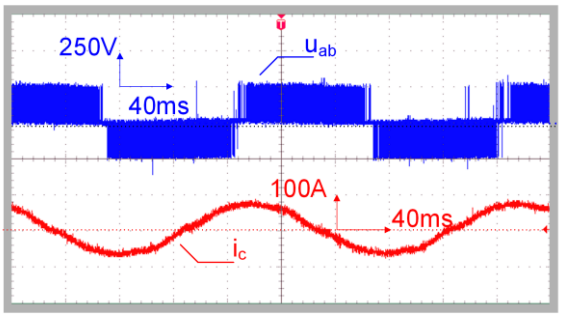

Fig.8. The converter output voltage u_{ab} and phase current i_c during generation of converter output voltage, Fundamental frequency:5[Hz] , Uout=69V, DC-link voltage Udc=520V

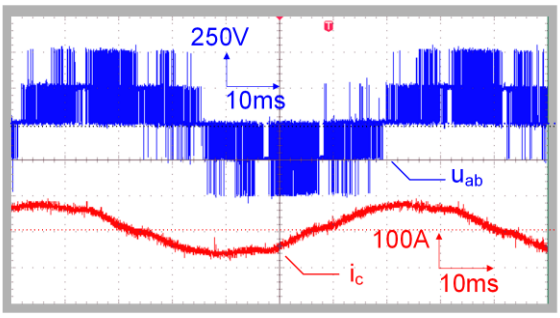

Fig.9. The converter output voltage u_{ab} and phase current i_c during generation of converter output voltage, Fundamental frequency:15[Hz] , Uout=207V, DC-link voltage Udc=520V

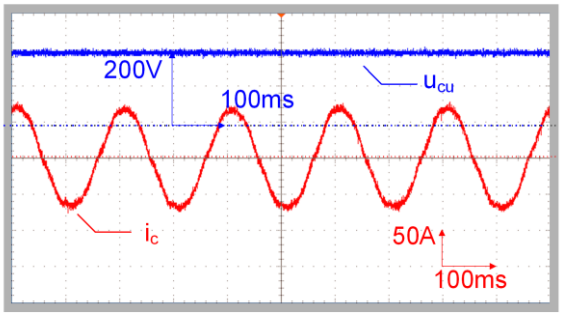

Fig.10. The voltage on upper capacitor of DC-link $u_{cu,}$ and phase current i_c during generation of converter output voltage, Fundamental frequency:5[Hz] , Uout=69V, DC-link voltage Udc=400V

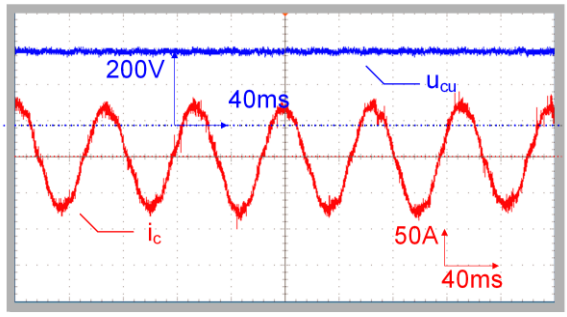

Fig.11. The voltage on upper capacitor of DC-link $u_{cu,}$ and phase current i_c during generation of converter output voltage, Fundamental frequency:15[Hz] , Uout=207V, DC-link voltage Udc=400V

$$\left.\begin{array}{l} i_{(1,0,0)} < 0, x > 0 \\ or \\ i_{(1,0,0)} > 0, x < 0 \end{array}\right\} \Rightarrow (1,0,0), \qquad \left.\begin{array}{l} i_{(0,-1,-1)} < 0, x > 0 \\ or \\ i_{(0,-1,-1)} > 0, x < 0 \end{array}\right\} \Rightarrow (0,-1,-1) \qquad (20)$$

where $i_{(0,-1,-1)}$ and $i_{(1,0,0)}$ are neutral point currents during activation of (0,-1,-1) and (1,0,0) redundant vector respectively. In the presented case, the neutral point current is equal to:

$$\begin{aligned} i_{(0,-1,-1)} &= i_a \\ i_{(1,0,0)} &= -i_a \end{aligned} \qquad (21)$$

where i_a is an "a" phase current.

The position of (0,-1,-1) and (1,0,0) vectors overlaps the position of (1,-1,-1) vector. The duration of redundant vector can be calculated as:

$$t_{(0,-1,-1),(1,0,0)} = abs\left(\frac{x}{i_{(0,-1,-1),(1,0,0)}}\right), \qquad (22)$$

where $t_{(0,-1,-1)}$ and $t_{(1,0,0)}$ are the durations of redundant vectors (0,-1,-1) and (1,0,0) respectively. Activation of redundant vector for calculated time will reduce the unbalance of the DC-link voltages to zero. Introduction of the additional redundant vector to the switching sequence demands correction of the duration of the large, active vector (1,-1,-1). The new duration of the vector (1,-1,-1) can be calculated from:

$$t'_{(1,-1,-1)} = t_{(1,-1,-1)} - t_{(0,-1,-1),(1,0,0)} \cdot \left(\frac{u_{\alpha(0,-1,-1),(1,0,0)}}{u_{\alpha(1,-1,-1)}}\right), \qquad (23)$$

where $t_{(1,-1,-1)}$, $t_{(0,-1,-1)}$, $t_{(1,0,0)}$: durations of (1,-1,-1), (0,-1,-1), (1,0,0) vectors respectively, $u_{\alpha(0,-1,-1)}$, $u_{\alpha(1,0,0)}$, $u_{\alpha(1,-1,-1)}$, - an α component of (1,-1,-1), (0,-1,-1), (1,0,0) vectors in α,β co-ordinate system, $t'_{(1,-1,-1)}$ – new duration of large vector (1,-1,-1).

If the duration of redundant vector, calculated from (22) is too long, the new duration of vector (1,-1,-1) will be negative. In this case the duration of redundant vector should be reduced to:

$$t_{(0,-1,-1),(1,0,0)} = t_{(1,-1,-1)} \frac{u_{\alpha(1,-1,-1)}}{u_{\alpha(0,-1,-1),(1,0,0)}}, \qquad (24)$$

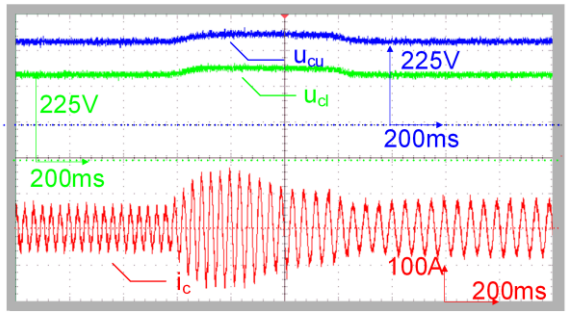

Fig.12. The voltage on upper u_{cu} and the lower u_{cL} capacitor of DC-link $u_{cu,}$ and phase current i_c during speed change of induction motor from 0.6 to 0.4 pu, , DC-link voltage Udc=450V

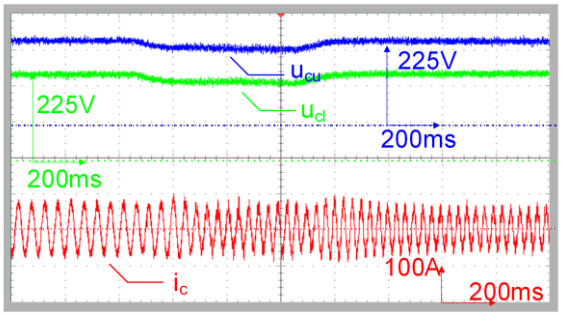

Fig.13. The voltage on upper u_{cu} and the lower u_{cL} capacitor of DC-link $u_{cu,}$ and phase current i_c during speed change of induction motor from 0.4 to 0.6 pu, , DC-link voltage Udc=450V

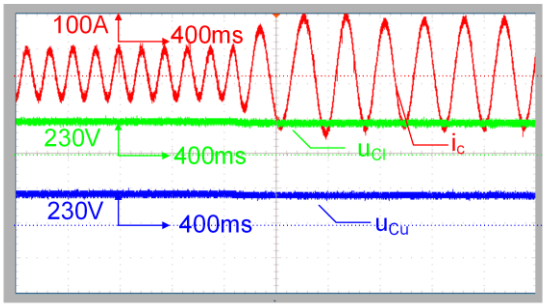

Fig.14. The voltage on upper u_{cu} and the lower u_{cL} capacitor of DC-link $u_{cu,}$ and phase current i_c during load change from 0.05 to 0.45 pu, Fundamental frequency: 5[Hz], DC-link voltage Udc=460V

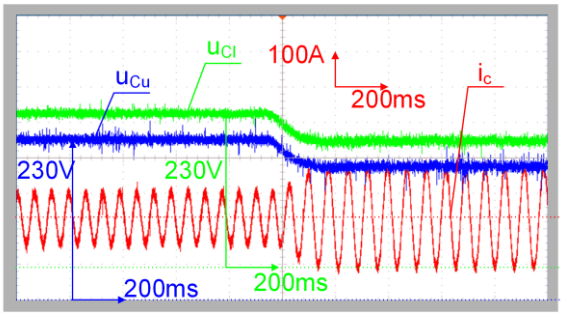

Fig.15. The voltage on upper u_{cu} and the lower u_{cL} capacitor of DC-link $u_{cu,}$ and phase current i_c during load change from 0.05 to 0.45 pu, Fundamental frequency: 15[Hz], DC-link voltage Udc=460V

and the duration of vector (1,-1,-1) should be set to zero. Appropriate switching sequence can be rewritten as:

$$(0,0,0)\rightarrow(0,-1,-1)\rightarrow(1,0,-1)\rightarrow(0,0,0)\,, \qquad (25)$$

or

$$(0,0,0)\rightarrow(1,0,-1)\rightarrow(1,0,0)\rightarrow(0,0,0)\,. \qquad (26)$$

In this case, the unbalance of the DC-link voltages will be reduced during a few pulse periods.

If the new duration of vector (1,-1,-1) is positive and a sum of all vectors in the switching sequence is higher than a pulse period:

$$t_{(0,-1,-1),(1,0,0)}+t_{(1,0,-1)}+t'_{(1,-1,-1)}>T_{imp}\,, \qquad (27)$$

the duration of redundant vector should be reduced to assure the criterion:

$$t'_{(1,-1,-1)}=T_{imp}-\left(t'_{(0,-1,-1),(1,0,0)}+t_{(1,0,-1)}\right), \qquad (28)$$

where $t'_{(0,-1,-1)}$ and $t'_{(1,0,0)}$ are the new, reduced duration of redundant vectors (0,-1,-1) and (1,0,0). At the same time, the next criterion should be fulfilled:

$$\frac{t_{(1,-1,-1)}}{T_{imp}}\cdot u_{\alpha(1,-1,-1)}= \frac{t'_{(1,-1,-1)}}{T_{imp}}\cdot u_{\alpha(1,-1,-1)}+\frac{t'_{(0,-1,-1),(1,0,0)}}{T_{imp}}\cdot u_{\alpha(0,-1,-1),(1,0,0)} \qquad (29)$$

where T_{imp} is a pulse period.

The new duration of redundant vector ((0,-1,-1) or (1,0,0)) can be calculated by the substitution of (28) to (29):

$$t'_{(0,-1,-1),(1,0,0)}= \left(T_{imp}-t_{(1,-1,-1)}-t_{(1,0,-1)}\right)\cdot\frac{u_{\alpha(1,-1,-1)}}{u_{\alpha(1,-1,-1)}-u_{\alpha(0,-1,-1),(1,0,0)}} \qquad (30)$$

The negative value of $t'_{(0,-1,-1)}$ or $t'_{(1,0,0)}$ denotes that the amplitude and position on inverter output voltage makes the introduction of redundant vector impossible. The inverter output vector using sequence (10) will be generated.

The redundant vector can also be introduced to (11) sequence. The algorithm for duration calculation will be performed in the same manner as that proposed for the switching sequence (10). In the case of the DC-link voltage unbalance, the switching sequence (11) can be performed as

$$(0,0,0)\rightarrow(0,-1,-1)\rightarrow(1,-1,-1)\rightarrow(1,1,-1)\rightarrow(0,0,0) \quad (31)$$

or

$$(0,0,0)\rightarrow(1,-1,-1)\rightarrow(1,1,-1)\rightarrow(1,1,0)\rightarrow(0,0,0) \quad (32)$$

depending on the sign of "x" coefficient and direction of the neutral point current.

The choice of one switching sequence from (8)-(10) is based on minimization of the unbalance criterion.

The second calculation of unbalance criterion (14) takes into consideration all redundant vectors introduced to the switching sequences and their calculated durations. This solution makes it possible to choose an optimum switching sequence in order to reduce voltage unbalance in the DC-link. The modified switching sequence (11) can be used instead of (10) in two cases. The first - if the predicted unbalance criterion (14), calculated for (11) sequence, has a lower value in comparison with the same criterion calculated for the (10) sequence (all sequences contain redundant vectors). The second - if the unbalance criterion (14), calculated for (10) sequence (including redundant vectors) is higher than:

$$x_{max} = 2 \cdot C \cdot \Delta u_{max}, \quad (33)$$

where Δu_{max} is a maximum allowed difference between voltages on the upper and lower DC-link capacitors.

The sequences (31)-(32) contain only one redundant vector which has an influence on the DC-link voltage balance. These sequences can be used for the control of DC-link voltage balance in the case of large amplitude of the inverter output voltage or large voltage unbalance in the DC-link.

On Fig. 7 the graphical representation of proposed algorithm is presented. Table 1 presents the redundant vectors introduced to switching sequences (8)-(11) for sectors 0 and 3.

IV. Minimization of Comutation Number

The number of commutations in the proposed PWM strategy can be reduced by the appropriate choice (or elimination) of passive vectors. Switching sequences (8)-(11) can be rewritten as:

$$(1,1,1)\rightarrow(1,1,0)\rightarrow(1,0,0)\rightarrow(0,0,0), \quad (34)$$
$$(-1,-1,-1)\rightarrow(0,-1,-1)\rightarrow(0,0,-1)\rightarrow(0,0,0), \quad (35)$$
$$(-1,-1,-1)\rightarrow(1,-1,-1)\rightarrow(1,0,-1)\rightarrow(1,1,1), \quad (36)$$
$$(-1,-1,-1)\rightarrow(1,-1,-1)\rightarrow(1,1,-1)\rightarrow(1,1,1). \quad (37)$$

Introducing an additional redundant vector to (36) gives the sequence:

$$(-1,-1,-1)\xrightarrow{t_{pasiv}}(0,-1,-1)\xrightarrow{t_{(0,-1,-1)}}(1,-1,-1)\xrightarrow{t_{(1,0,-1)}}(1,0,-1)\xrightarrow{t_{pasiv}}(0,0,0) \quad (38)$$

or

$$(-1,-1,-1)\xrightarrow{t_{pasiv}}(1,-1,-1)\xrightarrow{t_{(0,-1,-1)}}(1,0,-1)\xrightarrow{t_{(1,0,-1)}}(1,0,0)\xrightarrow{t_{(1,0,0)}}(0,0,0) \quad (39)$$

where t_{pasiv} is a duration of passive vector, $t_{(0,-1,-1)}$, $t_{(1,-1,-1)}$, $t_{(1,0,-1)}$, $t_{(1,0,0)}$ are durations of active vectors.

The switching sequence (38) can be replaced by the sequence:

$$(-1,-1,-1)\xrightarrow{t_{pasiv}'}(0,-1,-1)\xrightarrow{t_{(0,-1,-1)}+\Delta t_r}(1,-1,-1)\xrightarrow{t_{(0,-1,-1)}'}(1,0,-1)\xrightarrow{t_{(1,0,-1)}}(1,0,0)\xrightarrow{\Delta t_r}(0,0,0)\xrightarrow{t_{pasiv}'} \quad (40)$$

and the sequence (39) by following:

$$(-1,-1,-1)\xrightarrow{t_{pasiv}'}(0,-1,-1)\xrightarrow{\Delta t_r}(1,-1,-1)\xrightarrow{t_{(0,-1,-1)}'}(1,0,-1)\xrightarrow{t_{(1,0,-1)}}(1,0,0)\xrightarrow{t_{(1,0,0)}+\Delta t_r}(0,0,0)\xrightarrow{t_{pasiv}'} \quad (41)$$

Both redundant vectors (0,-1,-1) and (1,0,0) have an opposite influence on the DC-link voltage balance. The duration of redundant vector is elongated for the same time, denoted as Δt_r.

For the switching sequences (40) and (41) the same criterion (42) have to be fulfilled:

$$t_{(1,-1,-1)} \cdot u_{\alpha(1,-1,-1)} = \Delta t_r \cdot u_{\alpha(0,-1-1)} + \Delta t_r \cdot u_{\alpha(1,0,0)} + t_{(1,-1,-1)}' \cdot u_{\alpha(1,-1,-1)} \quad (42)$$

where $t_{(1,1,-1)}$ is an actual duration and $t_{(1,1,-1)}$' is the new duration of (1,-1,-1) vector.
Because:

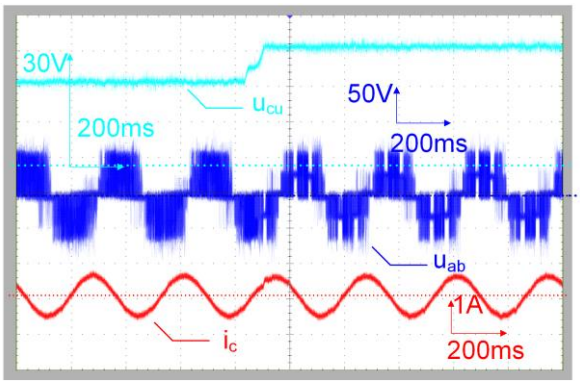

Fig.16. The voltage on upper capacitor of DC-link u_{cu}, converter output voltage u_{ab} and phase current i_c in case of voltage imbalance reduction. Fundamental frequency:3[Hz] , Uout=24V, DC-link voltage Udc=60V

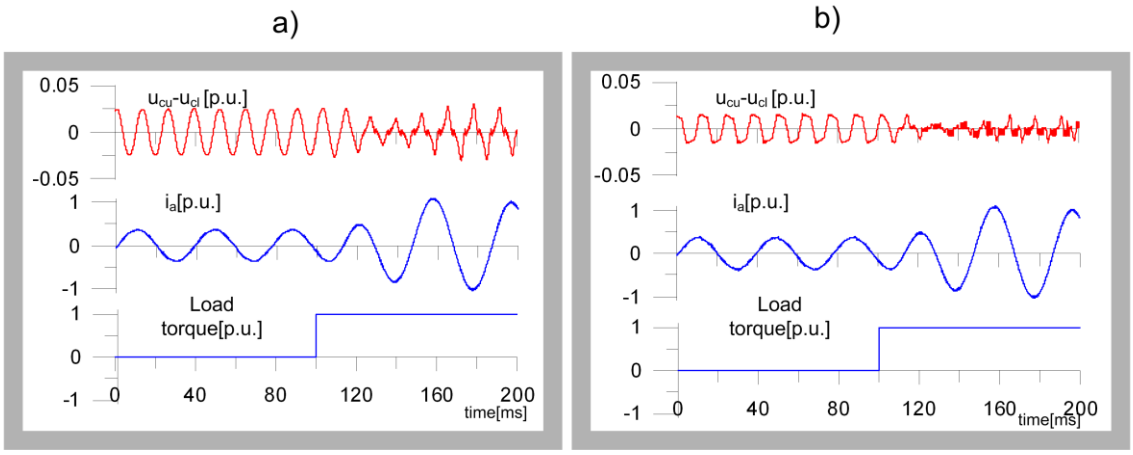

Fig.17 Result of simulation on classic SV-PWM strategy with PI controller utilized to DC-link voltage balancing a) and proposed SV-PWM strategy with prediction of DC-link voltage unbalance b). The difference between upper and lower capacitor voltages (u_{cu}-u_{cl}), the converter output current (i_a) in case of load torque changes (from 0 to nominal). The maximum allowed voltage difference for proposed SV-PWM strategy (33): Δu_{max}=5V

$$u_{\alpha(1,-1,-1)} = u_{\alpha(0,-1-1)} + u_{\alpha(1,0,0)}, \quad (43)$$

the criterion (42) can be rewritten as:

$$t_{(1,-1,-1)} = \Delta t_r + t_{(1,-1,-1)}', \quad (44)$$

The next criterion should be fulfilled:

$$t_{(1,-1,-1)} + 2 \cdot t_{pasiv} = 2 \cdot \Delta t_r + \left(t_{(1,-1,-1)}' + 2 \cdot t_{pasiv}' \right), \quad (45)$$

where t_{pasiv} is a duration and t_{pasiv}' is a new duration of passive vectors in sequences (40)-(41).
By substitution (44) to (45), the duration Δt_r. and the new duration of (1,-1,-1) vector can be calculated:

$$\Delta t_r = 2 \cdot \left(t_{pasiv} - t_{pasiv}' \right), \quad (46)$$

$$t_{(1,-1,-1)}' = t_{(1,-1,-1)} - \Delta t_r, \quad (47)$$

where new duration of passive vector t_{pasiv}' have to be chosen according to criterion

$$t_{pasiv} \geq t_{pasiv}' \geq t_{pasiv} - \frac{t_{(1,-1,-1)}}{2}. \quad (48)$$

V. Simulation and Experimental Results

The used experimental system consists of three-level inverter and three-level controlled rectifier with DC-link capacitances C_u=C_l=7.2mF, two DSP control boards for generating the PWM control signals for both converters, and unloaded induction motor with the parameters: P_n=160kW, U_n=690V, I_n=161A, cosφ=0.87, f=50Hz. The PWM sampling period T_{imp} was equal to 150μs (the Carrier frequency: 3.33kHz) . The speed of the induction motor was controlled in sensorless closed loop mode. Proposed SV-PWM strategy was used in both converters, but the control systems of converters weren't coupled. Fig. 8 and Fig.9 show the output voltage and phase current during generation of inverter output voltage when fundamental frequency is 5Hz and 15 Hz respectively. Fig 10 and 11 show the voltage on the upper capacitor of DC-link and phase current for the same fundamental frequencies. Fig 12 and 13 show the voltages on both capacitors and phase current during speed change of induction motor. The voltages on both DC-link capacitors during load change on fig 14 and 15 are presented. The difference between capacitor voltages, during experimental investigations, didn't exceed 5V. The voltage drop (shown on fig 15) is an effect of controllers' limits on rectifier control system. Such limit has been chosen not to exceed the current rating of the existing fuses.

Fig.16 presents transients of DC-link voltage, inverter phase current and output voltage in the case of voltage unbalance reduction. In this case the unbalance of DC-link voltages was forced by introducing of a non-zero value of Δu_f component into equation:

$$\Delta u = u_{Cu} - u_{Cl} + \Delta u_f, \quad (49)$$

which is used for determining the DC-link voltage unbalance. This experimental investigation (fig 16) was carried out for reduced DC-link voltage (u_{dc}=60 V) and unloaded 1.5kW induction motor. DC-link capacitances were equal to C_u=C_l=500μF.

The comparison of the proposed SV-PWM strategy and a SV-PWM strategy with PI controller-balanced DC-link voltages was realized by simulation and presented on fig 17a and 17b. The inverter parameters are: DC-link capacitance – 2 series connected capacitors (500μF each), DC-link voltage 564V (1.41 p.u). The model used is the NPC inverter supplies an induction motor with parameters: P=1.5kW, Un=400V, In=3.5A. Sampling period T_{imp}=150μs. Motor control strategy – scalar control U/f=const with commanded frequency 18Hz. In both SV-PWM strategies, the sector division of space

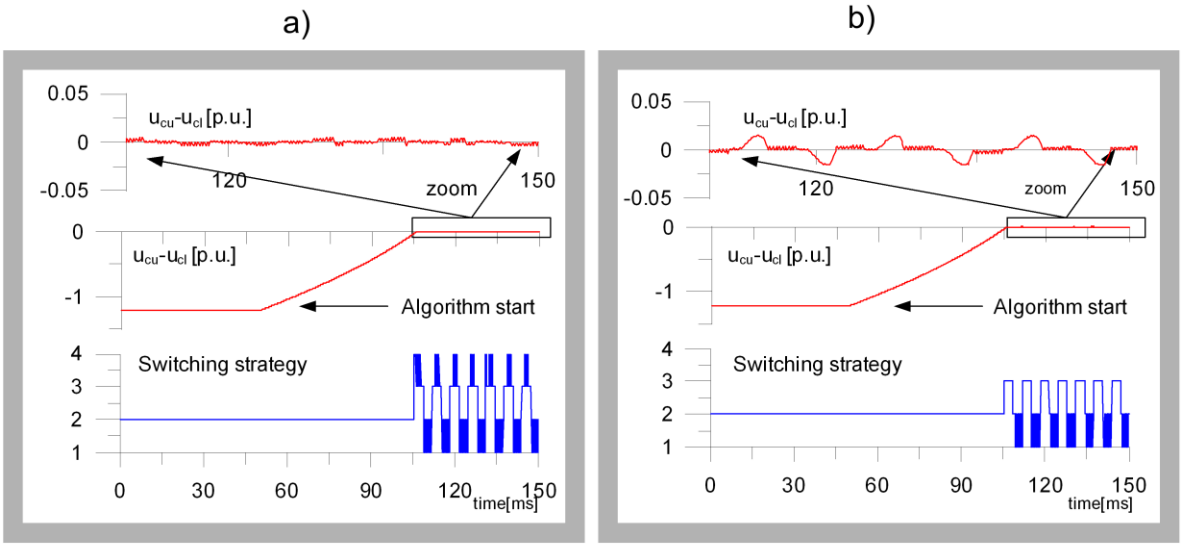

Fig.18. Result of simulation on proposed SV-PWM strategy. The difference between an upper and lower capacitor voltages (u_{cu}-u_{cl}) and used switching strategy (1- sequence (8), 2 – sequence (9), 3-sequence (10), 4- sequence (11) in case of unbalance, for maximum allowed voltage difference (33) Δu_{max}=0.5V a) and Δu_{max}=10V b)

vector area takes into account the position and amplitude of active vectors, as shown in Fig. 6. The switching sequences, used in SV-PWM strategy with PI balance controller, contain two redundant vectors. For sector ”0“ there are redundant vectors (0,-1,-1) and (1,0,0) with durations $t_{(0,0,-1)}$ and $t_{(1,0,0)}$ respectively:

$$\begin{aligned}&(0,0,0)\rightarrow(0,-1,-1)\rightarrow(1,-1,-1)\\&\rightarrow(1,0,-1)\rightarrow(1,0,0)\rightarrow(0,0,0)\end{aligned}, \qquad (50)$$

The durations of redundant vectors are equal to:

$$\begin{aligned}&t_{(0,-1,-1)}=\frac{t_a}{2}\cdot(1+f),\\&t_{(1,0,0)}=\frac{t_a}{2}\cdot(1-f), \quad ,\\&f\in\langle-1,1\rangle\end{aligned} \qquad (51)$$

Where t_a – the duration of both redundant vectors in a switching sequence, f- control factor set by DC-link balance controller.

VI. Conclusion

In this paper a new SV-PWM strategy for 3-level NPC converter is proposed. In the proposed solution, the division of space vector area into sectors is based on the analysis of position and length of boundary vectors. It allows properly generating the inverter output voltage, even in the case of large voltage unbalance in the DC-link. Proposed modulation strategy takes into consideration voltage unbalance, neutral point current and DC-link capacitance for determining the duration of redundant vector in switching sequence. For each of the twelve sectors, four alternative switching sequences are defined. The optimum choice of one of switching strategies is based on the analysis of predicted voltage unbalance for any sequence, including their capability of reducing the voltage unbalance. Choice of the redundant vectors introduced to switching sequences and selection of their durations makes the reduction of voltage unbalance very fast.

The proposed PWM strategy, similarly to other control strategies, utilizes redundant active vector in switching sequence in order to reduce the DC-link voltage unbalance. The main differences are in selecting methods of redundant vector duration. The prediction of voltage unbalance allows reducing the voltage unbalance before its occurrence.

Additionally, in the proposed method it is possible to use four alternative switching strategies to reduce voltage unbalance as fast as possible. In most cases the balancing of DC-link voltages relies on using one of three sequences (seq. 8-10). The maximum voltage unbalance, which makes it possible to activate sequence (11), can be set by equation (33). Figures 18a and 18b show the difference between an upper and lower capacitor voltages (u_{cu}-u_{cl}), and utilized modulation strategy in case of large DC-link unbalance occurrence for Δu_{max}= 0.5V and Δu_{max}=10V respectively. The motor load was set to 0.5 p.u, however the rest of simulation parameters were the same as used for fig.17.

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Arkadiusz Lewicki received the M.Sc. and Ph.D. degrees in electrical drives from the Faculty of Electrical Engineering, Gdansk University of Technology, Gdansk, Poland in 1998 and 2003, respectively. He is currently with the Institute of Automatic Control of Electric Drives, Gdansk University of Technology. His scientific activities are concentrated on microprocessor control of converters, pulse width modulation techniques, and nonlinear control.

Zbigniew Krzeminski received the Ph.D. degree from the Technical University of Łodz, Łodz, Poland, in 1983 and the D.Sc. degree from Silesian Technical University, Gliwice, Poland, in 1991. From 1993 he is a Professor of Electrical Engineering at Gdansk University of Technology. His main areas of research interests are modeling and simulation of electric machines, control of high performance electric drives and signal processor based control systems.Prof. Z. Krzeminski is author of over 130 articles, 2 books and 6 patents. Main achievements of prof. Z. Krzeminski is development of multiscalar models of the induction motor, which are generalized form of known vector model, and invention of variable observer for the induction motor used in sensorless drives.

Haitham Abu-Rub (M'99–SM'07) received the M.Sc. degree in electrical engineering from the Gdynia Maritime University, Poland, in 1990 and the Ph.D. degree from Gdansk University of Technology, Poland, in 1995, in which he was later on hired as assistant professor.

For eight years, he has been hired as an Assistant Professor and as an Associate Professor at Birzeit University, Palestine. For four years, he has been appointed the Chairman of Electrical Engineering Department at the same university for four years. He is currently an Associate Professor with Texas A&M University at Qatar. His main research interests include electric drives and power electronics.

Dr. Abu-Rub is the recipient of many prestigious international awards, such as the American Fulbright Scholarship (at Texas A&M University), the German Alexander von Humboldt Fellowship (at the University of Wuppertal), the German DAAD Scholarship (at Bochum University), the British Royal Society Scholarship (at Southampton University), and others. Dr. Abu-Rub has published more than one hundred journal and conference papers.