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Wideband Modeling of DC-DC Buck Converter with GaN Transistors

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Abstract: The general wideband modeling method of the power converter is presented on the example of DC-DC buck converter with GaN High Electron Mobility Transistors (HEMT). The models of all basic and parasitic components are briefly described. The two methods of Printed Circuit Board (PCB) layout parameter extraction are presented. The results of simulation in Saber@Sketch simulation software and measurements are compared. Next, the model of the converter is reduced to obtain one lumped inductance of the input filter PCB for the analytical prediction of transistor turn-off ringing frequency and overvoltage. The practical use of the model is presented for sizing optimal capacitance of snubber.

Keywords: wideband modeling; converter modeling; DC-DC converter; GaN HEMT; PEEC

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1. Introduction

Today's power electronics converters are increasingly more often build using the Wide Bandgap (WBG) semiconductor switches. These allow operating with higher switching frequency and shorter turn on and turn off times. Unfortunately, it is a reason for increasing the electromagnetic interference (EMI), oscillations, and overvoltages. For the designing process of the power converter, it is preferred to forecast the high-frequency phenomena with satisfying accuracy, in the early stage of design. The WBG semiconductors like Silicon Carbide (SiC) or Gallium Nitride (GaN) require improving the simulation methods with high precision of model parameters and accurate results.

Many authors present the wideband modeling methods for predicting EMI [1–4]. In [5], the models of SiC power modules and Schottky diode based on I-V and C-V characteristic are presented. The high-frequency model of GaN-Based LLC Half-Bridge Converter—shown in [6]—allows forecasting CM current, but semiconductor devices' models are too simple to obtain an accurate result. The precise model of GaN-HEMT transistor can be found in [7], but the demonstrated circuit of boost converter does not include the parasitics of other components and layout. The model of boost converter from in [8] yields accurate results, but it is not described in detail. In [9], the authors focus on cable and motor impact on high frequency oscillations and power losses.

In this paper, the general procedure of wideband modeling of switched-mode power supply (SMPS) based on GaN-HEMT transistors is presented by the example of DC-DC buck converter. The operation mode, the switching strategy, and the efficiency of converter are described in details in [10]. The main objective of this paper is to build the converter model which allows forecasting of EMI generation in the conducting interference frequency range for effective overvoltage limitation in the design stage. First, the topology of the converter is presented. In Section 3, the modeling procedure of semiconductor device is shown. In Section 4, models of passive components are briefly described. Next, layout of

the PCB model and its reduction are shown in Section 5. Finally, simulation results are compared with measurement in Section 6, and the simulation is used to find the optimal value of snubber capacitor in Section 7.

2. Topology of GaN Buck Converter

The converter including GaN HEMTs in cascode structure from Transphorm (TPH3207WS: 650 V/50 A) supplied through the line stabilization network (LISN) Schaffner NNB 41 from the DC voltage source is presented in Figure 1. The input capacitor C_{in} consisted of three parallel connected polypropylene capacitors (5 µF, 10 nF, and 100 nF). The output low pass LC filter was sized to the cut-off frequency f_c = 1630 Hz. In the load R_{load}, the power of 350 W was dissipated at the output value V_o = 55 V. The gate driver based on Si8275 IC enabled control signal insulation and the output stage of the driver [11]. This topology allows operating in synchronous and asynchronous mode. In this paper, the converter operation was tested in discontinuous current mode and triangular current mode [12], where only the upper transistor was controlled and only the lower side reverse diode of the Cascode GaN structure was used.

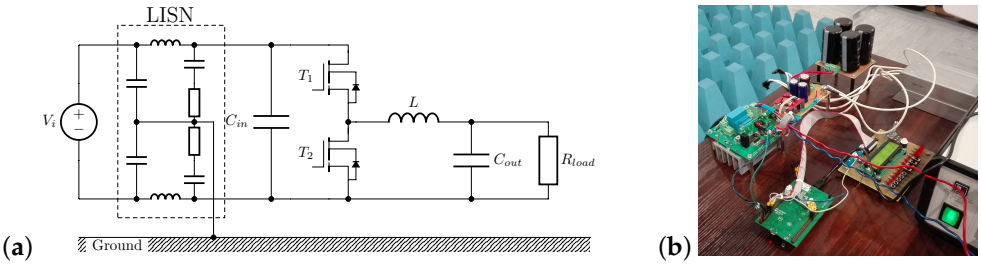

Figure 1. The buck converter: (**a**) circuit schematic and (**b**) experimental setup.

3. GaN HEMT Transistor Model

The GaN transistors are characterized by the possibility of changing their state in a very short time with the fast switching edges. The rapid changes in voltages and currents in the converter are the main origin of the EMI generation. The transistor model should reflect its dynamic including recharging of nonlinear capacitance. Moreover, the parasitic components should be included, because they are usually a part of the internal resonant circuit in the converter and play a great role in oscillation and overvoltage generation. The instantaneous value of internal capacitance depends on voltage V_{DS}. The characteristics can be found in the manufacturer's data sheet, but the given values there may be burdened with a statistical error that may significantly affect the simulation results. The wideband model of GaN transistor applied for simulation study is presented in Figure 2.

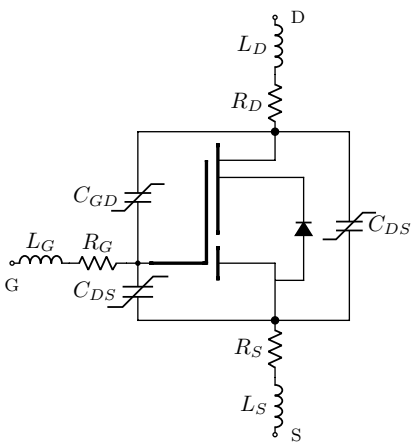

Figure 2. Equivalent circuit of GaN transistor.

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The internal structure of the GaN FET transistor used is cascode of high-voltage GaN HEMT and low-voltage MOSFET [13,14]. Without knowing the internal structure, it is impossible to measure the capacitance of each of these transistors separately. Therefore, the capacitances have been modeled as it is presented in manufacturer data-sheet. Moreover, the tools included in Saber@Sketch allow to model only one internal transistor.

The parasitic capacitance of a transistor results from its internal structure, in which the areas with different potentials are very close to each other. Typical capacitance characteristics in transistor data sheets are input capacitance $C_{ISS} = C_{GS} + C_{GD}$, output capacitance $C_{OSS} = C_{DS} + C_{GD}$, and transfer capacitance $C_{RSS} = C_{GD}$. In order to obtain a precise model, the characteristics of internal capacitances should be measured for the applied transistors. The direct measurement of these parameters with impedance analyzer or RLC bridge is not possible, because the mentioned devices do not provide a sufficiently high voltage, which should be applied between drain and source of the transistor. Accordingly, external auxiliary circuits have been proposed in [15] enabling the measurement with suitable voltage range of V_{DS} from an external source. The isolating ceramic or polypropylene capacitor $C_{is} = 1$ µF connected to the impedance analyzer provides isolation between the measuring device and the positive node of DC voltage (Figure 3).

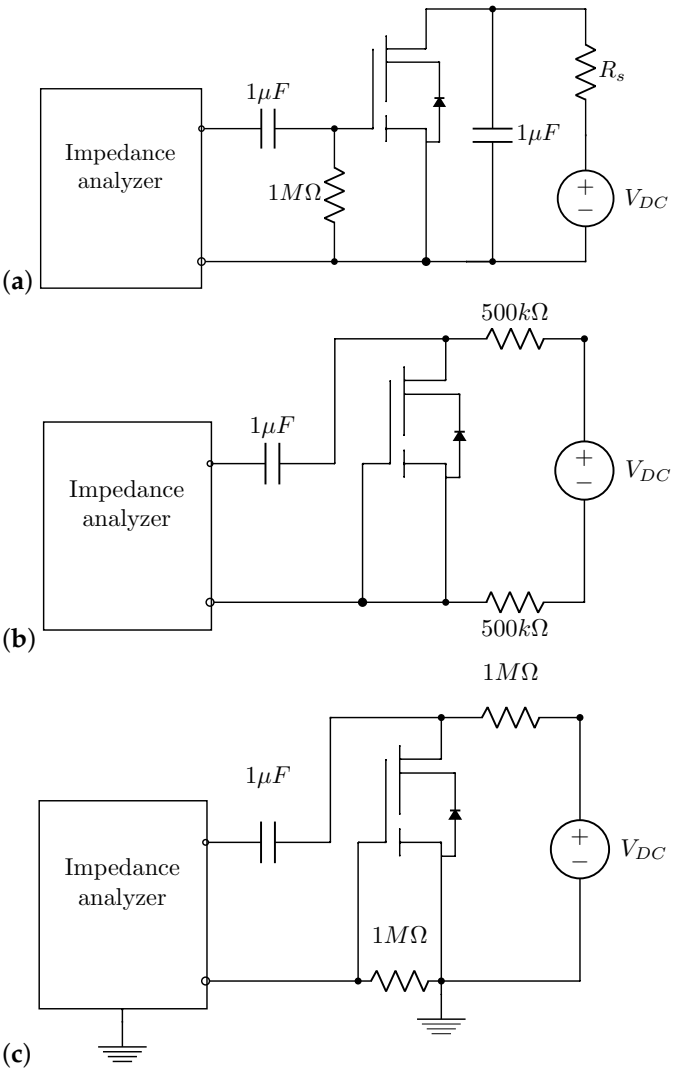

Figure 3. Schematics of dedicated circuits for transistor capacitances measurement: (**a**) C_{ISS}, (**b**) C_{OSS}, and (**c**) C_{RSS}.

In the considered converter, the capacitances have been measured using impedance analyzer Keysight E4990A. The results of measurement are compared with data from

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producer data-sheet in Figure 4. The presented differences— especially for C_{ISS}—result from the technological spread in the production of transistors. Note that in the simulation of experimental setup, such a discrepancy can cause significant errors.

The internal gate resistance is modeled as a series resistor and represents a combination of many internal resistances in a semiconductor structure. The value of this resistance is an important parameter as it directly influences the RC time constant of the gate and determines the maximum switching speed of the transistor. However, usually this parameter is not listed in data-sheets, but it can be measured. The gate resistance of the TPH3207WS transistor measured with an impedance analyzer is $R_G = 3.95\ \Omega$.

The total stray inductances of the transistors are composed of two different parts: internal and external (connections). The internal stray inductances cannot be measured by the user as there is no access to the internal structure of the transistor. Accordingly, the building of the transistor model should consider internal stray inductance (values delivered by the manufacturer in the datasheet or extracted from the simulation model) and external ones (measured by the user). The assembly technology affects the model to be accompanied by a parasitic inductance of connections of transistor-external stray inductance. For SMD (surface mount), inductances that come from connections could be neglected, but for THT (through-hole-technologies assembly) connecting wires should be included in the total value of L_g, L_s, and L_d (Figure 2). The resistance of the connection is negligibly small. For the considered transistor housing TO-247, the connection is 10mm long, which results in parasitic inductance of about 10 nH (total stray inductance values: L_g = 12 nH, L_d = 13 nH, L_s = 11 nH). Note that these values are given for the nominal length of connections but in the real converter, they can be smaller because of the quality of mounting (shorter connections between TO-247 and PCB).

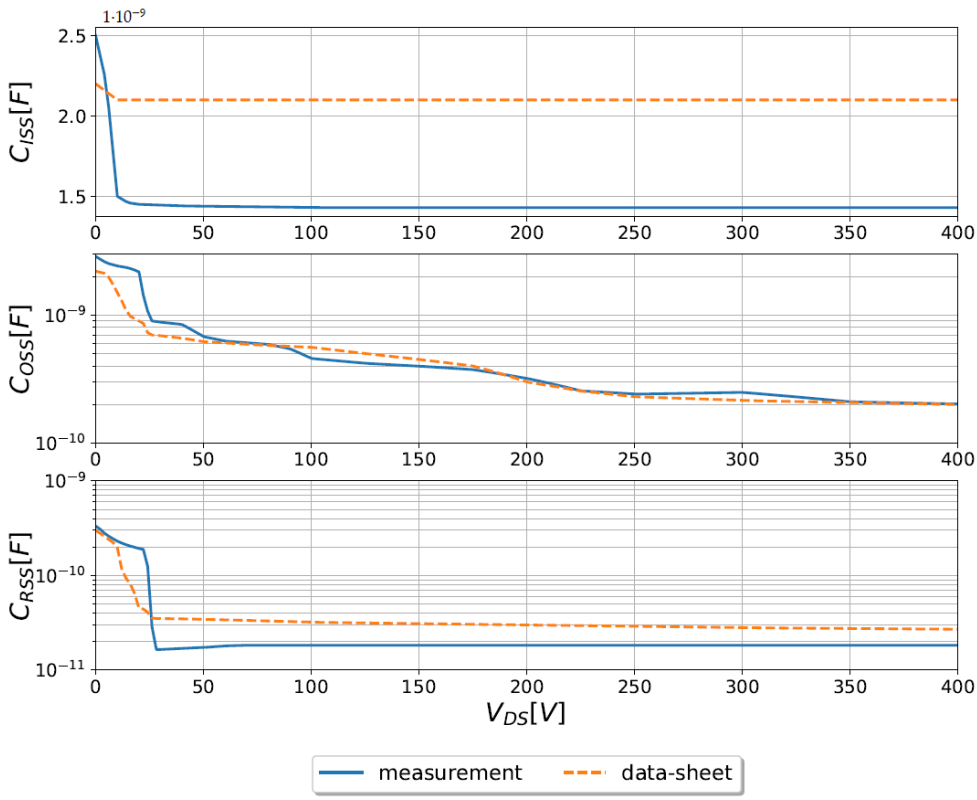

Figure 4. TPH3207WS GaN capacitances.

4. Passive Components Model

The widebanded passive component models—in addition to the basic parameter—should contain components that represent physical high-frequency phenomena such as ESR—equivalent series resistance, EPR—equivalent parallel resistance, ESL—equivalent

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series inductance, and EPC—equivalent parallel capacitance. The models of capacitor and inductor used in the simulation are presented in Figure 5.

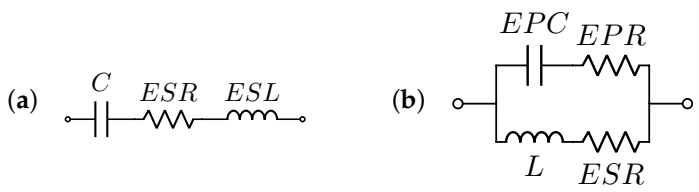

Figure 5. The equivalent circuit of (**a**) capacitor (**b**) inductor.

The parameters of input capacitor C_{out} and inductor L are presented in Table 1 and their impedance in the frequency domain is presented in Figure 6. Note that the character of impedance changes for higher frequency. The presented capacitor starts to behave like an inductor for a frequency above 10 kHz. Similarly, the impedance of the inductor changes its character in the frequency range above 26 MHz.

The equivalent circuit parameters of all passive components (as in Figure 1a) have been measured using the impedance analyzer Keysight E4990A. The presented model of inductor gives proper results in conducted EMI frequency range, but it does not take into consideration the saturation of the core. If it is necessary to include saturation, the model should be extended [16].

Table 1. The parameters of input capacitor C_{out} and inductor L.

Component	Parameter	Value
C_{out}	C	985 µF
	ESR	124 mΩ
	ECP	338 nH
L	L	8.7 µH
	ESR	33 mΩ
	ESL	4.8 pF
	EPR	922 Ω

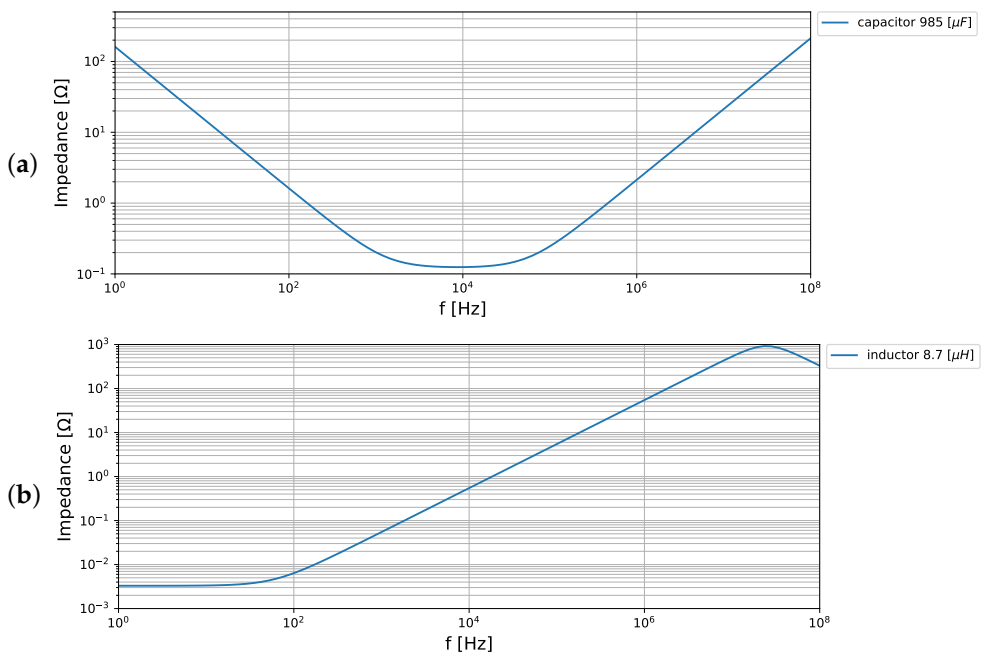

Figure 6. Passive components impedance: (**a**) capacitor C = 985 µF and (**b**) inductor L = 8.7 µH.

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5. PCB Layout Model

The PCB layout, including the conducting tracks, wires, and cables, has primary importance in high-frequency behavior of the converter. The magnetic and electric couplings of conducting tracks can be represented by the coupled inductors and capacitors. These components are part of the resonant circuit responsible for overvoltages and oscillations at transistor turn off. Many software tools are offered to model PCB parasitics. In this paper, authors focus on the Q3D Extractor from Ansys and PEEC (Partial Element Equivalent Circuit) method [17] used by InCa3d from Altair. The geometry of layout is defined or exported to the applied software environment and next ready-to-use model is generated. The PEEC method allows calculating the value of resistance and self- and mutual inductances using geometrical and physical properties of the tracks. The formulas can be directly implemented in the computing environment. In the presented example of buck converter, the PEEC method has been implemented in the Matlab software by authors. Based on formulas from in [17], the Matlab functions have been written, where the input variables were entered manually in accordance to the dimension of the conduction tracks.

Using the Q3D Extractor, first sources and sinks should be defined and then the model including the following:

- inductors equal to half of the inductance between two nodes,
- inductive couplings between each inductor,
- resistors representing AC and DC resistance of the tracks,
- capacitors for capacitance between previously defined sources and between sources and artificial reference point.

Using the artificial reference points allows to define the capacitance between each conducting track and also the ground if it is placed within the circuit. However, the user has no access to this point in the generated ready-to-use model. Thus, the additional reference point of ground should also be included in the Q3D model. In the Q3D Extractor, models are generated for the one selected frequency, thus for other frequencies (e.g., harmonics) an inaccuracy may appear. However, the great advantage of these models is their numerical stability.

In the PEEC method, each conductor is segmented. Next, resistance, self-inductance and mutual inductance between each segment are calculated. In this approach, a frequency-independent model that takes into account skin or proximity phenomena is obtained.

The topologies of both models are totally different. However, the simulation of both models should provide the same results. In order to show the differences, models of two conducting parallel tracks (two microstrip example) are shown in Figure 7. The Q3D model of Figure 7b includes RL components, capacitors between A and B sources, and a reference point. The C and D points were defined as sinks. The magnetic coupling is realized by the use of coefficient k.

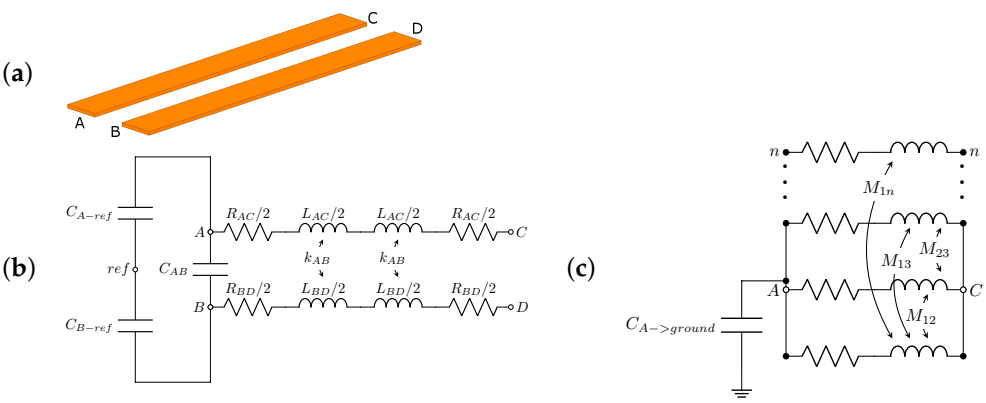

Figure 7. The example of two conducting copper track (**a**) geometry view (**b**) model generated with Q3d Extractor (**c**) model generated with PEEC method.

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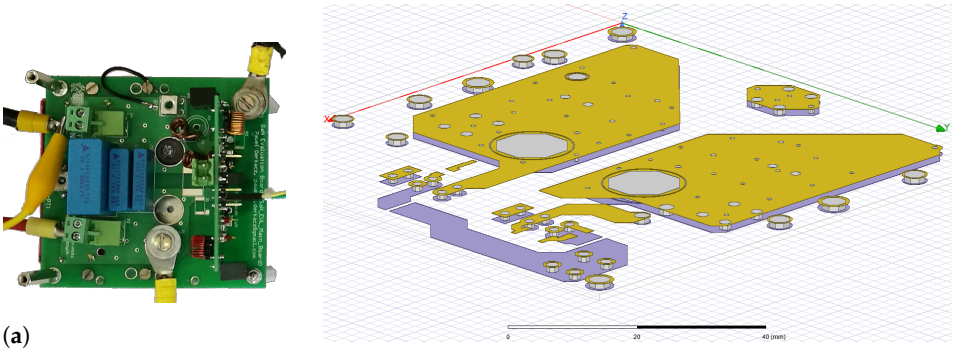
In order to keep the clarity of the diagram, the PEEC model of only one track is presented in Figure 7c. It is divided into n number of segments.

The presented circuit is simplified: the complete model should contain the same model of the second track and the mutual inductances M between all segments of both tracks and capacitance between them.

For the considered GaN HEMT buck converter, the parasitic inductances of PCB have been calculated using the PEEC method and parasitic capacitance to the ground with the Wheeler–Schneider formula [18]. The top view of the converter and the geometrical model is presented in Figure 8. The Saber@sketch simulation schema of PCB and the three input capacitors from Saber@sketch is shown in Figure 9. The conducting tracks are represented by lumped RLC components with the included matrix of mutual inductance M merged in MAST language. In order to show the range of values, the example parameters are shown in Table 2.



(**a**) (**b**)

Figure 8. The PCB of the presented buck converter (**a**) view from the top (**b**) geometrical model of PCB.

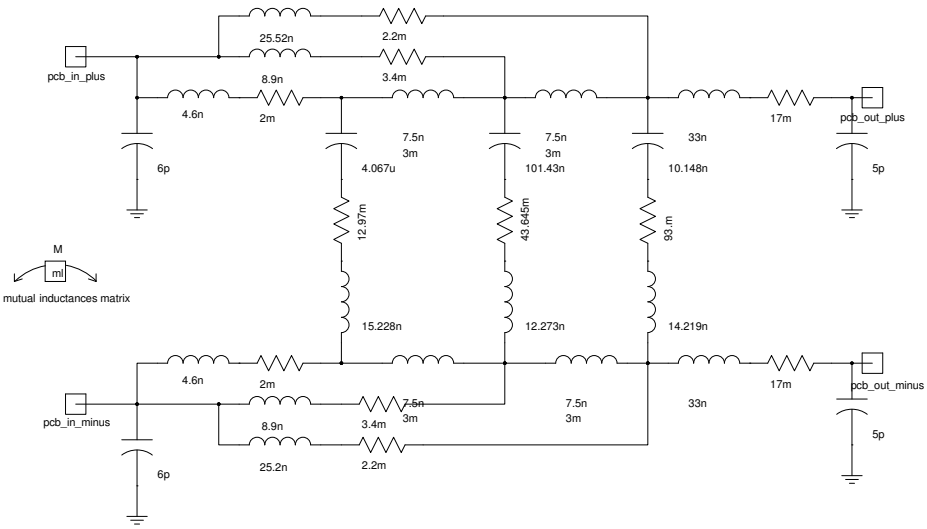


Figure 9. The equivalent circuit of the PCB with the capacitive input filter.

Table 2. Parasitic values of PCB for the presented buck converter.

Parameter	Value	Unit
L_1	4.6	[nH]
R_1	2	[mΩ]
$C_{1\to GND}$	6	[pF]
$M_{1\to 6}$	0.07	[nH]

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6. Simulation Results

The wideband simulation circuit of buck converter from Figure 1 was composed of the elements described in previous section of this paper using Saber@Sketch simulator from Synopsys Inc. The scheme includes the power supply U_i = 70 V, the inductance model of PCB layout as hierarchical circuit with lumped capacitors represented capacitance to the ground of main conducting tracks, semiconductors, and passive elements models. Moreover, the simplified model of transistor gate driver described in details in [11] was included.

The entire simulation circuit can be a heavy burden on the simulation software because it contains numerous elements, including nonlinear elements. Therefore, it is necessary to check if that the calculations are free of calculation errors and that the whole system is numerically stable. The simplest and most effective method of checking the numerical stability is to run a series of simulations for various numerical conditions, e.g., calculation step or truncation error. If the simulation results do not differ significantly (there are any unexpected variations or an increase in the current and voltage values), it can be concluded that the obtained results are not burdened with numerical errors. If the results are not stable, it is recommended to add low value resistors in series with the nonlinear elements.

Another important aspect is adequate simulation time so that the circuit is in a quasi-steady state (all capacitors should be charged). In the Saber@sketch software, it is possible to continue the second simulation with initial conditions from the previous one. The simulation of the presented circuit was performed as follows:

1. the DC analysis was done in order to estimate all voltages quasi-steady state,
2. the time simulation with relative large calculation step (1 µs) and long time (10 ms) to obtain the steady state (operation point) of the converter,
3. short time simulation (100 µs) with a small step (1 ns).

The results obtained with short time simulation are present in Figure 10b and compared with the measurement. The inductor current i_L and voltages across both transistors waveforms are satisfactorily coherent in the time domain.

However, slight differences can be noticed when comparing the spectra. In Figure 11, the spectra of voltages across the transistor T_1 are compared. The levels of harmonics derived from the switching frequency are almost equal (up to 5 MHz). The peaks linked with ringing during transistor turn off ($f_{rT1} \sim 21$ MHz) and diode turn off ($f_{rD} \sim 44$ MHz) overlap for simulation and measurement. The ringing frequencies depend mainly on the internal capacitance of semiconductor devices and the parasitic inductance of the input part of PCB.

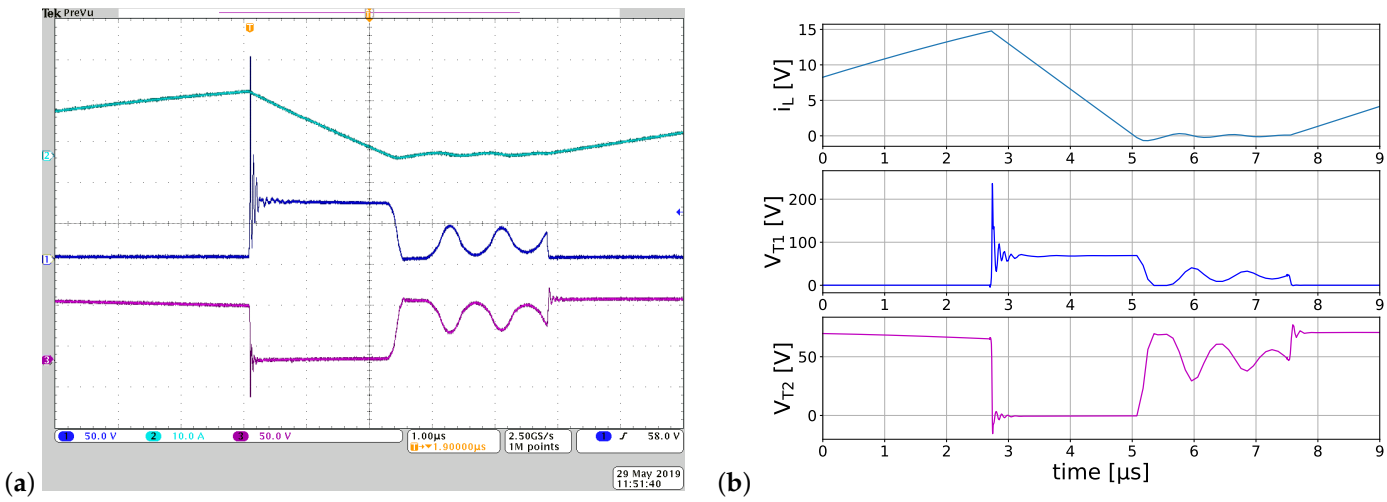

Figure 10. The buck converter at DCM operation (i_L, V_{T1} and V_{T2}): (**a**) experiment (time: 1 µs/div, i_L: 10 A/div, V_{T1}, V_{T2}: 50 V/div) and (**b**) simulation.

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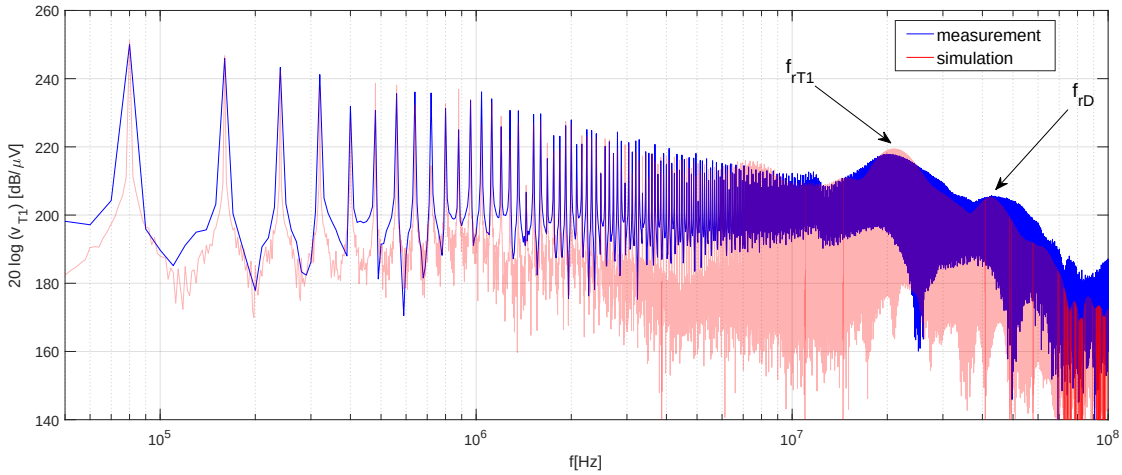

Figure 11. The comparison of V_{T1} spectra measured and simulated.

Model Reduction

Usually, models obtained with calculation software can not be used in analytical analyses, so the reduction to a few lumped components model is applied. In [10], the value of the leakage inductance was needed in order to calculate the value of overvoltage after commutation. The AC signal analysis has been performed to find the values of the lumped parasitic inductance of this part of the circuit. First, the model of tracks PCB of input filter was extracted and exported into circuit simulator Saber@Sketch (Figure 9) and fed by AC current source equal 1A (placed on the high-side transistor location) as it is shown in Figure 12a. The output of the PCB model was shortened. Using the results of the simulation, the impedance viewed from the current source was determined in the frequency domain. The calculations were performed in two cases: the first one with PCB tracks only, the second one with PCB tracks and three input capacitors included. Assuming that resistance is the dominant parameter for low frequencies, it can be read directly from the characteristic in Figure 12b. For higher frequencies, the impedance equals the geometric sum of resistance and inductance, thus the value of inductance can be calculated using the Formula (1).

$$L_s = \frac{\sqrt{Z^2 - R^2}}{2\pi f} \tag{1}$$

For the considered buck converter, the calculation has been preformed for: Z(f = 1.4 MHz) =1 Ω, R = Z(f = 1 Hz) = 30 mΩ, which results L_s = 113.63 nH.

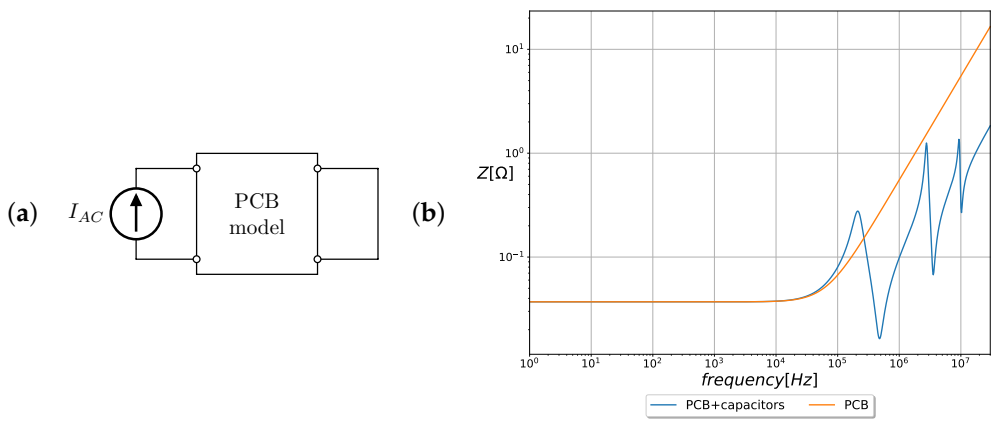

Figure 12. The models reduction based on impedance analysis.

Another method is to use the value of the first resonant frequency for the circuit including the parasitic inductance of PCB and three input capacitors using Formula (2).

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The values for calculation are f_r = 208 kHz and C_{in} = 5.11 µF, which result L_s =114.6 nH. The values from both methods should agree, but in this case the difference is 1nH, which may be due to non-precise frequency measurement.

$$L_s = ((2\pi f_r)^2 C)^{-1} \tag{2}$$

7. Sizing of the Snubber Capacitor

The accurate wide-band modeling allows obtaining precise information about the overvoltage and ringing after semiconductor devices commutation. One of the examples (proposed by authors) can be solving the problem of unwanted overshoot. Presented simulation scheme was used to to design the attenuating component like the snubber. Usually, design procedure of the snubber is based on a laboratory measurement on the prototype after its realization. However, the simulation allows to do it on an earlier design stage and find optimal properties of components and adapt the layout to the required snubber.

Using the varied parametric analysis in Saber@Sketch, it is possible to perform series of simulations for changing the value of one chosen parameter in the whole simulation circuit. The range and the changing step can be set in the software as "by step", linear, or logarithmic. In order to find the optimal value of the snubber capacitor parallel connected to transistors, the model from Saber@Sketch library was modified. The value of capacitance was set using an external control signal source for both capacitors as it is shown in Figure 13. Using the control source value as a parameter allows performing parametric analysis with changed capacitance value in both capacitors simultaneously. The simulation series were performed varying the snubber capacitors in the range from 10 pF to 10 nF.

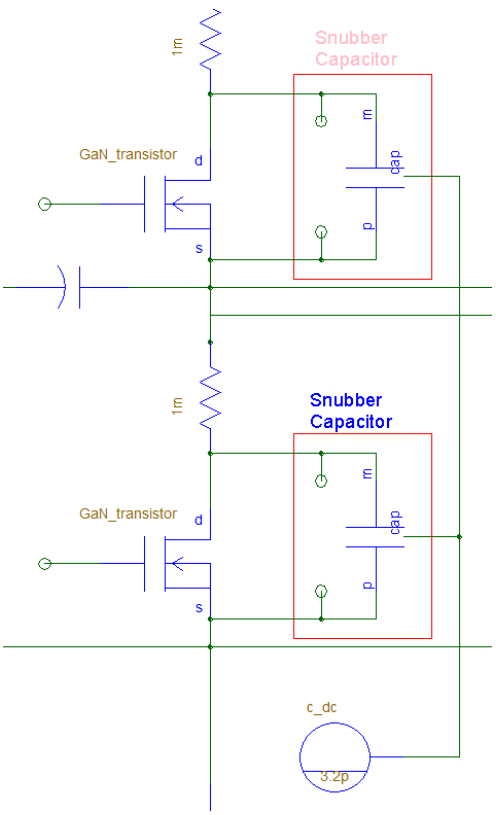

Figure 13. The part of Saber@Sketch schema for determination of the optimal snubber capacitor.

After extracting data from the result of the simulation series, the maximum value of voltage across the transistor T_1 can be presented in the function of the snubber capacitance as in Figure 14. The results are similar as presented in [10], where the analytical formula was used.

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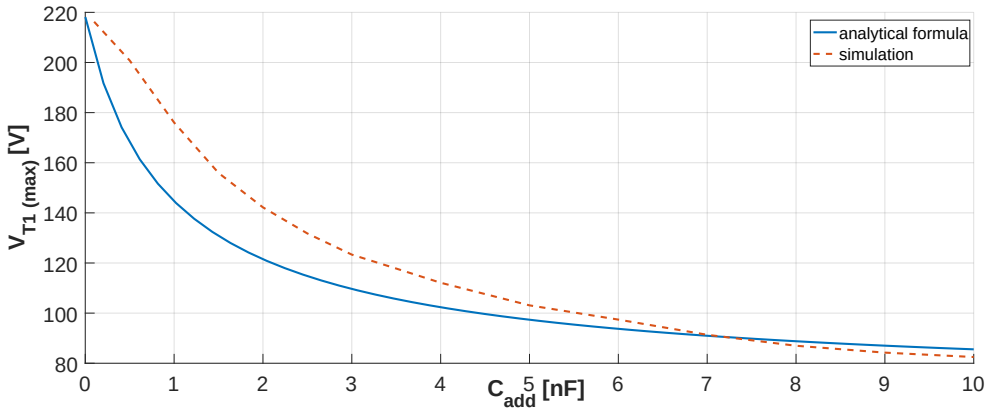

Figure 14. The overvoltage characteristic in the function of the snubber capacitor value: (—) calculated with analytical formula from [10] and (- -) Saber@sketch simulation

8. Conclusions

The accurate forecasting of EMI generation and propagation allows ensuring the required levels of interference in the early design stage. The use of fast semiconductor switches, such as wide gap transistors, requires increased modeling accuracy and verification of parameters provided by the manufacturer. Models of all—both basic and parasitic—components should reflect their behavior in the entire required frequency range. In this paper, the modeling methodology is described and used on the example of DC-DC buck converter. The comparison of the obtained simulation results with waveform and spectra from measurement confirms the correctness of the method. Moreover, the model is used to extract the chosen parasitic parameter of the PCB and determine the optimal snubber capacitance value.

Author Contributions: Conceptualization, P.M. and P.B.D.; methodology, P.M. ; software, P.M. and P.B.D.; validation, P.M.; formal analysis, P.M. and P.B.D. and P.J.C.; investigation, P.B.D.; resources, P.J.C.; data curation, P.J.C.; writing—original draft preparation, P.M.; writing—review and editing, P.J.C. and P.B.D; visualization, P.M.; supervision, P.M.; project administration, P.J.C.; funding acquisition, P.J.C. All authors have read and agreed to the published version of the manuscript.

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